EE 140 / 240A Analog Integrated Circuits

Spring 2015

MWF 1-2pm, 540 Cory
Class info, homework questions, etc.: piazza (signup)

My policy on CHEATING. READ IT!

Instructor **Office Hours**	Kristofer S.J. Pister pister@eecs <-- easiest method of contact 512 Cory Hall W 9-10, F 2-3
TAs, OH	Fil Maksimovic, fil@eecs.berkeley.edu, M 9-10, W 4-5 Mike Lorek, mlorek@berkeley.edu, Th 2-3
Required Texts	Gray, Hurst, Lewis, Meyer, *Analysis and Design of Analog Integrated Circutis*, 5th edition.
Suggested reference	Razavi, *Design of Analog CMOS Integrated Circuits* Johns and Martin, *Analog Integrated Circuit Design* Horowitz and Hill, *The Art of Electronics*
Grading	Homework & labs 25% Midterms (2) 20% Project 25% Final 30%
Homework	Collaboration is encouraged; copying is not. Explaining how you solved a problem to someone is fine; handing them your solutions is not. Helping someone debug their schematic or circuit is fine; giving them your schematic is not. Write your own answers and draw your own schematics without staring at someone else's.
Project	

Schedule

Week	Lectures by Date	Topic	HW & labs	Reading (GHLM)
1	1/21 1/23	Introduction: what is 140 all about; Op-amps circuits	hw1 Lab1 2T2Ropamp 2T2RopampFB 3T3Ropamp 3T3RopampFB	Page xiv symbol conventions; 1.5, 1.6 MOS large & small signal models; skim chapter 3
2	1/26 1/28 1/30	Taylor, Heaviside, and Bode diode, BJT, & MOS physics	hw2 RoI chart pdf pptx	1.2

		MOS small signal model(s)		
3	2/2 2/4 2/6	Common source frequency response	Lab2 hw3+lab3	7.1, 7.2.1 up through eqn. 7.27 3.1, 3.2, 3.3.2
4	2/9 2/11 2/13	CS; single-pole; input pole Cascode Active load, body effect	hw4	3.3.5 (eqns. 3.55 and 66) 3.4.2.2 (eqns 3.126, 127, 128) Figure 4.17
5	2/16 2/18 2/20	Presidents Day. no classes Common gate; Review Midterm I 1 page notes, 2 sides	sp08 mid1 solutions fa09 mid1 solutions	
6	2/23 2/25 2/27	Current mirrors Differential pair Differential amplifier	Lab4b BJTopamp BJTopampUnityFB BJTopamp100xFB hw5	3.5.{3,4,5} MOS diff pair (eqns. 161, 171..174, 188, 189, 191, 199, 201; Fig 3.51) 4.2.2.2 MOS current mirror (eqns 17..20) 4.3.1, 4.3.5.2 Active loads (eqns 143, 149)
7	3/2 3/4 3/6	2 stage op-amp feedback, stability frequency response	Frequency response notes hw6	6 read 6.1.1, skim through eqn 6.25 6.3 through 6.3.5 inclusive 8 through 8.2 inclusive 9.1,2
8	3/9 3/11 3/13	2 stage op-amp	Miller compensation figures hw7	9.3 through 9.4.3 inclusive
9	3/16 3/18 3/21	Folded Cascode	hw8	6.6
	3/23 3/25 3/27	SPRING BREAK! Pray for snow.	SNOW	SNOW
10	3/30 4/1 4/3	folded cascode biasing, high-swing mirror, review Midterm II Extended class period: 1:10 2:30 for the exam	old exams preliminary final project spec updated	
11	4/6 4/8 4/10	Supply-independent biasing Switched capacitors ADCs and DACS	Lab5 hw9	4.4.2, 4.4.3 biasing; with emphasis on the MOS parts 6.1.7.1 Switched capacitor amplifier Wikipedia: ADC, SAR ADC
12	4/13 4/15 4/17	Switched capacitors	Lab6 hw10	4.2.5.2 high swing current mirrors
13	4/20 4/22 4/24	Switched capacitors Presenting results; const-gm biasing		
14	4/27 4/29	rail-to-rail input and output Ri, Ro, and feedback		

	5/1	noise		
15	5/4 5/6 5/8	RRR week. Project presentations.	hw11 (finals prep)	

- Final Exam: Tuesday, May 12, 8-11 AM