EE 140 / 240A Analog Integrated Circuits

Spring 2016

MWF 1-2pm, 293 Cory
Class info, homework questions, etc.: piazza (signup)
previous semesters: 15sp, 09fa
lectures; homework

My policy on CHEATING. READ IT!

Instructor **Office Hours**	Kristofer S.J. Pister pister@eecs <-- easiest method of contact 512 Cory Hall if my door is open, feel free to come in M 9:30-10:30, W 2-3
TAs, OH	David Burnett, db@eecs.berkeley.edu, tba
Required Texts	Gray, Hurst, Lewis, Meyer, *Analysis and Design of Analog Integrated Circuits*, 5th edition.
Suggested reference	Razavi, *Design of Analog CMOS Integrated Circuits* Johns and Martin, *Analog Integrated Circuit Design* Horowitz and Hill, *The Art of Electronics*
Grading	Homework & labs 25% Midterms (2) 10+15% Project 25% Final 25%
Homework	Collaboration is encouraged; copying is not. Explaining how you solved a problem to someone is fine; handing them your solutions is not. Helping someone debug their schematic or circuit is fine; giving them your schematic is not. Write your own answers and draw your own schematics without staring at someone else's.
Project	

Schedule

Week	Lectures by Date	Topic	HW & labs	Reading (GHLM)
1	1/20 1/22	Introduction: what is 140 all about; Op-amps circuits	hw1 solutions Lab1 lab files	Page xiv symbol conventions; 1.5, 1.6 MOS large & small signal models; skim chapter 3
2	1/25 1/27 1/29	Taylor, Heaviside, and Bode diode, BJT, & MOS physics MOS small signal model(s)	hw2 solutions RoI chart pdf pptx	1.2

3	2/1 2/3 2/5	Common source single pole amplifiers frequency and step response	Lab2: Cadence hw3 solutions	7.1, 7.2.1 up through eqn. 7.27 3.1, 3.2, 3.3.2
4	2/8 2/10 2/12	CS; input pole Input capacitance Active load, body effect	hw4 self-grading	3.3.5 (eqns. 3.55 and 66) 3.4.2.2 (eqns 3.126, 127, 128) Figure 4.17
5	2/15 2/17 2/19	Presidents Day. no classes Common gate; Review Midterm I – 1 page notes, 2 sides	sp08 mid1 solutions fa09 mid1 solutions sp15 mid1	Frequency response notes
6	2/22 2/24 2/26	Current mirrors Differential pair Differential amplifier	hw5 hw5soln hw5soln2	3.5.{3,4,5} MOS diff pair (eqns. 161, 171..174, 188, 189, 191, 199, 201; Fig 3.51) 4.2.2.2 MOS current mirror (eqns 17..20) 4.3.1, 4.3.5.2 Active loads (eqns 143, 149)
7	2/29 3/2 3/4	2 stage op-amp common mode and differential gain input/output swing	hw6 hw6soln hw6soln2 hw6solnP2 hw6solnk2-w	6 read 6.1.1, skim through eqn 6.25 6.3 through 6.3.5 inclusive 8 through 8.2 inclusive 9.1,2
8	3/7 3/9 3/11	2 stage op-amp feedback, stability frequency response	Miller compensation figures Lab4 hw7 hw7pts hw7soln2	9.3 through 9.4.3 inclusive
9	3/14 3/16 3/18	Miller compensation and pole splitting Current mirror pole/zero doublet; RHP zero from C_c Supply-independent biasing	hw8 hw8soln2	4.4.2, 4.4.3 biasing; with emphasis on the MOS parts
	3/21-25	SPRING BREAK! Pray for snow.	SNOW	SNOW
10	3/28 3/30 4/1	Supply-independent biasing midterm review Midterm II – Extended class period: 1:10–2:30 for the exam	sp08 mid2 sp15 mid2 FC like problem 2 will not be on your exam midterm2 solutions	
11	4/4 4/6 4/8	Folded cascode Switched capacitors ADCs and DACS	Final Project Lab5 hw9	6.1.7.1 Switched capacitor amplifier 6.6 folded cascode Wikipedia: ADC, SAR ADC
12	4/11 4/13 4/15	Folded cascode biasing Switched capacitors: ADC, PGA MOS switch	hw10	4.2.5.2 high swing current mirrors
13	4/18 4/20	Switched capacitors Presenting results; const-gm		

	4/22	biasing		
14	4/25 4/27 4/29	rail-to-rail input and output Ri, Ro, and feedback noise		
15	5/2 5/4 5/6	RRR week.  Project presentations.		

- Final Exam: Tuesday, May 10, 8-11 AM