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Course Syllabus

Contact Information

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Course Description

This course is an introduction to digital circuit and system design. The material provides a top-down view of the VLSI system design. The underlying CMOS devices and manufacturing technology are introduced, but quickly abstracted into higher-level to focus the class on design of larger digital modules both in FPGA design environment and in ASIC design environment. Verilog hardware description language will be covered and used in class for digital design. Basic digital system design concepts, boolean operations/combinational logic, sequential elements and finite-state-machines, will be described. Design of larger building blocks such as adders, multipliers, crossbars, I/O, as well as memory design (SRAM, Caches, FIFOs) and integration will be covered. Parallelism and pipelining micro-architectural concepts will be introduced. A number of physical design issues visible at the architecture level will be covered as well, such as interconnects, power, reliability.

The class includes getting familiar with industrial design automation and verification tools, and using them in assignments, labs and projects.

EECS 151/251A LB labs will focus on design flow in the FPGA environment and preparation for a big system design on the FPGA.

EECS 151/251A LA labs labs and project will exercise the full digital chip design flow in 28nm CMOS process (synthesis, floor-planing, SRAM integration, place-and-route tools, post-layout extraction, design-rule and layout vs. schematics checks and verification). The labs will be centered around a big digital design and focused on learning how to use the tools to design the chips as well as quickly explore the chip design space.

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Textbooks

- **Required:**
  - *Digital Design and Computer Architecture*, by Haris & Haris
  - *Digital Integrated Circuits, by Rabaey, Chandrakasan, Nikolic*
- ***Recommended References:***
  - *Digital VLSI Chip Design with Cadence and Synopsys CAD Tools, Erik Brunvand*

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Software and Labs

Laboratory exercises are an essential component in getting acquainted with the various design tools used in this class.

Lab sections will meet in 125 Cory. Outside of the lab sections, you can visit the lab if any open computers are available or log-in remotely.

1. Compute Server Access.

Most of the tools used in the course will be run on our compute servers. For more information on how to get access to those servers, how to set up your environment, and how to run the tools, please refer to the following document **(Compute Server Access and General Information)** **(https://bcourses.berkeley.edu/courses/1378447/files/60091514/download?wrap=1)** **(https://bcourses.berkeley.edu/courses/1378447/files/60091514/download?wrap=1)** .

- Note: To access the 77400-* Linux servers using NoMachine, you need to download the following **key file** **(https://bcourses.berkeley.edu/courses/1378447/files/60091515/download?wrap=1)** **(https://bcourses.berkeley.edu/courses/1378447/files/60091515/download?wrap=1)** .

2. Tool manuals and instructions.

The design tools you will use during the semester has been made available by the EDA major vendors **for sole use in this course**. The are not to be employed for any other purpose. In addition, **all information provided in the form of manuals and tutorials is protected**, and should not be shared or disseminated to anyone else. We truly appreciate your collaboration on this. Please refrain from posting your lab and project scripts and code on public repositories (e.g. gitHub) as these scripts contain confidential EDA vendor information. We will be checking this.

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Office Hours, Discussion and Lab Sessions

Office Hour times:

FPGA:

Prof. John Wawrzynek Tue 11am-12pm, Soda 631

GSI: James Martin TBD, Cory 125

ASIC:

Prof. Vladimir Stojanovic Thu 10-11am, Cory 513

GSI: Katerina Papadopoulou TBD, Cory 125

GSI: John Wright Tue 3pm-9pm, Cory 125

Discussion Session times:

Discussion sessions are supplementary to lectures. They will discuss sample practice problems, pset issues and provide a bridge between the lectures and lab material.

W 3-4P (3109 Etcheverry)
W 4-5P (3107 Etcheverry)
F 2-3P (521 Cory)

Lab Session times:

All labs will take place in 125 Cory.

FPGA (LB) - W 5:30-8:30pm, TBD
ASIC (LA) - Tu 3-6pm, Tu 6-9pm

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Grading Policies

Course grades will be assigned according to the following tentative grading formula:

Lecture:
(a) Problem Sets (10%)
(b) Midterm 1 (20%)
(c) Midterm 2 (20%)
(d) Final Exam (50%)

FPGA Lab (LB):
(a) Labs (25%)
(b) Project (75%)

ASIC Lab (LA):
(a) Labs (37.5%)
(b) Project (62.5%)

Letter grades will be assigned based approximately on the following scale:

98 - 100: A+	91 - 98: A	89 - 91: A-
87 - 89: B+	80 - 87: B	78 - 80: B-
76 - 78: C+	69 - 76: C	67 - 69: C-
65 - 67: D+	58 - 65: D	56 - 58: D-
	< 56: F	

Reading and Video Assignments:

Reading and video assignments include sections of the required textbook, distributed readings, supplementary notes and video materials. Reading and video assignments are indicated on Module Overview pages, and will also be included in homework assignments where appropriate. Supplementary notes will be provided for topics where lecture coverage is substantially different from the textbook. Students are responsible for all material in the reading. In particular, the scope of coverage for problem sets, quizzes, the design project, and the final examination includes the reading assignments as well as lecture material.

Problem Sets:

There will be a number of problem sets assigned over the course of the semester, approximately one per week. Electronic versions of your completed problem sets must be turned in online by the due date assigned. Late assignments will not be accepted. Solutions will be posted on the Modules page.

You are encouraged to discuss problems with other students in the class, the course facilitator and/or the Professor. However, the work which you submit for grading must be your own.

Labs:

There will be 7 ASIC labs and 6 FPGA labs to complete, during the first half of the semester. Use the **Lab Information** (https://bcourses.berkeley.edu/courses/1378447/pages/lab-information) page as your resource for all project materials and information.

Course Project:

There will be 3 phases of a course project to complete during the second half of the semester. The project will bring together the skills developed in the labs as well as the topics covered in lecture. Use the Course Project page as your resource for all project materials and information.

Midterm Exams:

The first midterm exam will cover Modules 1-6 and will be held in class on October 13, 2015. The second midterm exam will cover Modules 7-10 and will be held in class on November 12, 2015.

Final Exam:

The final exam will be comprehensive, covering all of the material in the course. The exam will be closed book, though notes will be allowed. Students will not be allowed to use a calculator. Final will be on Wed Dec 18, 8-11am.

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Date	Details	
Fri Dec 5, 2014	**ASIC Project** (https://bcourses.berkeley.edu/courses/1378447/assignments/6702866)	5pm
Fri Sep 11, 2015	**Homework 1** (https://bcourses.berkeley.edu/courses/1378447/assignments/6702843)	5pm
Fri Sep 18, 2015	**Homework 2** (https://bcourses.berkeley.edu/courses/1378447/assignments/6702845)	5pm
Fri Sep 25, 2015	**Homework 3** (https://bcourses.berkeley.edu/courses/1378447/assignments/6861384)	5pm
Fri Oct 2, 2015	**Homework 4** (https://bcourses.berkeley.edu/courses/1378447/assignments/6883081)	5:01pm
Fri Oct 9, 2015	**Homework 5** (https://bcourses.berkeley.edu/courses/1378447/assignments/6906643)	5:01pm
Tue Oct 13, 2015	**Midterm 1** (https://bcourses.berkeley.edu/calendar?event_id=1791987&include_contexts=course_1378447)	12am
Fri Oct 23, 2015	**Homework 6** (https://bcourses.berkeley.edu/courses/1378447/assignments/6940878)	5:01pm
Fri Oct 30, 2015	**Homework 7** (https://bcourses.berkeley.edu/courses/1378447/assignments/6966050)	5:01pm
Thu Nov 12, 2015	**Midterm 2** (https://bcourses.berkeley.edu/calendar?event_id=1791988&include_contexts=course_1378447)	12am
Wed Dec 9, 2015	**FPGA Final Project** (https://bcourses.berkeley.edu/courses/1378447/assignments/6702860)	7pm

	ASIC Lab 1 - Getting Around the Compute Environment (https://bcourses.berkeley.edu/courses/1378447/assignments/6702840)
	ASIC Lab 2 - Verilog Simulation (https://bcourses.berkeley.edu/courses/1378447/assignments/6702844)
	ASIC Lab 3 - Synthesis (https://bcourses.berkeley.edu/courses/1378447/assignments/6702847)
	ASIC Lab 4 - Floorplanning, Placement and Power Routing (https://bcourses.berkeley.edu/courses/1378447/assignments/6702851)
	ASIC Lab 5 - CTS and Routing (https://bcourses.berkeley.edu/courses/1378447/assignments/6702855)
	ASIC Lab 6 - Power and Timing (https://bcourses.berkeley.edu/courses/1378447/assignments/6702859)
	ASIC Lab 7 - SRAM (https://bcourses.berkeley.edu/courses/1378447/assignments/6702861)
	FPGA Lab 1 - Introduction to the FPGA Development Board (https://bcourses.berkeley.edu/courses/1378447/assignments/6702841)
	FPGA Lab 2 - FPGA Physical Layout (https://bcourses.berkeley.edu/courses/1378447/assignments/6702842)
	FPGA Lab 3 - Verilog Synthesis and FSM's (https://bcourses.berkeley.edu/courses/1378447/assignments/6702846)
	FPGA Lab 4: Simulation and Testing (https://bcourses.berkeley.edu/courses/1378447/assignments/6702850)
	FPGA Lab 5: List Processor and Chipscope (https://bcourses.berkeley.edu/courses/1378447/assignments/6702852)
	FPGA Lab 6: Serial I/O (https://bcourses.berkeley.edu/courses/1378447/assignments/6702858)
	Homework 8: EE 241A (https://bcourses.berkeley.edu/courses/1378447/assignments/6702870)
	Midterm 1 (https://bcourses.berkeley.edu/courses/1378447/assignments/6716468)