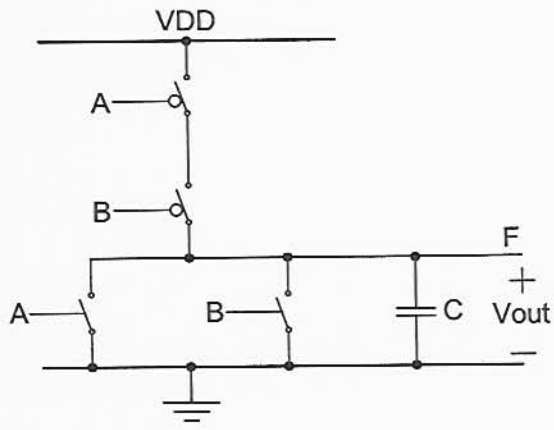
Problem 1 [10 points]

Shown below is a logic gate. Transistors are represented as switches which can be modeled as an ideal open circuit (no current flowing) when the switch is off, and a resistor of value R when the switch is on. When the input changes from A=0, B=1 to A=0, B=0, the output F of the gate transitions from logic 0 to logic 1. Because of the finite switch on-resistance R and load capacitance C (e.g. from wiring) this transition is not instantaneous. In practice this effect sets the maximum operating frequency of digital circuits.



Derive an algebraic expression for the time Δt it takes for V_{out} to transition from 0V to $V_{dd}\left(1 - {}^{1}/_{e}\right)$(constant $e \approx 2.718$).

Hint: Draw equivalent circuits for the two different input conditions and find an expression for $V_{out}(t)$.

$\Delta t =$ $2RC$

$V_{OUT} = V_{DD}\left(1 - e^{-t/\tau}\right)$

$\tau = 2RC$

Solve for t

$-t/\tau = \ln\left(1 - \frac{V_{OUT}}{V_{DD}}\right)$

$t = -\tau \ln\left(1 - \frac{V_{OUT}}{V_{DD}}\right)$

$t = -\tau \ln\left(1 - \frac{V_{DD} - V_{DD}/e}{V_{DD}}\right) = -\tau \ln(1/e)$

$= \tau = 2RC$

$= \tau = 2RC$

Problem 2 [10 points]

Microprocessors consist of a large number of (appropriately connected) logic gates. The output of each gate is connected to a capacitor C (resulting e.g. from wiring). The capacitor charges through a transistor (which can be treated as a resistor) from 0V to VDD each time the output of the gate transitions from logic 0 to logic 1 and is discharged when the output goes back to logic 0. This charging and discharging happens at a fraction of the clock frequency fclk of the microprocessor and is responsible for power dissipation.

Determine the numeric factors by with the microprocessor power dissipation changes if

a) The clock rate fclk is doubled.
b) The supply voltage VDD is cut in half.
c) The capacitance C is cut in half (e.g. by fabricating the microprocessor in a new technology with smaller features).

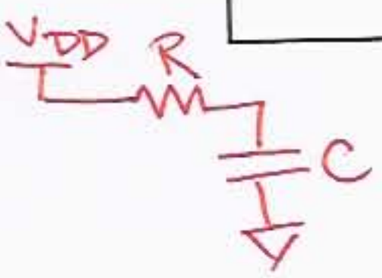
Hint: Derive first an expression for the energy delivered from the source to charge the capacitor and then relate this to power dissipation. Assume that the logic gate switches state at the same rate as the clock frequency, and that the capacitor charges fully to VDD (that is that $1/f_{clk} = T_{clk} \gg \tau$).

Show your work!

c) $\frac{P(2f_{clk})}{P(f_{clk})} =$ 2

b) $\frac{P\left(\frac{V_{DD}}{2}\right)}{P(V_{DD})} =$ 1/4

a) $\frac{P\left(\frac{C}{2}\right)}{P(C)} =$ 1/2



$P = I \cdot V \qquad I = \frac{V_{DD} - V_C}{R} \qquad V_C = V_{DD}(1 - e^{-t/RC})$

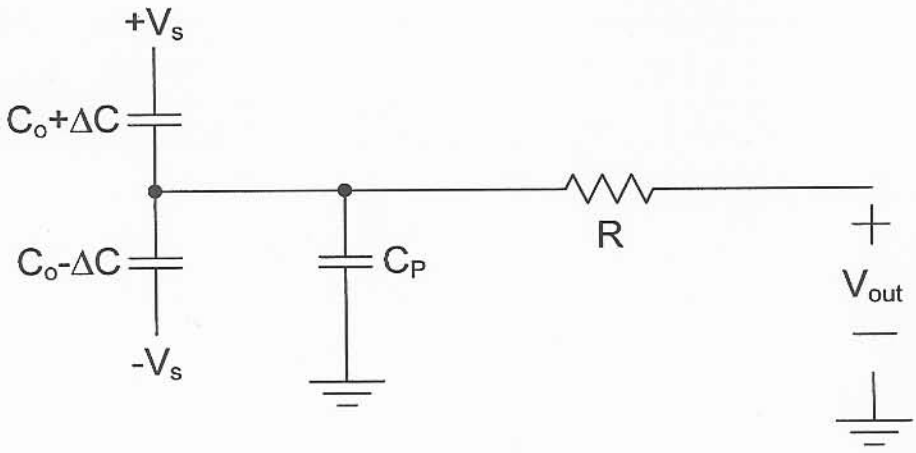
$I = \frac{V_{DD} - V_{DD} + V_{DD} e^{-t/RC}}{R} = \frac{V_{DD}}{R} e^{-t/RC}$

$E = \int_0^\infty P\,dt = \int_0^\infty \frac{V_{DD}^2}{R} e^{-t/RC}\,dt = CV_{DD}^2$

$P = E \cdot f_{clk} = CV_{DD}^2 f_{clk}$

Problem 3 [10 points]

In the circuit below $\Delta C = Ka$ represents the output of a capacitive accelerometer with input a. K is a constant that depends on the mechanical design of the accelerometer and C_P is a parasitic capacitance (e.g. from wiring) and ideally zero. Noise from the resistor R (e.g. due to wiring or other circuits not shown) limits the SNR of V_{out}.



By how many dB is the SNR of V_{out} changing when the parasitic capacitance increases from an ideal C_P=0F to a more practical C_P=C_o?

Hint: derive first an expression for the SNR of V_{out}. Show your work!

$\Delta SNR = 10 \cdot \log_{10} 4/9 = -3.5\,dB$ dB

$V_{out} = \frac{2V_S \Delta C}{2C_o + C_P}$ (VOLTAGE DIVIDER)

$\overline{V_n^2} = 4kTR\Delta f$

$P_{SIG} = \frac{V_{out}^2}{R_L} = \frac{4V_S^2 \Delta C}{(2C_o+C_P)^2} \cdot \frac{1}{R_L}$

$P_{NOISE} = \frac{\overline{V_n^2}}{R_L} = \frac{4kTR\Delta f}{R_L}$

$SNR = \frac{P_{SIG}}{P_{NOISE}} = \frac{4V_S^2 \Delta C}{(2C_o+C_P)^2} \cdot \frac{1}{4kTR}$

$\frac{SNR|_{C_P=C_o}}{SNR|_{C_P=0}} = \left(\frac{2C_o}{3C_o}\right)^2 = \frac{4}{9}$

Problem 4 [10 points]

Find a Boolean expression for a circuit with 3 binary inputs A, B, C and output F that is logic 1 if exactly 2 of the inputs are logic 1. Use the notation $\overline{X}$ for logic inversion.

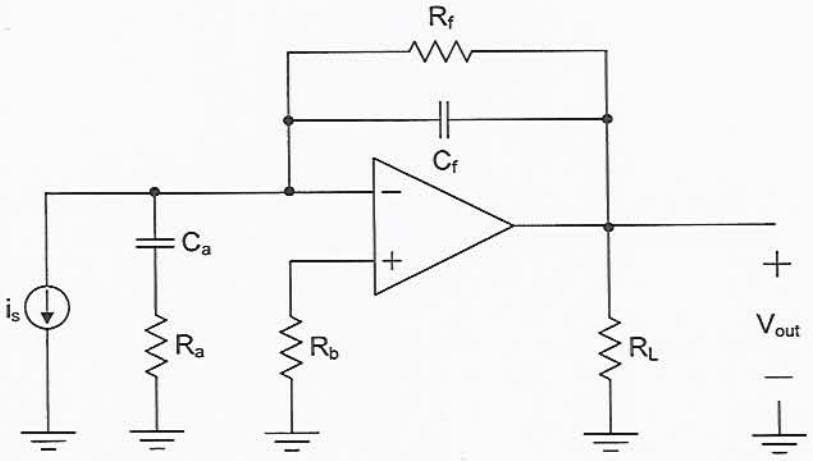
Do not attempt to simplify the Boolean expression for F.

F = $\overline{A}BC + A\overline{B}C + AB\overline{C}$

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Problem 5 [10 points]

Fiberoptic receivers use diodes that produce an output current i_s proportional to the incident light. Find the transfer function $H(s) = \frac{V_{out}(s)}{i_s(s)}$ of the receiver circuit shown in the diagram below.



Hint: check the unit of your result.

$$H(s) = \frac{V_{out}(s)}{i_s(s)} = \frac{R_F}{1+sR_FC_F}\ \Omega$$

$V_+ = V_- = 0$

All of I_s flows through feedback network R_F.

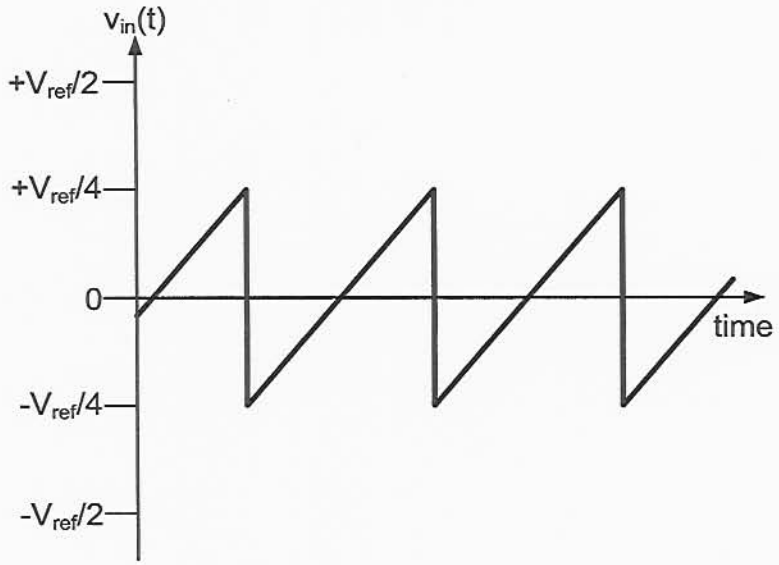
$$Z_F = \frac{R_F}{1+sR_FC_F}$$

$$V_{OUT} = I_s \cdot Z_F$$

Problem 6 [10 points]

The periodic analog signal $v_{in}(t)$ (period T) shown below is converted to a digital representation with a 10-Bit ADC. Derive an expression for the SNR in dB at the output of the ADC. The full-scale input range of the ADC is $\pm V_{ref}/2$.

Hint: find first an expression for the rms power of $v_{in}(t)$.



SNR = $10 \cdot \log_{10}(2^{18})$ dB

$V_{in} = \frac{V_{ref}}{4} \cdot \frac{t}{T}$

$V_{rms}^2 = \frac{1}{T}\int_0^T \frac{V_{ref}^2}{16}\frac{t^2}{T^2}\,dt = \frac{V_{ref}^2 t^3}{3 \cdot 16 \cdot T^3} = \frac{V_{ref}^2}{3 \cdot 16}$

$P_{SIG} = \frac{V_{rms}^2}{R_L}$ $\qquad P_{NOISE} = \frac{\Delta^2}{12 \cdot R_L} = \frac{\left(\frac{V_{ref}}{2^{10}-1}\right)^2}{12 \cdot R_L}$

$SNR = \frac{P_{SIG}}{P_{NOISE}} = \frac{V_{ref}^2}{3 \cdot 16 \cdot R_L} \cdot \frac{12 R_L (2^{10}-1)^2}{V_{ref}^2} = \frac{(2^{10}-1)^2}{4} \approx 2^{18}$

Problem 7 [10 points]

Measurements of the frequency response of an Ethernet cable and receiver circuit indicate a zero represented by

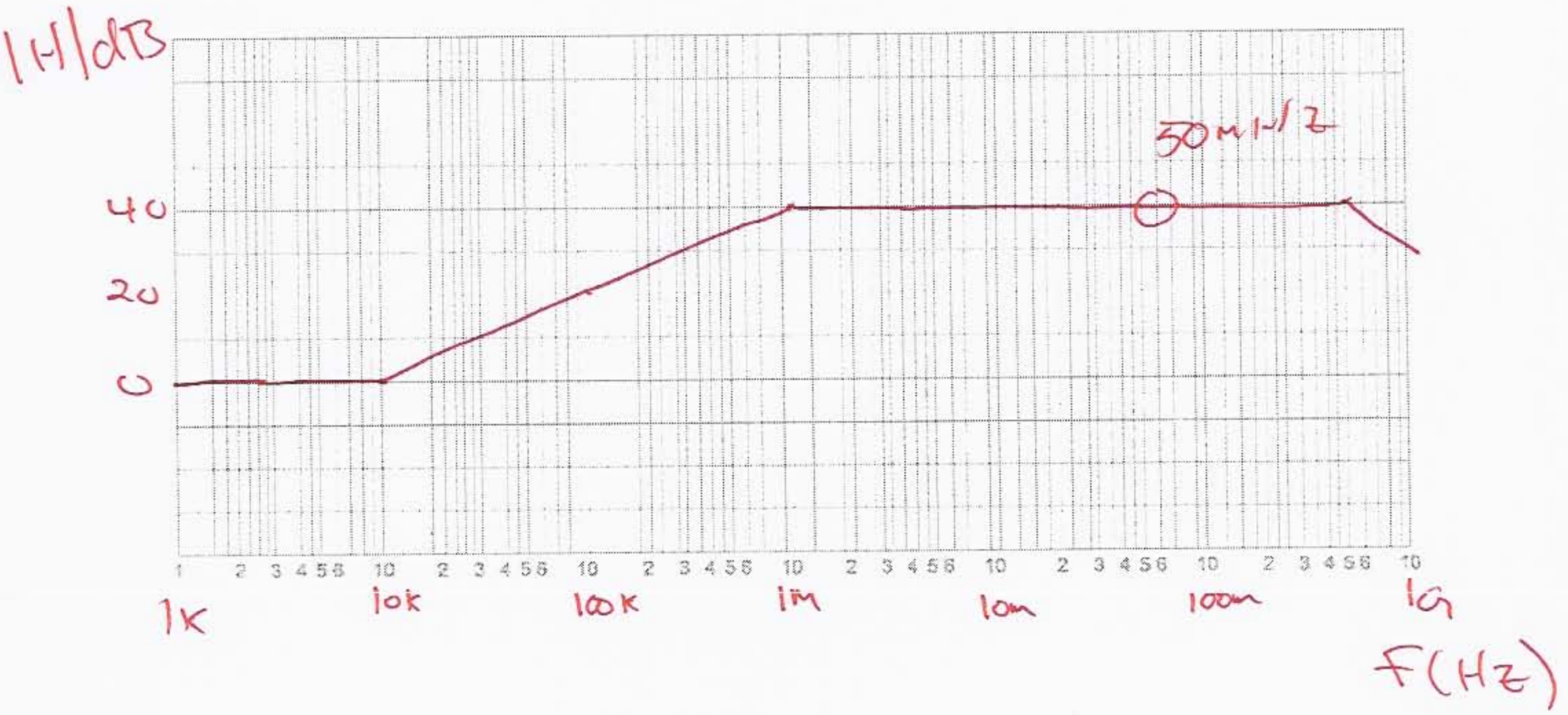
$$\frac{s}{2\pi(1\text{kHz})}$$

and poles and zeros at

$$p_1 = -2\pi(1\text{kHz})$$
$$z_2 = -2\pi(10\text{kHz})$$
$$p_3 = -2\pi(1\text{MHz})$$
$$p_4 = -2\pi(500\text{MHz})$$

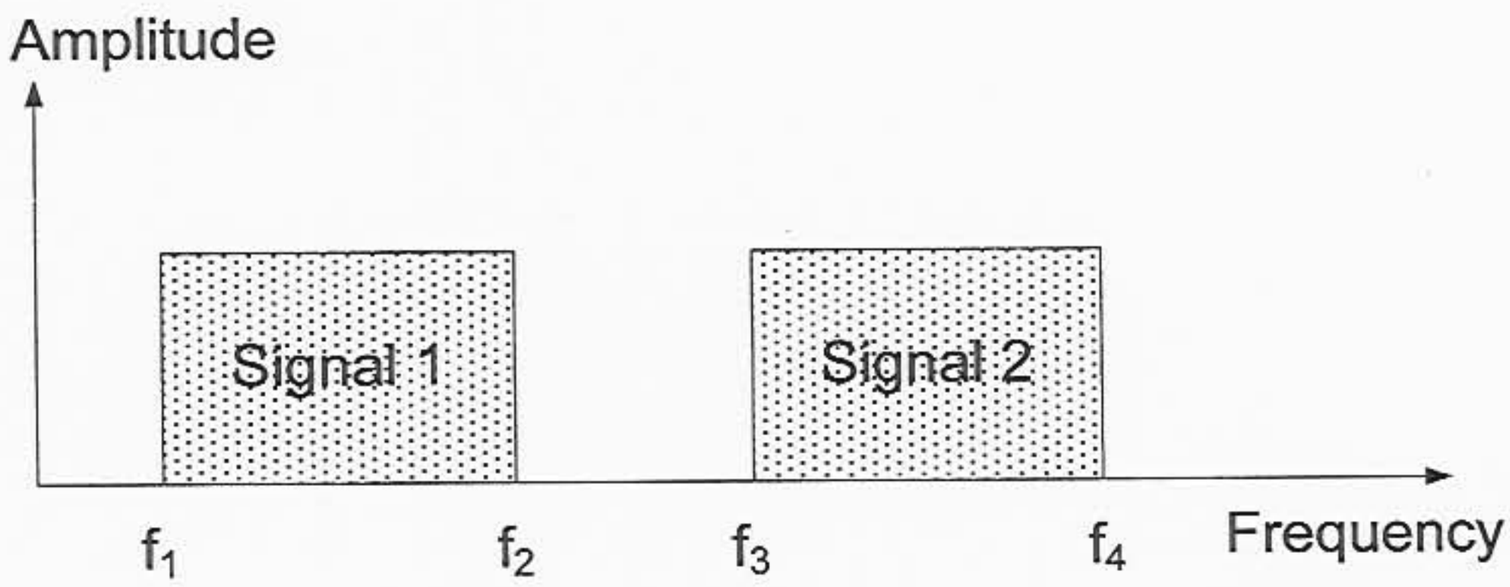
By how many dB is a sinusoidal signal with $f = 50\text{MHz}$ attenuated (negative sign) or amplified (positive sign)? Use the piecewise straight line approximation of the Bode plot to estimate your answer (the error compared to the correct result is small). Show your work.

$\Delta G =$ +40 dB



Problem 8 [10 points]

Often it is advantageous to transmit more than one signal over a single wire. One approach, illustrated below, separates different signals by frequency ("frequency division multiplexing"). Signal 1 occupies frequencies from f_1 to f_2 and signal 2 occupies frequencies from f_3 to f_4. The receiver recovers the individual signals with appropriately designed filters. This approach is used for example in cable networks to distribute hundreds of video channels over a single cable.



A condition for this to work is that the signals are bandlimited. Signal 1, for example, must not contain energy at frequencies higher than f_3 to avoid corrupting signal 2. This is accomplished by passing signal 1 through a filter $H(s)$. Assuming this filter has a frequency response

$$H(s) = \frac{1}{1 - \frac{s}{2\pi f_2}}$$

For f_2 = 10kHz, find the value of frequency f_3 that results in 32dB attenuation at f_3. Explain.

$f_3 =$ 400 kHz Hz

$20 \cdot \log_{10}(0.1) = -20\,dB$

$20 \cdot \log_{10}(1/2) = -6\,dB$

$-20 - 6 - 6 = -32\,dB$

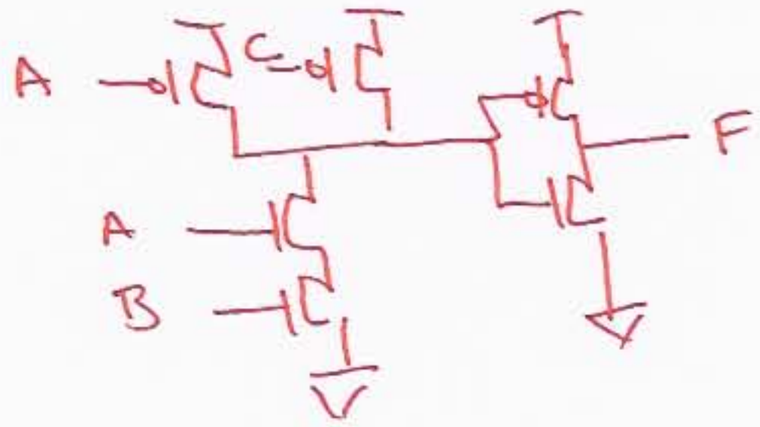
$\Rightarrow$ 1 decade + 2 octives.

$\Rightarrow$ 10kHz $\cdot 10 \cdot 2 \cdot 2 = 400$ kHz

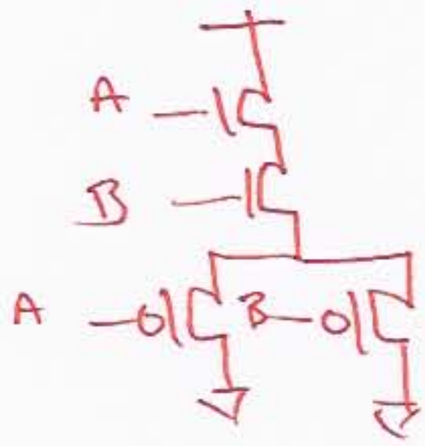
Problem 9 [10 points]

Using switches that turn on when the control signal is logic 1 or 0, respectively, synthesize a circuit that realizes a 2-input AND operation, i.e. $F = A \cdot B$. Draw the circuit in the box below and label the inputs A and B and the output F.

BEST SOLUTION (PMOS ON TOP, NMOS ON BOTTOM)



ALTERNATIVE (FULL CREDIT)



Problem 10 [10 points]

Fueled by Moore's law, which states that the number of transistors that can be fabricated on a chip doubles every two years, microprocessor performance has increased exponentially from 10^4 flops/s in the year 1980 to 10^8 flops/s in 2000. The unit flop/s stands for one floating point operation per second. Assuming continued exponential performance increases at the same rate, estimate microprocessor performance in flop/s in years ahead. Explain.

Year 2010: 10^{10}	flops/s

Year 2020: 10^{12}	flops/s

10^4 CHANGE IN 20 YEARS

$\Rightarrow 10^2$ CHANGE EVERY 10 YEARS

$10^8 \cdot 10^2 = 10^{10}$ IN 2010

2000 ↑ ↑ 10 YEARS