NAME ____

SID ______________________

UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
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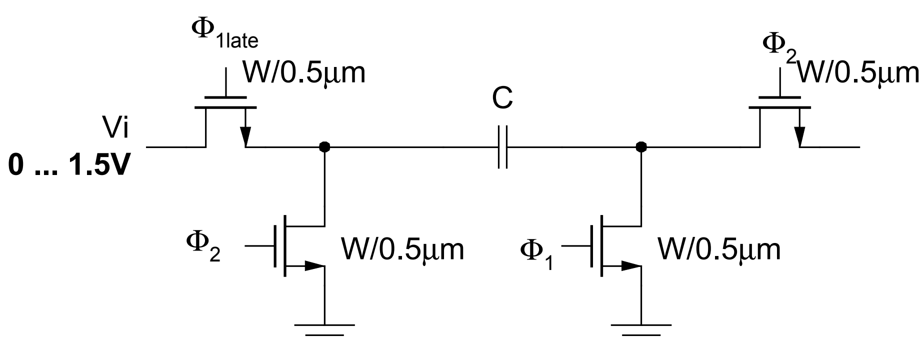
	Final Exam	**EECS 240**
B. E. BOSER	**May 21, 2002**	**SPRING 2002**

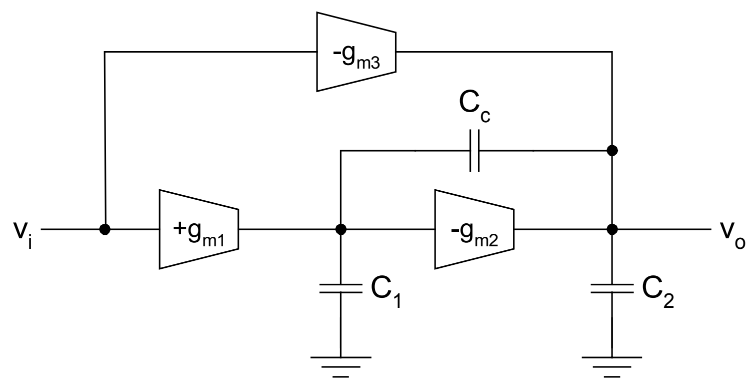
Show derivations and ***mark results*** *with box around them. Erase or cross-out erroneous attempts. Mark your name and SID at the top of the exam sheet.*

1. [25 points] MOS S/H
The circuit below operates from a two-phase non-overlapping 0V/3V clock. The switch Φ_{1late} opens shortly after the switch clocked with Φ_1.
   a) Calculate the maximum value of W for which the charge injected onto C results in a sampling error of less than 50mV. Assume fast gating and that the channel charge splits equally between source and drain.
   b) Assuming that the source V_i has zero output resistance and W=10μm (not the correct answer for a), what is the **worst-case** relative settling accuracy for t_{settle}=5ns (ignore charge injection)?

Parameter: V_{THN}=1V, $\mu_n C_{ox}$=200μA/V^2, C_{ox}=5fF/μm^2, C_{ol}'=0.2fF/μm, C=1pF. Assume square-law and ignore the body-effect.

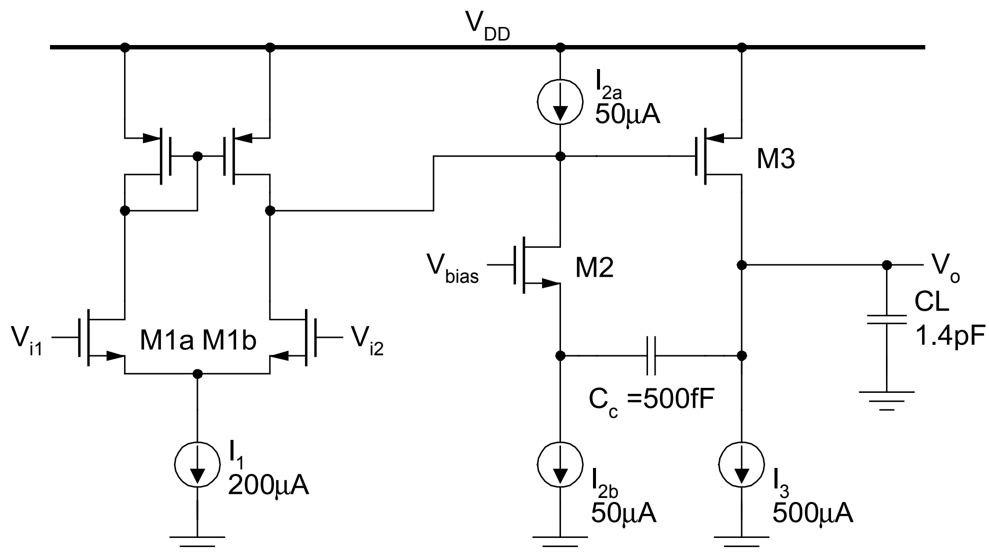


2. [25 points] The diagram below illustrates an alternative method for removing the feedforward zero arising from Miller compensation.
   a) Find the value of g_{m3} that moves the zero of $V_o(s)/V_i(s)$ to infinity as a function of g_{m1}, g_{m2}, C_1, C_2, and C_c. Simplify your result, but do not make assumptions regarding the relative value of component sizes.
   b) Compare this approach to using a nulling resistor. List key advantages or disadvantages of the proposed solution.



3. [25 points] For the amplifier below find
   a) The positive and negative slew-rate at the output.
   b) The input referred offset if I_{2a} and I_{2b} are mismatched by 10%; i.e. $I_{2a} - I_{2b} = 0.05(I_{2a} + I_{2b})$.

   Ignore all capacitors except those shown explicitly, transistor output impedance. g_{m1}=1mS, g_{m2}=5mS. M2 and M3 can source very large currents.



4. [25 points] Find a reasonably simplified analytical expression for the low-frequency CMRR of the circuit below as a function of

$$R_L = \frac{R_{L1} + R_{L2}}{2} \qquad R_S = \frac{R_{S1} + R_{S2}}{2} \qquad \text{and } R_x.$$

$$\Delta R_L = R_{L1} - R_{L2} \qquad \Delta R_S = R_{S1} - R_{S2}$$

Assume $G_m R_i \gg 1$ for i=L, S, X.
What is the fraction of amplifiers having CMRR=60dB or better?
Parameter: $g_{m1}=g_{m2}=1\text{mS}$, $R_S=10\text{k}\Omega$, $R_X=10\text{k}\Omega$, $R_L=100\text{k}\Omega$, $\sigma_{\Delta R/R}=0.12\%$.