University of California at Berkeley
College of Engineering
Dept. of Electrical Engineering and Computer Sciences

EE 105 Midterm I

Spring 2007 Prof. Ming C. Wu Feb. 22, 2007

Guidelines

- Open book and notes.
- The values of common parameters are listed at the beginning of next page.

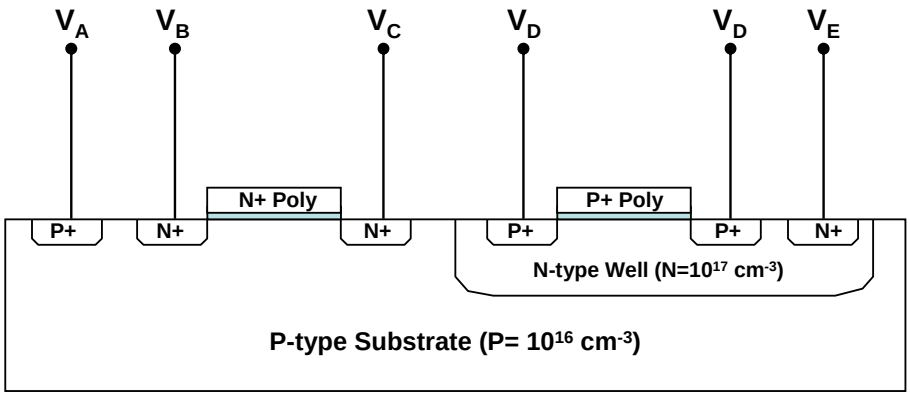
Please use the following parameters for all problems unless specified otherwise:

$\phi_{n+} = 550$ mV, $\phi_{p+} = -550$ mV, $V_{th} = 26$ mV
$\varepsilon_{Si} = 11.7$, $\varepsilon_{SiO2} = 3.9$, $\varepsilon_0 = 8.854\times10^{-14}$ F/cm,
$q = 1.6\text{x}10^{-19}$ C, $n_i = 10^{10}$ cm^{-3}.

(1) The figure below shows the schematic cross section of a CMOS device.

a) [5 pt] Please circle all the PN junctions in this CMOS device directly on the cross-sectional diagram in your answer sheets. How many PN junctions are there?

b) [5 pt] If the power supply voltages available for this CMOS are +2V and -2V, what voltage should be applied to V_A and V_E? Why?



(2) Consider a PN junction with both N and P doping concentration of 10^{16} cm^{-3}.

a) [5 pt] Find the built-in potential.

b) [5 pt] What is the depletion width at zero bias?

c) [5 pt] What is the maximum electric field at zero bias?

d) [5 pt] The PN junction is used as a varactor. If the bias voltage is varied from zero to 10V reverse bias, what is the capacitance tuning ratio (i.e., the ratio of maximum and minimum capacitance)

(3) Consider a PMOS capacitor with a p+ poly gate and a 1-nm-thick high-k gate dielectric whose relative dielectric constant is 20. The substrate doping is 10^{16} cm^{-3}.

a) [5 pt] Find the flat-band voltage.

b) [5 pt] Find the threshold voltage.

c) [10 pt] Find the charge distribution of the MOS capacitor (i.e., $\rho(x)$ vs x) when the gate is biased at 0V. Please be quantitative.

d) [5 pt] What is the total gate charge per unit area at the gate, channel, and body, respectively, when the gate is biased at 0V.

e) [5 pt] What is the total capacitance per unit area when the gate is biased at 0V?

(4) For the circuit shown below, W/L = 10 for both M_1 and M_2, $\mu_n C_{ox} = 100$ μA/V^2, $\mu_p C_{ox} = 50$ μA/V^2, $\lambda = 0.05$ V^{-1} for NMOS and 0.01 V^{-1} for PMOS, $V_{TH} = 1$V for NMOS and -1V for PMOS, $V_{DD} = 5$V.

a) [10 pt] Find the DC bias voltages, V_b and V_G, such that the bias current is 100 μA. Use $\lambda = 0$ for this part.
b) [5 pt] Find the small-signal parameters (i.e., g_m, r_0) corresponding to the condition in a).
c) [5 pt] What is the voltage gain of this amplifier, both symbolically and numerically?
d) [5 pt] What is the input and output resistance of this amplifier (both symbolically and numerically)?
e) [5 pt] What determines the output voltage swing? Find the maximum and the minimum output voltages.
f) [5 pt] How does the voltage gain and the output resistance change if the gate of M_1 is connected to the output directly (no V_b is applied)?
g) [5 pt] What is the DC value of the output voltage?