University of California at Berkeley
College of Engineering
Dept. of Electrical Engineering and Computer Sciences

EE 105 Midterm I

Spring 2006 Prof. Ming C. Wu Feb. 23, 2006

Guidelines

- Closed book and notes.
- One-page information sheet allowed.
- There are some useful formulas in the end of the exam.
- The values of common parameters are listed at the beginning of next page.

Please use the following parameters for all problems unless specified otherwise:
$\phi_{n+} = 550$ mV, $\phi_{p+} = -550$ mV, $V_{th} = 26$ mV
$\varepsilon_{Si} = 11.7$, $\varepsilon_{SiO2} = 3.9$, $\varepsilon_0 = 8.854\times10^{-14}$ F/cm,
$q = 1.6\text{x}10^{-19}$ C, $n_i = 10^{10}$ cm^{-3}.

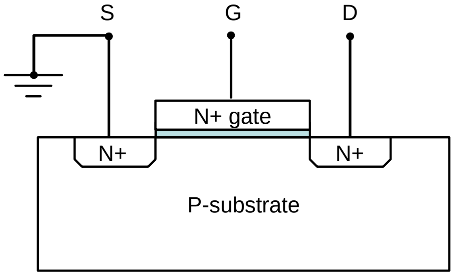
(1) Consider a silicon PN junction diode with an N-doping concentration of 10^{16} cm^{-3} and a P-doping concentration of 10^{18} cm^{-3}. Their cross-sectional area of the diode is 100 μm^2. Assume the reverse saturation current of the diode is 10^{-14} Amp. The diode is forward biased at 0.7V.
a) [10 pt] Find the dynamic resistance at this bias.
b) [10 pt] Find the depletion capacitance at this bias.

(2) Consider a MOS capacitor with a P+ polysilicon gate and an N-doped substrate with a doping concentration of 10^{16} cm^{-3}. The thickness of the oxide is 20 nm.
a) [10 pt] Find the threshold voltage.
b) [10 pt] Which mode is the MOS capacitor in when its gate is biased at 1 V?
c) [10 pt] What is the maximum capacitance per unit area?
d) [10 pt] What is the minimum capacitance per unit area?

(3) [10 pt] For the MOS capacitor in Problem (2), plot the charge density distribution as a function of position when the gate is biased at -2V. Please be as quantitative as possible. Show the positions of all charges, and show the magnitude and polarity of the charges.

(4) [10 pt] If the P+ gate of the MOS capacitor in Problem (2) is replaced by a metal whose electrostatic potential is 0V. What is the threshold voltage of the new MOS capacitor?

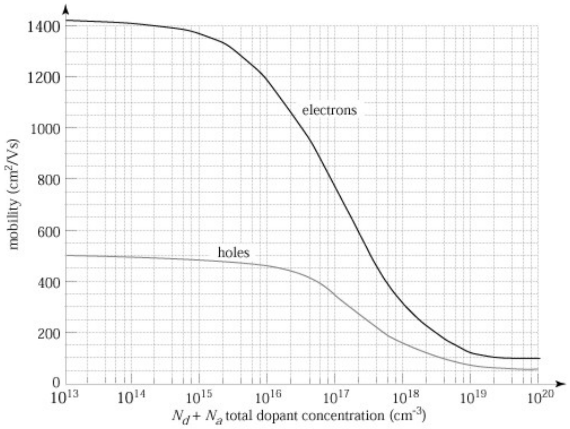
(5) Consider an N-MOSFET with an N+ polysilicon gate on P-type substrate ($N_a = 10^{17}$ cm^{-3}). The source is grounded, and the drain is biased at 5V. The transistor has a gate length of 1 μm, and a width of 10 μm. The thickness of gate oxide is 10 nm. For simplicity, assume the channel-length modulation parameter $\lambda = 0$.

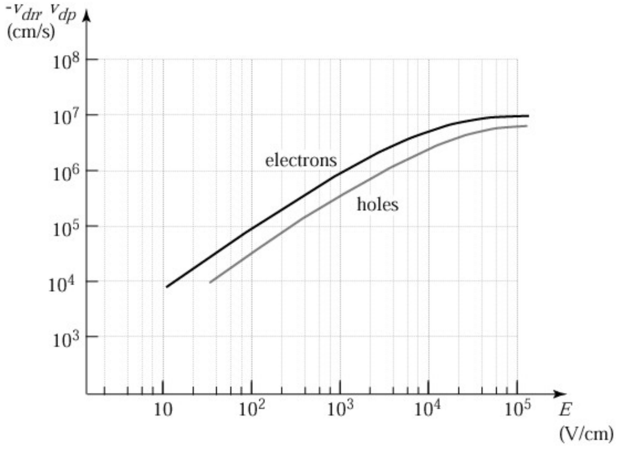


a) [10 pt] At what gate voltage does the transistor turn on, i.e., start to have significant current flowing between source and drain?
b) [10 pt] Find the drain current when the gate is biased at 2V.

Some equations

Mass-action law $n \times p = n_i^2(T)$





Resistivity: $\rho_n = \dfrac{1}{\sigma_n} = \dfrac{1}{q\mu_n N_{d,eff}}$

Resistance: $R = \dfrac{\rho L}{Wt} = \left(\dfrac{\rho}{t}\right)\left(\dfrac{L}{W}\right) = R_{sq}\left(\dfrac{L}{W}\right)$

Total current (e$^-$): $J = J_{drift} + J_{diff} = q\mu_n nE + qD_n \dfrac{dn}{dx}$

Gauss's law: $\oint E \cdot dS = \dfrac{Q}{\varepsilon}$ $\quad Q = CV \quad$ $E = -\dfrac{d\phi}{dx}$

Depletion layer: $X_{d0} = x_{p0} + x_{n0} = \sqrt{\dfrac{2\varepsilon_s \phi_{bi}}{q}\left(\dfrac{1}{N_a} + \dfrac{1}{N_d}\right)}$ $\quad X_d(V_D) = X_{d0}\sqrt{1 - \dfrac{V_D}{\phi_{bi}}}$

pn depletion layer capacitance: $C_j = \dfrac{qN_a x_{p0}}{2\phi_{bi}\sqrt{1 - \dfrac{V_D}{\phi_{bi}}}} = \dfrac{C_{j0}}{\sqrt{1 - \dfrac{V_D}{\phi_{bi}}}}$

pn diffusion current $J^{diff} = qn_i^2\left(\dfrac{D_p}{N_d W_n} + \dfrac{D_n}{N_a W_p}\right)\left(e^{\frac{qv_D}{kT}} - 1\right)$ $i_D = I_S\left(e^{\frac{qv_D}{kT}} - 1\right)$

Diffusion capacitance: $C_d = \dfrac{1}{2}\dfrac{qI_D}{kT}\tau$

Threshold voltage (NMOS)

$$V_{Tn} = V_{FB} - 2\phi_p + \frac{1}{C_{ox}}\sqrt{2q\varepsilon_s N_a\left(-2\phi_p\right)} \qquad \phi_p = -\frac{kT}{q}\ln\frac{N_a}{n_i}$$

$$V_{Tn} = V_{Tn0} + \gamma\left(\sqrt{V_{SB} - 2\phi_p} - \sqrt{-2\phi_p}\right)$$

NMOS equations:

$$I_D = 0, \quad \mathrm{V}_{GS} < V_{Tn}$$

$$i_D = \frac{W}{L}\mu C_{ox}\left(v_{GS} - V_{Tn} - \frac{v_{DS}}{2}\right)v_{DS}\left(1+\lambda V_{DS}\right), \quad V_{GS} > V_{Tn}, V_{DS} < V_{GS} - V_{Tn}$$

$$i_D = \frac{W}{L}\frac{\mu C_{ox}}{2}\left(v_{GS} - V_{Tn}\right)^2\left(1+\lambda V_{DS}\right), \quad V_{GS} > V_{Tn}, V_{DS} > V_{GS} - V_{Tn}$$

MOS capacitances in saturation $C_{gs} = (2/3)WLC_{ox} + C_{ov}$ $\qquad C_{ov} = L_D W C_{ox}$

MOS signal parameters:

$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{V_{GS},V_{DS}} = \mu C_{ox}\frac{W}{L}\left(V_{GS} - V_{Tn}\right)\left(1+\lambda V_{DS}\right) \approx \mu C_{ox}\frac{W}{L}\left(V_{GS} - V_{Tn}\right)$$

$$r_o = \left(\left.\frac{\partial i_D}{\partial v_{DS}}\right|_{V_{GS},V_{DS}}\right)^{-1} \approx \frac{1}{\lambda I_{DS}}$$

$$g_{mb} = \left.\frac{\partial i_D}{\partial v_{BS}}\right|_Q = \frac{\gamma g_m}{2\sqrt{-V_{BS} - 2\phi_p}}$$

EE 105 Midterm-1 Solution

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$q := 1.6\cdot10^{-19}$ $ni := 10^{10}$ $Vth := 0.026$

$\varepsilon0 := 8.854\cdot10^{-14}$ $\varepsilon s := 11.7\cdot\varepsilon0$ $\varepsilon ox := 3.9\cdot\varepsilon0$

$\mu m := 10^{-4}$ $nm := 10^{-7}$ $mV := 10^{-3}$

$\mu\_n := 1450$ cm2/V-sec

(1) (a) $Is := 10^{-14}$

$$Id(Vd) := Is\cdot\left(\exp\left(\frac{Vd}{Vth}\right)-1\right)$$

$Id(0.7) = 4.927\times10^{-3}$

$r\_d := \dfrac{Vth}{Id(0.7)}$ $r\_d = 5.278$ Ω

(b) $Nd := 10^{16}$ $Na := 10^{18}$ $Area := 100\cdot\mu m^{2}$

$\phi n := 60\cdot mV\cdot\log\left(\dfrac{Nd}{ni}\right)$ $\phi n = 0.36$

$\phi p := -60\cdot mV\cdot\log\left(\dfrac{Na}{ni}\right)$ $\phi p = -0.48$

$\phi b := \phi n - \phi p$ $\phi b = 0.84$

$xd(Vd) := \sqrt{\dfrac{2\cdot\varepsilon s\cdot(\phi b - Vd)}{q}\cdot\left(\dfrac{1}{Na}+\dfrac{1}{Nd}\right)}$ $xd(0.7) = 1.353\times10^{-5}$

$Cj := \dfrac{\varepsilon s}{xd(0.7)}\cdot Area$ $Cj = 7.656\times10^{-14}$ F

(2) $Nd := 10^{16}$ $tox := 20\cdot nm$

$\phi n := 60\cdot mV\cdot\log\left(\dfrac{Nd}{ni}\right)$ $\phi n = 0.36$

$\phi pp := -550\cdot mV$

$V\_FB := \phi n - \phi pp$ $V\_FB = 0.91$ V

(a) $Xd\_max := \sqrt{\dfrac{2\cdot\varepsilon s\cdot(2\cdot\phi n)}{q\cdot Nd}}$ $Xd\_max = 3.053\times10^{-5}$

$Qb\_max := q\cdot Nd\cdot Xd\_max$

$Cox := \dfrac{\varepsilon ox}{tox}$

$V\_Tp := V\_FB - 2\cdot\phi n - \dfrac{Qb\_max}{Cox}$ $V\_Tp = -0.093$

(b) 1V is greater than flatband voltage --> the MOS is in accumulation mode

(c) Maximum capacitance is simply Cox:

$\text{Cmax} := \text{Cox}$ $\qquad$ $\text{Cmax} = 1.727 \times 10^{-7}$ =/cm^2

(d) $\text{Cb\_min} := \dfrac{\varepsilon s}{\text{Xd\_max}}$

$\text{Cmin} := \dfrac{\text{Cox}\cdot\text{Cb\_min}}{\text{Cox} + \text{Cb\_min}}$ $\qquad$ $\text{Cmin} = 2.835 \times 10^{-8}$ F/cm^2

(3) -2V is more negative than threshold (-0.093V), so it is in inversion. The charge on the semiconductor side include a fixed donor charges from the semiconductor-oxide interface to the maximum depletion width, Xd_max and the inversion hole charges at the interface, Qp. The gate charge is equal to the total charge with opposite sign.

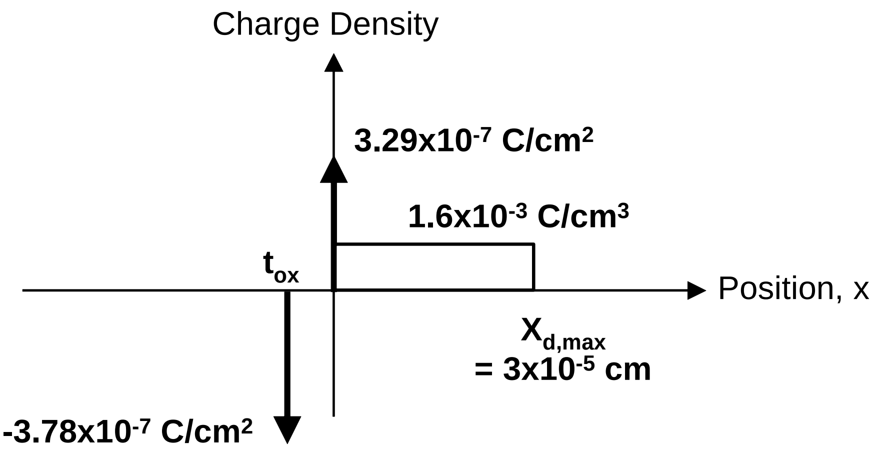
$\text{V\_GB} := -2$

$\text{Qp} := -\text{Cox}\cdot(\text{V\_GB} - \text{V\_Tp})$ $\qquad$ $\text{Qp} = 3.293 \times 10^{-7}$ C/cm^2

$\rho\text{\_b} := q\cdot\text{Nd}$ $\qquad$ $\rho\text{\_b} = 1.6 \times 10^{-3}$ C/cm^3

$\text{Qg} := -\text{Qp} - \rho\text{\_b}\cdot\text{Xd\_max}$ $\qquad$ $\text{Qg} = -3.781 \times 10^{-7}$ C/cm^2

$\text{Xd\_max} = 3.053 \times 10^{-5}$



(4) Flatband voltage and threshold voltage is shifted by the same amount:

$\phi m := 0$

$\text{V\_FB\_m} := \phi n - \phi m$ $\qquad$ $\text{V\_FB\_m} = 0.36$

$\Delta\text{V\_FB} := \text{V\_FB\_m} - \text{V\_FB}$ $\qquad$ $\Delta\text{V\_FB} = -0.55$

$\text{V\_Tp\_m} := \text{V\_Tp} + \Delta\text{V\_FB}$ $\qquad$ $\text{V\_Tp\_m} = -0.643$ V

(5) $Na := 10^{17}$ $tox := 10 \cdot nm$ $W := 10 \cdot \mu m$ $L := 1 \cdot \mu m$

$\phi p := -60 \cdot mV \cdot \log\left(\frac{Na}{ni}\right)$ $\phi p = -0.42$

$\phi nn := 550 \cdot mV$

$V\_FB := \phi p - \phi nn$ $V\_FB = -0.97$

$Xd\_max := \sqrt{\frac{2 \cdot \varepsilon s \cdot (-2 \cdot \phi p)}{q \cdot Na}}$ $Xd\_max = 1.043 \times 10^{-5}$

$Qb\_max := -q \cdot Na \cdot Xd\_max$

$Cox := \frac{\varepsilon ox}{tox}$

$V\_Tn := V\_FB - 2 \cdot \phi p - \frac{Qb\_max}{Cox}$ $V\_Tn = 0.353$

(a) The NMOS FET is turned on when the gate voltage is equal to the thresold voltage

$V\_Tn = 0.353$

(b) $V\_GS := 2$

$V\_DS := 5$

$V\_DS\_sat := V\_GS - V\_Tn$ $V\_DS\_sat = 1.647$

Since V_DS is greater than V_DS_sat, the FET is in saturation

$I\_DS(V) := \frac{W}{L} \cdot \frac{\mu\_n \cdot Cox}{2} \cdot (V\_GS - V\_Tn)^2$ $I\_DS(5) = 6.789 \times 10^{-3}$ Amp