UNIVERSITY OF CALIFORNIA
College of Engineering
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EECS 143 Professor Ali Javey

Fall 2008

Exam 1

Name: Answer Key

SID: 1337

Closed book. One sheet of notes is allowed.
There are a total of 13 pages on this exam, including the cover page.

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Physical Constants

Electronic charge	q	1.602×10^{-19} C
Permittivity of vacuum	ε_0	8.845×10^{-14} F cm^{-1}
Relative permittivity of silicon	$\varepsilon_{Si}/\varepsilon_0$	11.8
Boltzmann's constant	k	8.617×10^{-5} eV/ K or 1.38×10^{-23} J K^{-1}
Thermal voltage at T = 300K	kT/q	0.026 V
Effective density of states	N_c	2.8×10^{19} cm^{-3}
Effective density of states	N_v	1.04×10^{19} cm^{-3}

1. True/False (20 pts)

Circle either (T)rue or (F)alse (2 pts each)

a) HMDS is a type of photoresist that is sometimes used to enhance the resolution.
T / (F)

b) Arsenide (As) is an n-type dopant for Silicon.
(T) / F

c) Reactive Ion Etching does not etch most photoresists.
T / (F)

d) Proximity lithography causes more mask damage than contact lithography.
T / (F)

e) When diluting strong acids, add acids to water, not the other way around.
(T) / F

f) To create a thicker PR layer on the wafers, we can apply a larger volume of PR before spinning.
T / (F)

g) Piranha removes both organic AND metallic contaminants from the wafers.
(T) / F

h) Plastic beakers should be used for Piranha.
(T) / (F)
Credit was given for either answer. It depends on whether you consider Teflon to be a plastic.

i) Silicon can be used as either an acceptor or a donor for doping GaAs.
(T) / F

j) The intrinsic carrier concentration in Germanium is less than that of Silicon.
T / (F)

2. **Device Physics (25 pts)**

A silicon sample is doped with 10^{18} cm^{-3} phosphorous atoms. Assume that the sample is at thermal equilibrium and uniformly doped.

a) Is this semiconductor n-type or p-type? (1 pt)

Phosphorus atoms have an extra valence electron compared to Silicon, making it an n-type dopant.

b) What is the majority carrier concentration for this sample at room temperature? (1 pt)

Since the intrinsic concentration is only about 10^{10}, the majority carrier concentration is essentially the dopant concentration: 10^{18} cm^{-3}

c) What is the net charge of this Si sample? (1 pts)

A silicon sample at equilibrium has zero net charge.

d) Find the Fermi level (with respect to either E_c or E_v) for this semiconductor at room temperature. (3 pts)

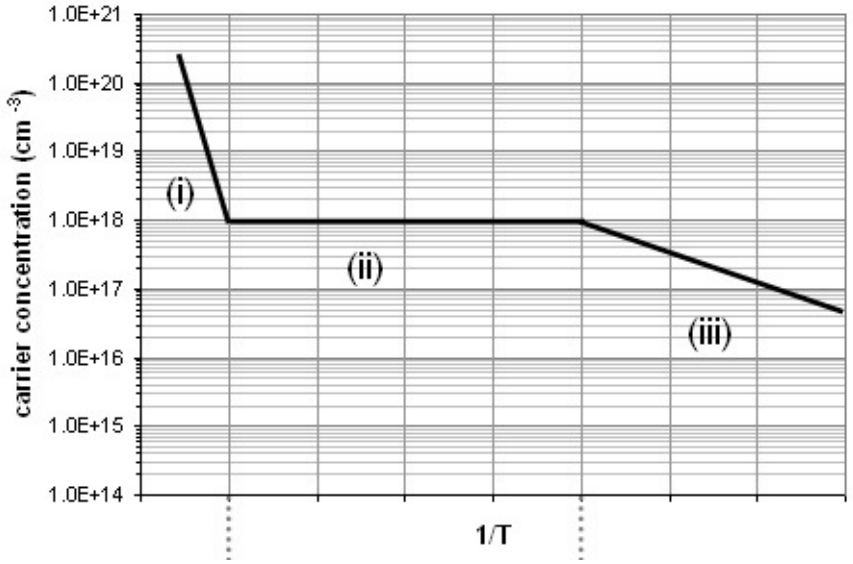
Recall: $n = N_c e^{-(E_c - E_F)/kT}$

$$E_C - E_f = -kT \cdot \ln\left(\frac{n}{N_C}\right) = -0.025eV \cdot \ln\left(\frac{10^{18}}{3.23 \cdot 10^{19}}\right) \cong 87meV$$

e) What is the definition of thermal equilibrium? (3 sentences max) (2 pts)

No external forces applied to sample (EM fields, mechanical stress). Thermal agitation leads to a constant average number of carriers per energy level.

f) The following figure shows the dependence of carrier concentration as a function of temperature for this sample. Three distinct regimes are evident. Concisely explain the physics that is taking place in each of these three labeled regimes (i, ii, and iii). (Hint: why do you observe this trend?) (6 pts)



(i) **Intrinsic region: Thermal generation of carriers overwhelms electrical doping.**

(ii) **Extrinsic region: Electrically active doping sets mobile carrier population.**

(iii) **Freeze-out region: Thermal energy is no longer sufficient to excite mobile carriers from all dopants.**

g) Historically, the first transistor was made with Ge, and yet Si has become the dominant semiconductor for IC processing over the past four decades. List 3 reasons why Si has become so successful. (3 pts)

Silicon is cheap and plentiful, and we know how to make it extremely pure. Its thermal oxide is electrically robust and reliable as an insulator. It has roughly symmetric electron and hole mobilities permitting CMOS integrated circuits. Also, it is easily doped. Sillicon wafers are also more mechanically robust than Germanium wafers. Sillicon is a non-toxic material, and is a better conductor of heat.

h) From the band theory point of view, what differentiates a semiconductor from an insulator? (2 sentences max) (2 pts)

Semiconductors have a bandgap of about 0.5 to 4 eV between their valence and conduction band. Insulators have a bandgap exceeding about 4 eV.

i) From the band theory point of view, what differentiates a metal from a semiconductor? (2 sentences max) (2pts)

A pure semiconductor has a Fermi level in the band gap. For a pure metal, the Fermi level is far into the conduction band, so there is no gap between occupied states and available states.

j) Briefly explain why crystalline Si, instead of amorphous Si, is used in IC processing as the main semiconductor material. (2 sentences max) (2pts)

Crystalline silicon enables much better transport of carriers since it is defect-free, leading to better circuit performance.

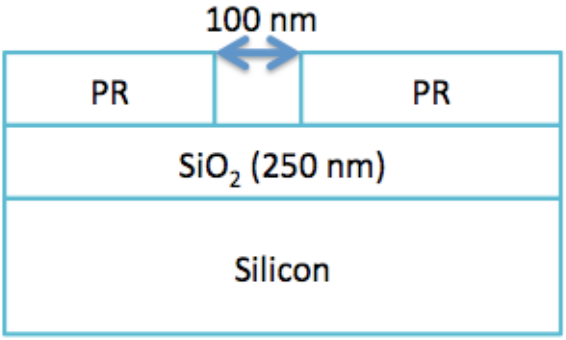
k) Gold is very much disliked in IC manufacturing. Briefly explain what problems gold contamination may cause. (2 sentences max) (2 pts)

Gold is a deep level trap. Therefore it results in high leakage currents and low carrier lifetimes.

3. **Etching I (20 pts)**

Assume 5:1 BOE (Buffered HF) etches SiO_2 isotropically at 100 nm/min.
RIE etches SiO_2 at 200 nm/min and has a SiO_2:Si selectivity of 15:1.

Assume a Si/SiO_2 substrate with patterned photoresist as shown below.



a) For the structure above, how long should this wafer be placed in 5:1 BOE etchant to record a 10% over-etch? (3 pts)

250 nm * 110% = 275 nm. 275 nm / 100 nm/min = 2.75 min

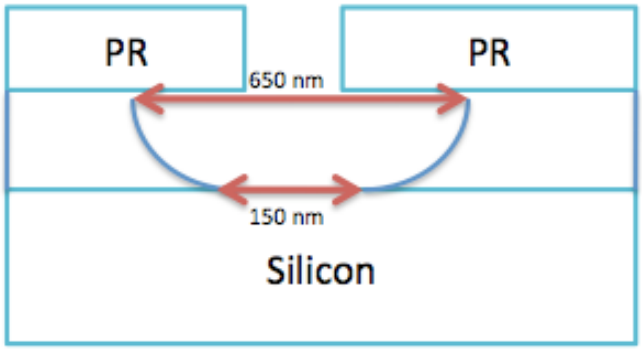
b) What is the width of SiO_2 removed at the top of the resulting trench (at the Photoresist/SiO_2 interface), and what is the width of SiO_2 removed at the bottom of the trench (at the SiO_2/Si interface) after the 10% over-etch? (3 pts)

Since HF is assumed to be completely isotropic, it etches 275 nm in all directions. Top of the trench = 275 + 100 gap + 275 = 650 nm

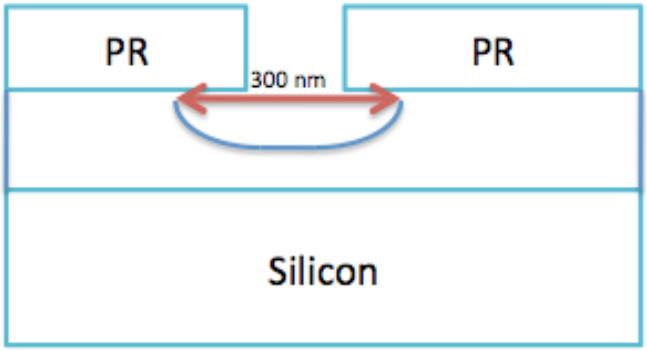
At 0% overetch, the bottom of the trench is 100 nm wide. 10% overetching results in 25 nm in both directions.

Bottom of the trench = 25 + 100 + 25 = 150 nm
Note: This is a simplified calculation. Vertical etching would broaden the bottom further.

c) Draw a schematic of the structure after 10% over-etch. (3 pts)



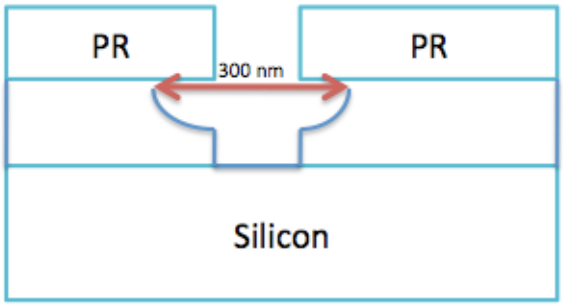
d) Now start over and once again assume the unetched structure given above. This time we do a 1 minute BOE etch. Draw a schematic of the etched structure. (3 pts)



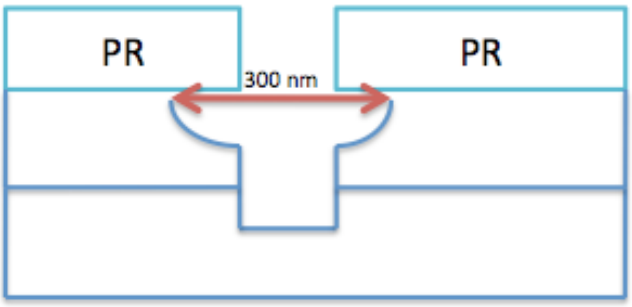
e) For the given RIE SiO_2 etch rate and selectivity, what is the etch rate of Si? (assume RIE etches SiO_2 at 200 nm/min and has a SiO_2:Si selectivity of 15:1.) (2 pts)

S = SiO2 / Si
15/1 = 200 / Si
Si = 13.33 nm / min

f) Now we take the wafer after part (d) and we do a completely anisotropic RIE dry etch of SiO_2 to fully pattern etch the oxide. Assume the PR is not attacked. Draw a schematic of the etched structure (0% over-etch). (3 pts)



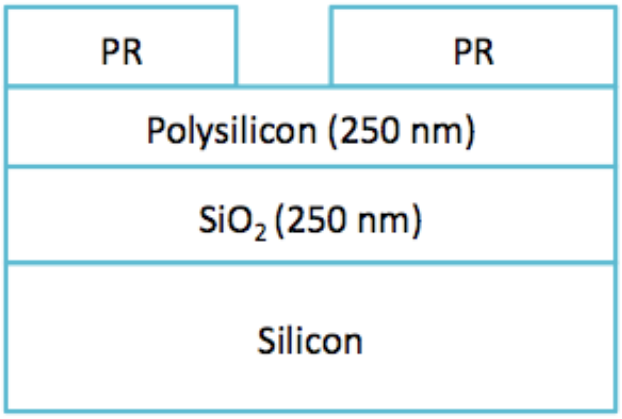
g) Suppose we instead take the wafer after (d) and do a completely anisotropic dry etch, but this time perform a 50% over-etch. Draw a schematic of the etched structure. (3 pts)



4. Etching II (12 pts)

Assume our RIE etches Si at an average rate of 25 nm/min.

Assume a Si/SiO_2/polysilicon substrate with patterned photoresist as shown below.



a) We decide to pattern etch the polysilicon layer. However, we find that after the polysilicon deposition, the thickness of poly varies by ± 10% over the wafer surface with an average film thickness of 250 nm. In addition, RIE etch rate varies by ± 5% across the wafer.

   Given the above information, what etch time should we use for successful patterned etching of the poly-Si layer across the entire wafer? (3 pts)

   The maximum thickness of poly is 250 * 1.1 = 275 nm. The worst case etch rate is 25*.95 = 23.75 nm /min. Thus, the minimum etch time is 11.58 minutes.

b) What are 5 parameters that control the selectivity of RIE? (3 pts)

   Plasma parameters, Plasma chemistry, Gas pressure, Gas flow, and Temperature

c) Briefly (3 sentences max) explain why RIE results in an anisotropic etch. (3 pts)

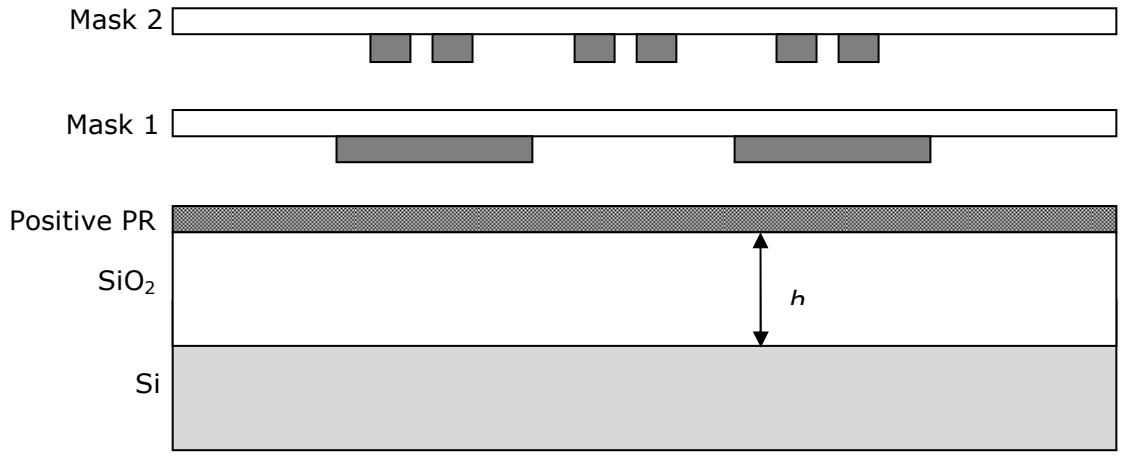
The ions are accelerated by the field and they come down normal to the wafer surface. They induce mechanical damage, which is needed to initiate the reaction of the radicals with the surface. Also mention sidewall coating inhibiting sidewall etching.

d) Briefly (3 sentences max) explain how adding O_2 to CF_4 plasma etch may affect the Si etch rate. (3 pts)

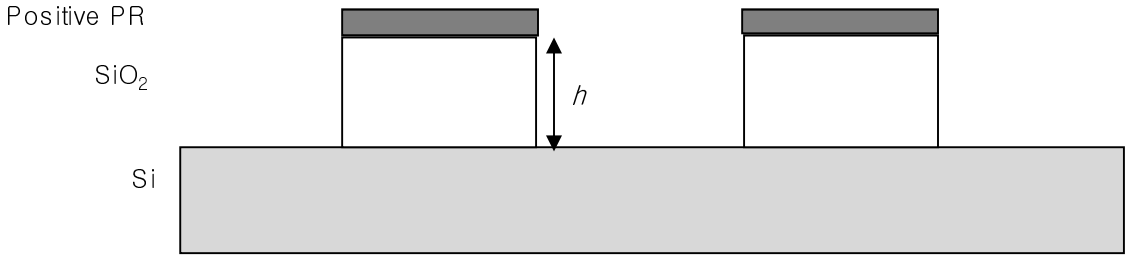
Adding a small amount of Oxygen results in the breakup of the CF_4 molecule and release of more F* ($O + CF_x \rightarrow COF_{x-1} + F^*$). Adding too much slows down the reaction by oxidizing the Si ($Si + O_2 \rightarrow SiO_2$).

5. **Photolithography (23 pts)**

Consider the following masks and wafer cross-section:



a) First we use only Mask 1 as a <u>contact mask</u> to pattern the wafer. Draw the cross section of the wafer after exposing, developing, and selective dry etching of SiO_2 to completion (until bare Si is reached). Assume a positive PR and that the dry etch is a <u>fully anisotropic</u>. (3 pts)



b) Now the PR layer is stripped in acetone, and a new conformal layer of Positive PR is applied. Assume that the thickness of this PR layer is negligible compared to *h* (thickness of the oxide). This time, projection printing is used with a second mask, Mask 2, which will be used to simultaneously pattern both Si and SiO_2 exposed surfaces. Which parameter of the projection system determines whether we will be able to achieve the same feature size on both layers? (2 pts)

Depth of Focus

c) Suppose we decide to set the parameter from (b) such that we are able to achieve near identical resolution on both Si and SiO_2. What is the smallest possible resolution that can be achieved on this photolithography step? (Assume that the following parameters are known: λ, k_1, k_2, h. Express your answer in terms of these variables.) (3 pts)

The resolution we can get is limited by our required Depth of Focus:

$$\Delta z = k_2 \frac{\lambda}{(NA)^2} = \frac{h}{2} \Rightarrow NA = \sqrt{2k_2 \frac{\lambda}{h}}$$

$$\therefore l_m = k_1 \frac{\lambda}{NA} = k_1 \frac{\lambda}{\sqrt{2k_2 \frac{\lambda}{h}}} = k_1 \sqrt{\frac{h\lambda}{2k_2}}$$

d) Propose one route to further enhance the resolution limit described in part (c). (2 sentences max) (2 pts)

e.g. phase shift mask, immersion lithography

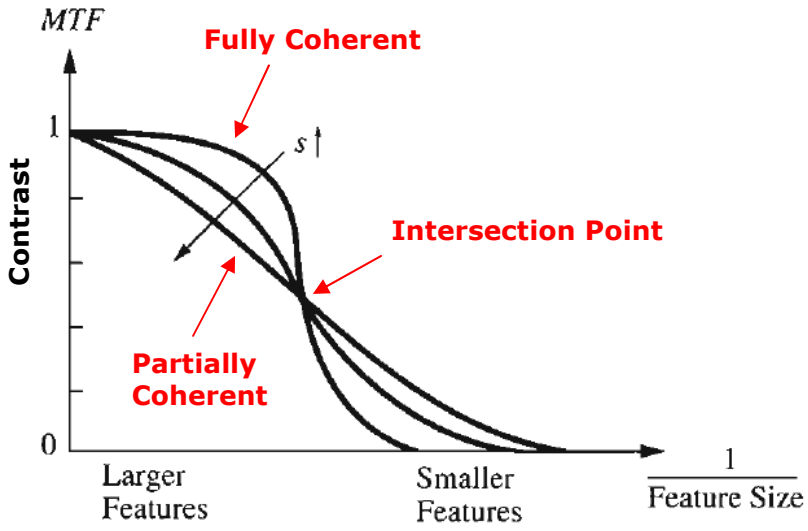
Note: Reducing λ alone would also reduce Δz, which we already set at its minimum acceptable value. Similarly, increasing NA alone would not work. Immersion lithography has the benefit of possibly altering k_2 in addition to NA.

e) List 2 advantages and 2 disadvantages of positive PR over negative PR. (3 pts)

Advantages:
- **Higher resolution**
- **Aqueous-based solution**

Disadvantages:
- **Less sensitive (lower exposure throughput)**
- **Less tolerant of developing conditions**
- **Less chemically resistant**

f) Draw two curves in the following plot of image contrast vs. inverse feature size, one corresponding to a fully coherent light source and the other to a partially coherent light source for projection lithography. Please clearly label the two curves. Also, label the minima and maxima values for contrast. (3 pts)



g) Briefly explain the effect that coherency of light has on the photolithography resolution. (3 pts)

The effect is different depending on which side of the intersection point you're working in.

For features sizes in the "large" range, less coherence will result in worse resolution. This is because the diffraction pattern of a given feature will be spread out over a larger angle, causing some information to be lost outside the finite aperture.

However, for features in the "small" range, less coherence will instead improve resolution. This is because a nearby feature that ordinarily would have been lost outside the aperture is partially smeared into the aperture. Features that are spaced far apart (i.e. large features) do not benefit from this effect.

h) Briefly explain what determines the resolution attained by electron beam lithography? (2 pts)

Although the wavelength of the electron beam determines the theoretical resolution, the actual resolution attained is determined by limiting factors such as the resist resolution, beam current, beam quality, or secondary electrons.

i) Briefly explain why electron beam lithography is not commonly used as a patterning process in IC manufacturing. (2 pts)

The throughput is low since the process is very slow for each wafer, and the equipment is too expensive to use a large number of machines in parallel.