EECS 16B Designing Information Devices and Systems II
Spring 2021 Midterm 1: Exam Instructions

Read the following instructions before the exam.

Good luck on the exam! We know you've worked hard, and we are rooting for you to do well!

Our advice to you: if you can't solve a particular problem, move on to another, or try a simpler one. You will perhaps find yourself on a path to the solution. **We believe in you!**

Format & How to Submit Answers

This exam starts with the honor code and and introductory questions, followed by 6 exam questions containing subparts with varying points. The problems are of varying difficulty, so **pace yourself accordingly and avoid spending too much time on any one question until you have gotten all of the other points you can**. If you are having trouble with one subpart, there may be easier points available later!

Complete your exam using either the template provided or appropriately created sheets of paper. Either way, you should submit your answers to the *Gradescope* assignment that is marked MIDTERM for your specific exam group. Make sure you submit your assignment to the correct *Gradescope* assignment. You MUST select pages for each question. We cannot grade your exam if you do not select pages for each question. If you are having technical difficulties submitting your exam, make a private Piazza post. You can email your answers to `eecs16b-sp21@berkeley.edu`, to meet the deadline and then upload to *Gradescope* as soon as possible after.

In general, show all your work legibly to receive full credit; we cannot grade anything that we cannot read. For some problems, we may try to award partial credit for substantial progress on a problem, and showing your work clearly and legibly will help us do that.

Timing & Academic Honesty

You are expected to follow the rules provided in the Exam Proctoring Guidelines.

https://docs.google.com/document/d/1ZCr6Vl8c5p90UzeUO7zYCmM_kc74KRNE9ZIy1tEygbE/edit?usp=sharing

The exam will be available to you at the link sent to you via email. The exam will be from 7-9pm Pacific Time, Monday, March 15th, 2021, unless you have an exam accommodation. Most of you will submit your exam by 9:40pm (9:30pm with tablet), unless you have an accommodation otherwise. An exam that is submitted N minutes after the end of the submission period will lose 2^N points. This means that if you are 1 minute late you will lose 2 points; if you are 5 minutes late you will lose 32 points and so on.

You may consult **one** handwritten 8.5" by 11" cheat sheet (front and back of one piece of paper). Do not attempt to cheat in any way. We have a zero tolerance policy for violations of the Berkeley Honor Code. On your browser, the only websites you may have open are

- the exam PDF and the Google doc with exam link, and any exam clarifications
- the detailed proctoring guidelines and/or the proctoring summary
- Piazza if necessary for emergencies
- Gradescope to submit the exam
- if necessary, other websites related to compiling or submitting your exam.

Any other open website will be considered a violation of policy.

EECS 16B Designing Information Devices and Systems II
Spring 2021 Midterm 1: Exam

The exam has *130* points. *125* points will be considered a full score.

1. Honor Code

If you have not already done so, please **copy the following statements into the box provided** for the honor code on your answer sheet, and **sign your name**.

I will respect my classmates and the integrity of this exam by following this honor code. I affirm:

- I have read the instructions for this exam. I understand them and will follow them.
- All of the work submitted here is my original work.
- I did not reference any sources other than my allocated reference cheat sheet(s).
- I did not collaborate with any other human being on this exam.

2. Pre-Exam Questions

a) **[2 points]** What is a TV show you've watched, or book/article you've read, that you found inspiring?
All answers will be awarded full credit.

b) **[2 points]** What are you looking forward to over Spring Break?
All answers will be awarded full credit.

3. Potpourri!

a) **[4 points]** You are given the graph in Figure 1. **Express the coordinates of vectors $\vec{v}$ and $\vec{w}$ in both Cartesian $((x,y))$ and Polar $\left(re^{j\theta}\right)$ form**. *You do not need to show your work for this subpart.*

You may use the atan2 or $\tan^{-1}$ function for angle (θ) as necessary.

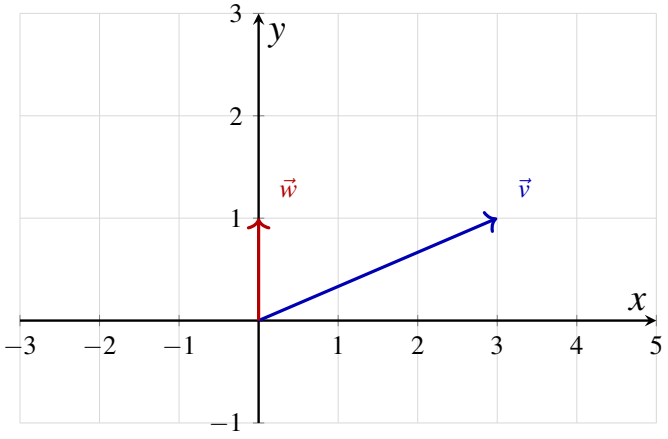


Figure 1: Vectors in the $\mathbf{x}-\mathbf{y}$ plane

i) Label $\vec{v}$ with its corresponding Cartesian $((x,y))$ and Polar $\left(re^{j\theta}\right)$ coordinates, in the given form.

ii) Label $\vec{w}$ with its corresponding Cartesian $((x,y))$ and Polar $\left(re^{j\theta}\right)$ coordinates, in the given form.

b) **[6 points]** You are given an input voltage signal below:

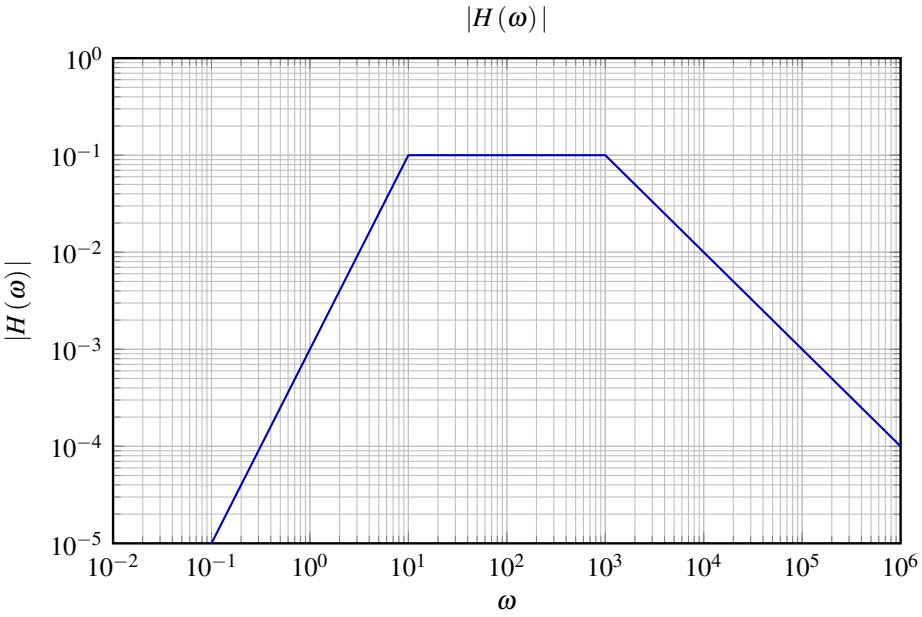
$$v_{\text{in}}(t) = -2\cos\left(\omega t + \frac{\pi}{3}\right). \tag{1}$$

Convert the signal of eq. (1) to its phasor representation. That is, find $\widetilde{V}_{\text{in}}$. *Justify your answer.*

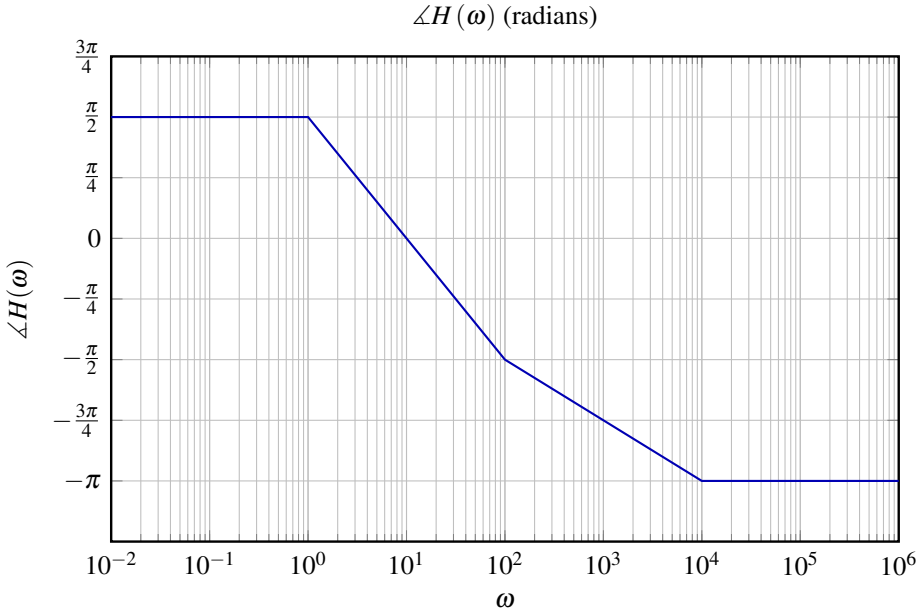
c) **[6 points]** You decided to analyze the transfer function of a band-pass filter, and have generated the Bode plots in Figure 2a and Figure 2b for $H(\omega)$. **If your input voltage signal is**

$$v_{\text{in}}(t) = 10\cos\left(\omega_s t + \frac{\pi}{3}\right), \tag{2}$$

where $\omega_s = 10^4$, **what is** $v_{\text{out}}(t)$? *Show your work and explain your answers. You do not need to copy the figures below to your answer sheet, you may just tell us what you read from the Bode plots.*



(a) Magnitude Bode Plot for part (c).



(b) Phase Bode Plot for part (c).

Figure 2: Bode Plots for part (c).

4. Analyzing an LC-LC Band-Stop/Notch Filter

In this sub-part, you will partially analyze a circuit built entirely out of L, C components as shown in Figure 3. Assume that the circuit is operating at a frequency of $\omega = \omega_s$ (i.e. $v_{\text{in}}(t) = \cos(\omega_s t)$).

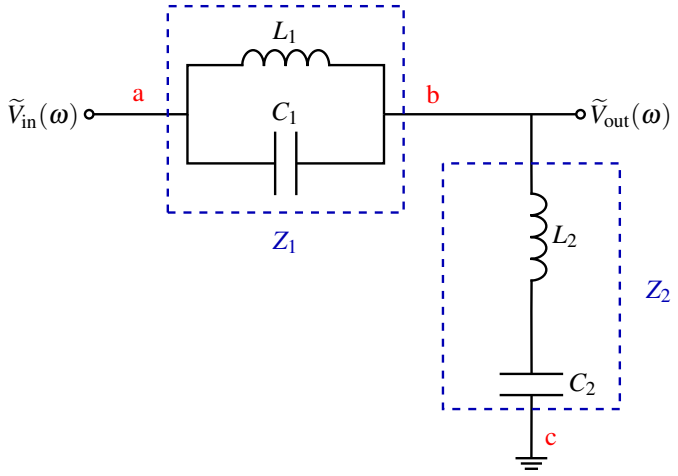


Figure 3: LC bandstop filter.

a) **[5 points] Find $\widetilde{V}_{\text{out}}(\omega)$ in terms of Z_1, Z_2, $\widetilde{V}_{\text{in}}(\omega)$.** *You do not need to compute $\widetilde{V}_{\text{in}}(\omega)$ for this part. Show your work.*

b) **[5 points] Find Z_1, the equivalent impedance between terminals a and b, in terms of L_1, C_1, and ω_s.** Leave your answer in the form $j\frac{M}{N}$, where M and N are real.
What is the impedance Z_1 at $\omega_s = \frac{1}{\sqrt{L_1 C_1}}$? *Show your work and justify your answers.*

c) **[5 points] Find Z_2, the equivalent impedance between terminals b and c, in terms of L_2, C_2, and ω_s.** Leave your answer in the form $j\frac{M}{N}$, where M and N are real.
What is the impedance Z_2 at $\omega_s = \frac{1}{\sqrt{L_2 C_2}}$? *Show your work and justify your answers.*

5. Hey Circuit, are you a Low-Pass Filter?

You have a mystery black box and you believe it contains an RC low-pass filter. You want to use the tools of converting a model from continuous-time to discrete-time and System ID to test your guess.

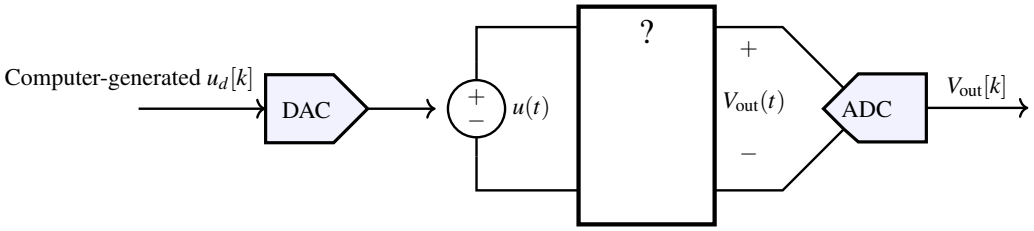


Figure 4: A schematic to show how our computer generated signals will interface through the DAC and the ADC with the mystery box.

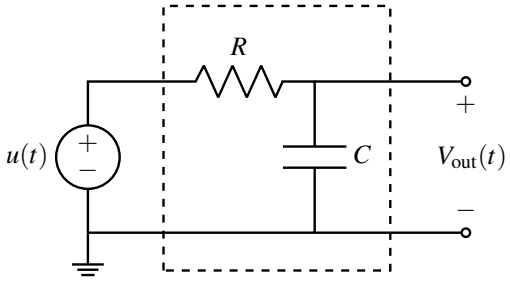


Figure 5: RC circuit that you suspect is inside the mystery (?) box.

a) **[4 points]** You know from lecture that the continuous-time equation

$$\frac{dx(t)}{dt} = \lambda x(t) + bu(t), \tag{3}$$

can be converted to a discrete-time equation given by

$$x_d[k+1] = e^{\lambda\Delta}x_d[k] + b\left(\frac{e^{\lambda\Delta}-1}{\lambda}\right)u_d[k], \tag{4}$$

where $x_d[k] = x(k\Delta)$ and $u_d[k] = u(k\Delta)$, for some constant Δ.
Assume that eq. (3) references the RC circuit in Figure 5. For a low-pass RC filter with input $u(t)$ you know that the following differential equation holds:

$$\frac{dV_{\text{out}}(t)}{dt} = -\frac{1}{RC}V_{\text{out}}(t) + \frac{1}{RC}u(t). \tag{5}$$

Convert this continuous system to a discrete-time difference equation for $V_{\text{out}}[k]$ in the form of

$$V_{\text{out}}[k+1] = \lambda_d V_{\text{out}}[k] + b_d u_d[k],$$

and write λ_d and b_d in terms of R, C, and Δ. *Show your work.*

b) **[5 points]** Now ignoring the physics of the model, you decide to use a data-centric approach to find λ_d and b_d in your model. In order to do so, you apply a sequence of inputs for 4 timesteps $u_d[0], u_d[1], u_d[2], u_d[3]$ and observe $V_{\text{out}}[0], V_{\text{out}}[1], V_{\text{out}}[2], V_{\text{out}}[3]$, and $V_{\text{out}}[4]$. You decide to use least squares of the form $D\vec{p} \approx \vec{y}$, with $\vec{p} = \begin{bmatrix} \lambda_d \\ b_d \end{bmatrix}$.

Write the matrix D and vector $\vec{y}$. *Write your answers in the provided box.*

6. A Spring System

The tools we have learned in this class are not limited to circuits. In this problem we will examine the following spring-mass system. This system can be modeled with eq. (6), where $x(t)$ is the position of the mass at time t, m is the constant mass of the block, and $u(t)$ is the force input to the system at time t.

$$\frac{d^2x(t)}{dt^2} = -\frac{k_1}{m}x(t) - \frac{k_2}{m}\frac{dx(t)}{dt} + \frac{1}{m}u(t). \tag{6}$$

a) **[4 points] Rewrite eq. (6) as a system of differential equations in the matrix form.** Let the state variables be $\vec{y} = \begin{bmatrix} x(t) \\ \frac{dx(t)}{dt} \end{bmatrix}$. *Show your work.*

b) **[10 points]** Regardless of your answer to the previous question, assume that you end up with the following system:

$$\frac{d\vec{y}(t)}{dt} = \begin{bmatrix} 0 & 1 \\ -3 & -4 \end{bmatrix}\vec{y}(t) + \begin{bmatrix} 0 \\ 2 \end{bmatrix}u(t). \tag{7}$$

The matrix $A = \begin{bmatrix} 0 & 1 \\ -3 & -4 \end{bmatrix}$ can be diagonalized as $A = V\Lambda V^{-1}$ where

$$V = \begin{bmatrix} 1 & 1 \\ -1 & -3 \end{bmatrix}, \tag{8}$$

$$\Lambda = \begin{bmatrix} -1 & 0 \\ 0 & -3 \end{bmatrix}, \tag{9}$$

$$V^{-1} = \begin{bmatrix} \frac{3}{2} & \frac{1}{2} \\ -\frac{1}{2} & -\frac{1}{2} \end{bmatrix}. \tag{10}$$

If the input is fixed to a constant $u(t) = u_0 \in \mathbb{R}$ for all t, **find the solution to the system of differential equations in eq. (7).** Use $\vec{y}(0) = \begin{bmatrix} \alpha \\ 0 \end{bmatrix}$ as the initial condition. *Show your work and justify your answers.*

c) **[5 points]** Suppose you apply a piece-wise constant input to this system, such that $u(t)$ is constant over intervals of Δ:

$$u(t) = u(i\Delta) = u_d[i] \text{ for } t \in [i\Delta, (i+1)\Delta), \tag{11}$$

and suppose your solution to the differential equation for the spring-mass system for $t \in (i\Delta, (i+1)\Delta]$ is

$$y_1(t) = (y_1(i\Delta) - u_d[i])e^{-(t-i\Delta)} + 2 \cdot y_2(i\Delta)e^{-2(t-i\Delta)} + u_d[i], \tag{12}$$

$$y_2(t) = -(y_1(i\Delta) - u_d[i])e^{-(t-i\Delta)} - 4 \cdot y_2(i\Delta)e^{-2(t-i\Delta)}, \tag{13}$$

Given the initial conditions $\vec{y}(0) = \begin{bmatrix} 4 \\ 0 \end{bmatrix}$ and input $u_d[0] = 4$, find $\vec{y}(\Delta)$. Assume $e^{-\Delta} = 0.5$. *Show your work and justify your answers.*

d) **[4 points]** We decide to examine stability of this system in discrete time, so we fix Δ and derive the following discretized system:

$$\vec{y}_d[k+1] = \begin{bmatrix} \frac{3}{4} & \frac{1}{4} \\ -\frac{1}{4} & \frac{1}{4} \end{bmatrix} \vec{y}_d[k] + \begin{bmatrix} \frac{3}{4} \\ \frac{1}{4} \end{bmatrix} u_d[k]. \tag{14}$$

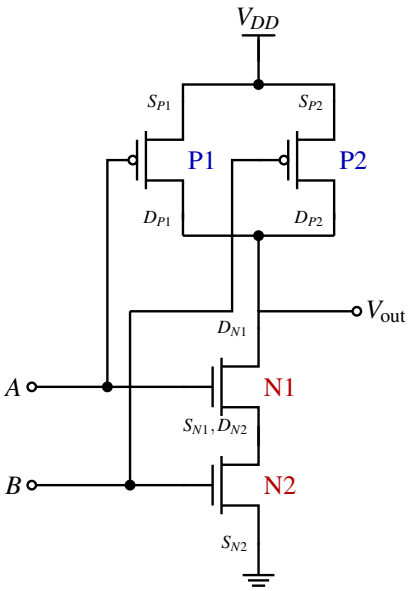
Identify if this open-loop system is stable. *Show your work and justify your answers.*

e) **[4 points]** If we put the system defined in eq. (14) in feedback, setting $u_d[k] = \begin{bmatrix} 1 & 1 \end{bmatrix} \vec{y}_d[k]$, **is the resulting closed-loop system stable?** *Show your work and justify your answers.*

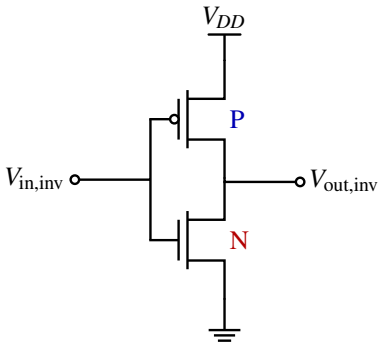
7. Transistor Switch Model

In this problem, we will analyze the behavior of a NAND gate driving an inverter. Figure 6a shows the transistor model of a NAND gate and Figure 6b shows the transistor model of an inverter.

In this question assume that V_{DD} is greater than both the NMOS threshold $V_{\text{th,n}}$ and PMOS threshold $|V_{\text{th,p}}|$.



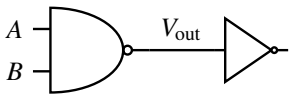
(a) NAND schematic with transistors.



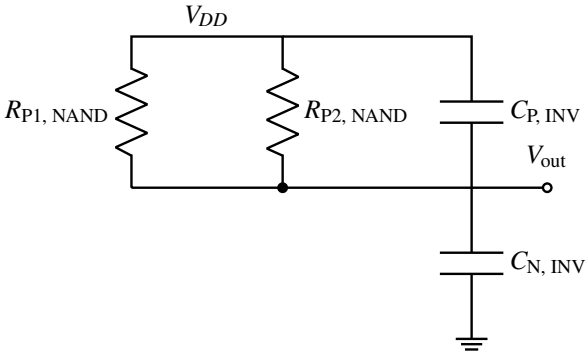
(b) Inverter schematic with transistors.

Figure 6: Transistor schematics

a) **[5 points]** A diagram of a NAND gate driving an inverter is shown in Figure 7a. Consider the case where $A = V_{DD}$ and $B = V_{DD}$ for a long time before $t = 0$. Then at $t = 0$, we switch A and B to 0 V. The equivalent simplified circuit after this transition is shown in Figure 7b. **Find V_{out} at time $t = 0$.** *Write your answers in the provided box.*



(a) NAND driving an Inverter



(b) A Simplified Equivalent Circuit for when $A = B = 0$V

Figure 7: Schematic and model of a NAND gate driving an inverter

b) **[8 points] Write the differential equation for solving $V_{\text{out}}(t)$ for $t \geq 0$ in the circuit shown in Figure 7b.** Specifically, **find coefficients λ and b in the following symbolic differential equation:**

$$\frac{dV_{\text{out}}(t)}{dt} = \lambda V_{\text{out}}(t) + bV_{DD}, \tag{15}$$

as a function of $R_P, C_{\text{P, INV}}, C_{\text{N, INV}}$, and V_{DD}. Assume that $R_{\text{P1,NAND}} = R_{\text{P2, NAND}} = R_P$. *Show your work and justify your answers.*

c) **[8 points] Solve $V_{\text{out}}(t)$ in the differential equation (15) and the initial condition $V_{\text{out}}(0)$.** You should leave your answer in terms of λ, b, V_{DD}, and $V_{\text{out}}(0)$. *Show your work and justify your answers.*

d) **[8 points]** Now consider the case where $A = 0$V and $B = 0$V for a long time before $t = 0$ in Figure 7a. At $t = 0$ we switch A and B to V_{DD}. **Write down the state (ON/OFF) of transistors P1, P2, N1, and N2 in the NAND gate. Draw the equivalent simplified circuit for this transition that will help us with writing the differential equation of $V_{\text{out}}(t)$.** *Write your answers in the provided box.*

Hint: You may find the NAND resistor-switch model in Figure 8 helpful. Don't forget to include the inverter's capacitors, $C_{N,\,INV}$ and $C_{P,\,INV}$, which are loading the NAND gate.

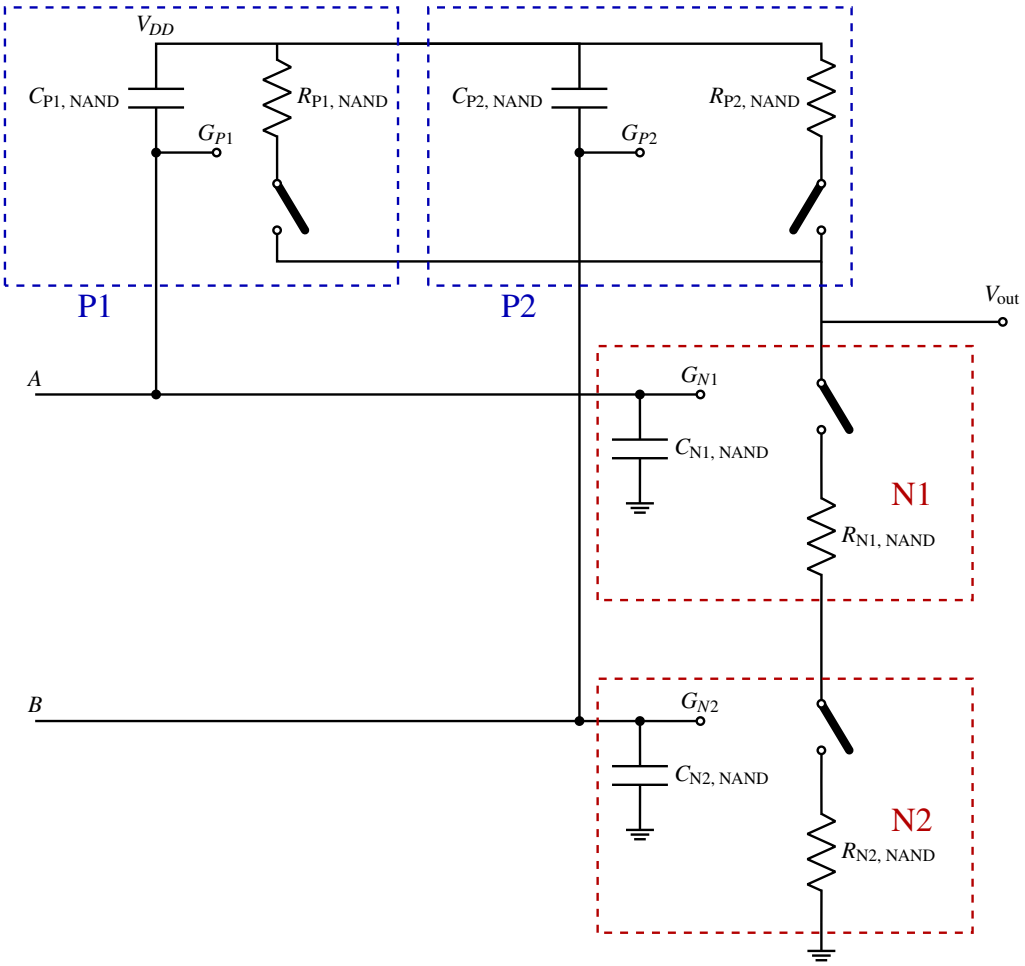


Figure 8: NAND Model: Capacitances

8. Loud Neighbors

The neighbors keep throwing loud parties and Divija is having trouble sleeping despite her ear plugs. She decides to build a device to reduce the noise, and needs your help designing the filters.

a) **[4 points]** Divija decides to build a band-stop filter by combining a low-pass and a high-pass filter. To start off, consider the skeleton circuit in Figure 9. **What is V_{out} in terms of u_1, u_2, and R?**

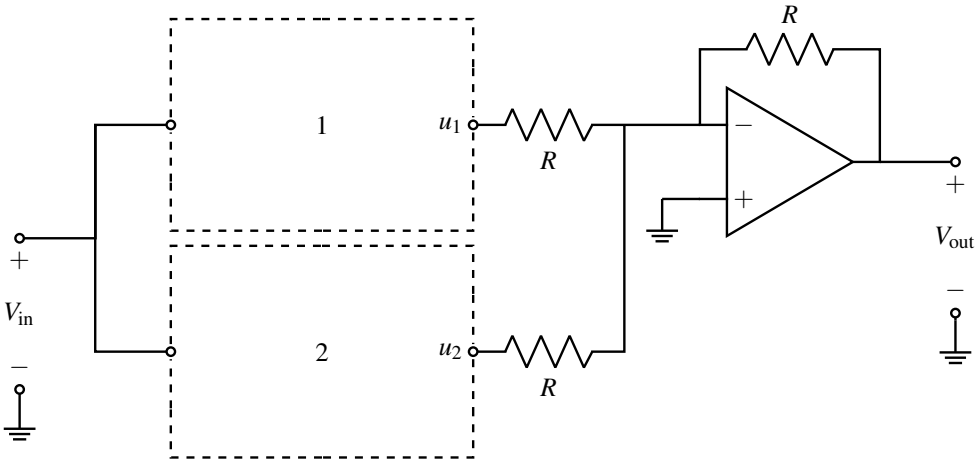


Figure 9: Skeleton Circuit for part (a).

b) **[6 points] Design a *high-pass* filter for Box 2.** This should be a circuit with cutoff frequency $\omega_c = 10^4 \text{rad/s}$ that can drive an arbitrary load. You may use one resistor, one op-amp, and one $1\mu\text{F} = 10^{-6}\text{F}$ capacitor. **Choose the value of the resistor to get the correct cut-off frequency ω_c.** *Show your work and justify your answers.*

[Question Continues on Next Page]

c) **[6 points]** Divija designed the **low-pass** filter shown in Figure 10 for a cut-off frequency of $\omega_c = 10^2 \text{rad/s}$ to be used in Box 1. To verify that the circuit she built matched the circuit she designed, she decided to test the circuit in isolation by applying an input V_{in} and measuring the filter's output V_{out}. The input output behavior of the circuit she built is shown in Figure 11.

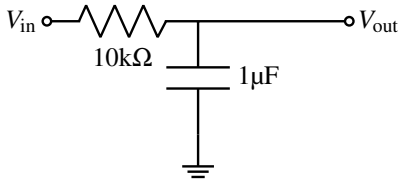


Figure 10: The filter Divija intended to build.

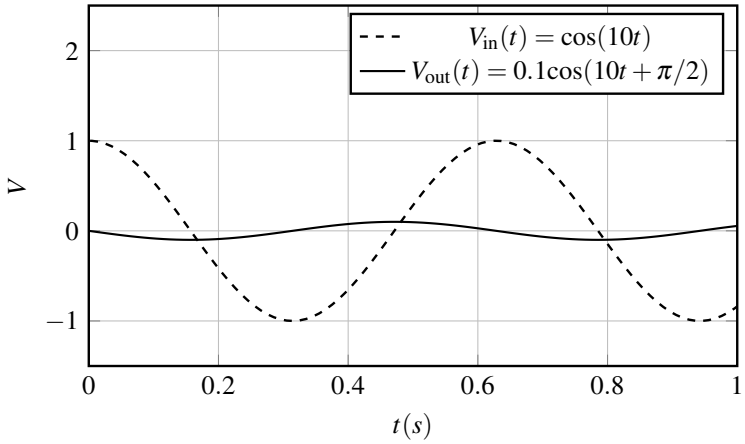


Figure 11: Input-Output behavior of the filter Divija built.

What is the most likely cause for this behavior? *Show your work and justify your answers.*

i) The resistors and capacitors were swapped.
ii) She used an inductor instead of the resistor.
iii) She used a 10μF capacitor and a resistor of 1kΩ.

[Question Continues on Next Page]

d) **[8 points]** After looking through the available components Divija realizes that she doesn't have enough capacitors and decides to build the filter with inductors instead. Assume she builds the overall circuit in Figure 12. **Find the transfer functions $H_1(\omega) = \frac{\widetilde{u}_1}{\widetilde{V}_{\text{in}}}$ and $H_2(\omega) = \frac{\widetilde{u}_2}{\widetilde{V}_{\text{in}}}$ in terms of L_1, L_2, R_1, R_2, and R_s.** *Show your work and justify your answers.*

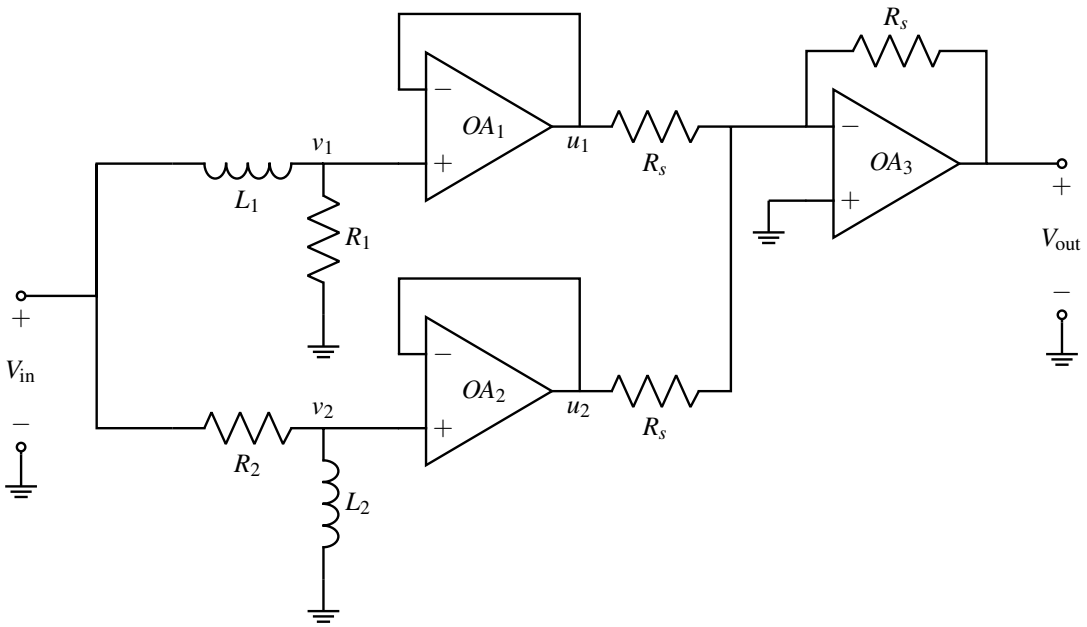


Figure 12: Overall Circuit

e) **[6 points]** Assume the overall transfer function of the final circuit in Figure 12, $H(\omega) = \frac{\widetilde{V}_{\text{out}}}{\widetilde{V}_{\text{in}}}$, is

$$H(\omega) = \left(\frac{1}{1 + j\omega/\omega_{c1}} + \frac{j\omega/\omega_{c2}}{1 + j\omega/\omega_{c2}} \right), \tag{16}$$

where $\omega_{c2} = 100\omega_{c1}$. **Qualitatively describe the magnitude of the transfer function $|H(\omega)|$ in three regions: frequencies below ω_{c1}, frequencies between ω_{c1} and ω_{c2}, and frequencies above ω_{c2}. Explain what the filter is doing qualitatively** (for example, a low-pass filter passes low frequencies but does not pass high frequencies). *Show your work and justify your answers.*