EECS 16A Designing Information Devices and Systems I
Fall 2020 Midterm 2

Midterm 2 Solution

1. HONOR CODE

If you have not already done so, please copy the following statements into the box provided for the honor code on your answer sheet, and sign your name.

I will respect my classmates and the integrity of this exam by following this honor code. I affirm:

- *I have read the instructions for this exam. I understand them and will follow them.*
- *All of the work submitted here is my original work.*
- *I did not reference any sources other than my allocated reference cheat sheet(s).*
- *I did not collaborate with any other human being on this exam.*

2. (a) **(2 Points) What are you looking forward to after this midterm?** *All answers will be awarded full credit.*

(b) **(2 Points) Tell us about something that makes you happy.** *All answers will be awarded full credit.*

3. Circuit Analysis (14 points)

(a) (3 points) Which components violate passive sign convention in Fig. 3.1? In your answer sheet, write down all that apply. **For full credit, you must write only components that *violate* passive sign convention. If you list any other components, you will receive no points.**

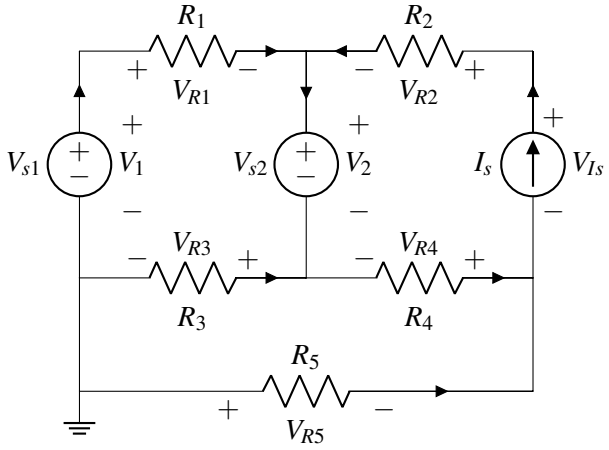


Figure 3.1: Schematic for part (a).

(1) R_1	(3) R_3	(5) R_5	(7) V_{s1}
(2) R_2	(4) R_4	(6) I_s	(8) V_{s2}

Solution: The only elements that have **violated** the current flowing into positive and coming out the negative voltage labellings are R_3, R_4, V_{s1}, I_s.

(b) (3 points) **Write a KVL expression for the loop drawn in Fig. 3.2. Your answer should be in terms of u_1, u_2, u_3, u_4, or u_5 and V_{s1} and V_{s2}**, please do not add labels to the figure. Show your work.

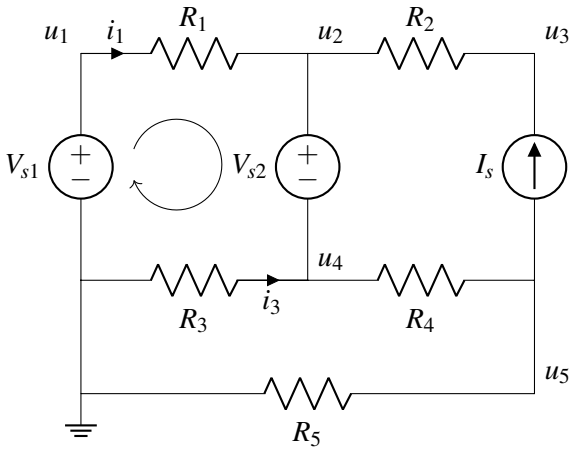


Figure 3.2: Schematic for part (b).

Solution: If we look at the voltage drops around the loop clockwise, we can write the KVL expression as:

$$(0-u_1)+(u_1-u_2)+(u_2-u_4)+(u_4-0)=0$$

We can recognize that $(0-u_1)=-V_{s1}$ and $u_2-u_4=V_{s2}$ to rewrite the expression in another way:

$$-V_{s1}+(u_1-u_2)+V_{s2}+(u_4-0)=0$$

We can also recognize that $(u_1-u_2)=R_1i_1$ and $(u_4-0)=-R_3i_3$ to rewrite the expression in yet another way:

$$(0-u_1)+R_1i_1+(u_2-u_4)-R_3i_3=0$$

or using voltage sources:

$$-V_{s1}+R_1i_1+V_{s2}-R_3i_3=0$$

Any equivalent variant of the four expressions above are acceptable.

(c) (3 points) **Write the expression** for KCL at node P in terms of currents I_s, i_4, and i_5 as labelled in Fig. 3.3. Then, **re-write the expression** in terms of I_s, node voltages, and resistances only. The rewritten expression should not contain i_4, and i_5. Note that P is a label for a node, and is not a node voltage value. Show your work.

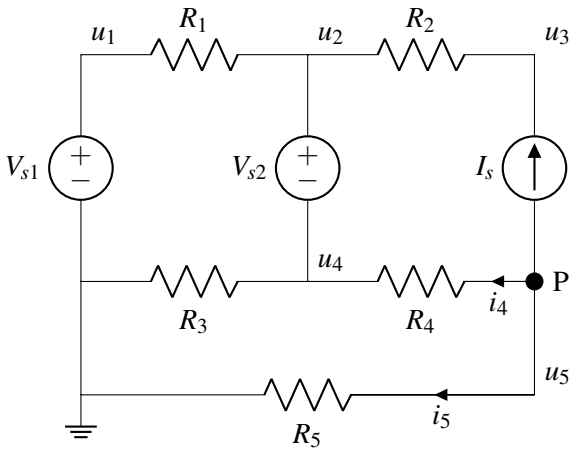


Figure 3.3: Schematic for part (c).

Solution: The first expression is KCL at the node P in terms of currents I_s, i_4, and i_5. These currents are all leaving the node P, and 0 current enters the node:

$$0=I_s+i_4+i_5$$

To re-write the expression in terms of I_s, node voltages, and resistances only, we recognize using Ohm's law that $i_4=\frac{u_5-u_4}{R_4}$ and $i_5=\frac{u_5}{R_5}$. Using this, we re-write the KCL expression as:

$$0=I_s+\frac{u_5-u_4}{R_4}+\frac{u_5}{R_5}$$

(d) (2 point) Given the node voltage $u_4 = 3\text{V}$ in Fig. 3.4, **find the node voltage** u_2. Justify your answer. *Hint: You should not have to do many calculations for this part.*

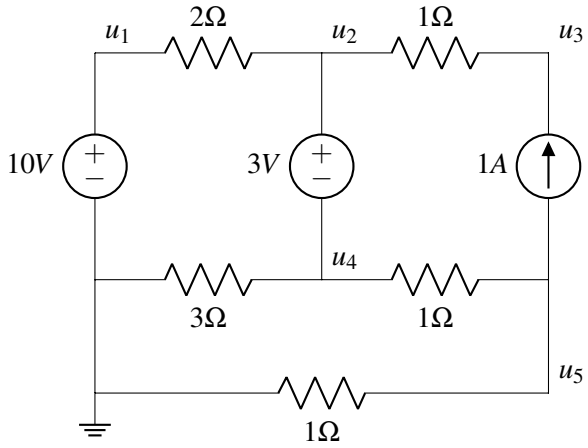


Figure 3.4: Schematic for parts (d) and (e).

Solution: $u_2 = u_4 + 3\text{V} = 6\text{V}$.

(e) (3 point) How would you connect an ammeter to this circuit to measure current flowing through the 3Ω resistor in Fig. 3.4? Recall that an ammeter is a device that measures current, and its symbol is shown in Fig. 3.5. **In your answer sheet, redraw the full schematic from Fig. 3.4 with the ammeter connected correctly.**

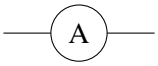


Figure 3.5: Ammeter symbol.

Solution: The ammeter must be placed in series with the element the current is passing through. As such, it must be placed in series with the 3Ω resistor. It can be placed on either side of the resistor.

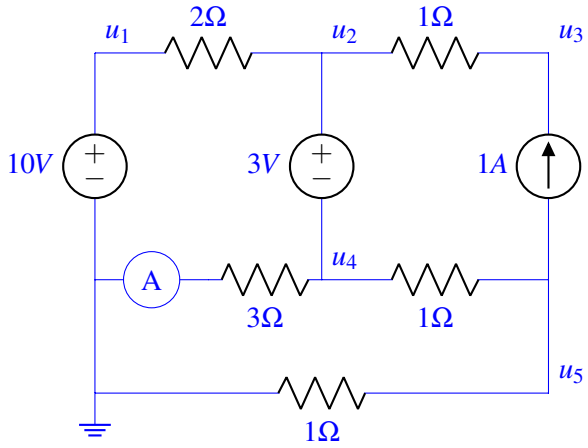


Figure 3.6: Ammeter placement to measure current flowing through the 3Ω resistor.

4. Take a Load Off (9 points)

Your 16A TA Amanda is an undergraduate researcher in Berkeley's power electronics lab, where she is working on building power converters to drive motors on electric aircraft.

As a part of her project, Amanda is building a piece of test equipment known as a resistive load bank. You are helping her do the calculations!

(a) (2 points) Consider the model in Figure (4.1) for the resistive load bank.
The load resistor $R_L = 100\,\Omega$ and $V_S = 100\,V$. **When the switch is closed, what is value of the power dissipated by R_L? Show your work.** The switch is ideal for this part, i.e. it acts a wire when it is closed.

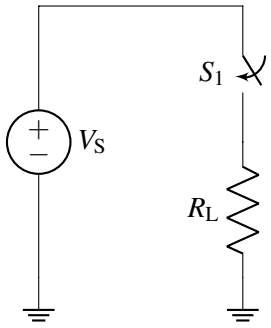


Figure 4.1: Model of resistive load bank in a circuit.

Solution:

$$P = \frac{V_S^2}{R_L}$$
$$P = \frac{100^2}{100}$$
$$P = 100\,W$$

(b) (3 points) Consider again the circuit from Figure (4.1) with the switch closed. Assume that the load resistor $R_L = 100\,\Omega$ can dissipate a max of $P_{max} = 2.5\,kW = 2.5 \cdot 10^3$ W without exceeding thermal limitations. **What is that maximum value of V_S you can use without exceeding the thermal limits? Show your work.** You may assume the switch is ideal, i.e., it acts a wire when it is closed.

Solution: Consider when the switch is closed; the power dissipated by the resistor is

$$P_{max} = \frac{V_{S,max}^2}{R_L}$$

Solving for $V_{S,max}$:

$$V_{S,max} = \sqrt{P_{max} R_L}$$
$$V_{S,max} = \sqrt{(2.5 \cdot 10^3)(100)}$$
$$V_{S,max} = 500\,V$$

(c) (4 points) For this part, we will no longer assume the switch is ideal; instead, the closed switch has a nonzero on-resistance R_{on}, as shown in Figure (4.2). You found the R_{on} dissipating 2.5 W at load current $I_{\text{L}} = 5\,\text{A}$, as shown in Figure (4.2). **What is the value of R_{on}? Show your work.**

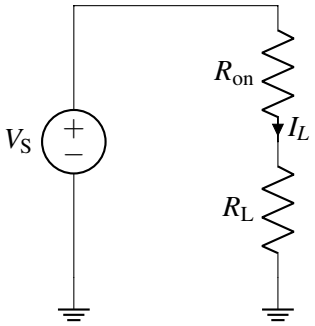


Figure 4.2: Resistive load bank in a circuit with a non-ideal switch.

Solution: Consider when the switch is closed; the power dissipated by the resistor is

$$P_{\text{sw}} = I_{\text{L}}^2 R_{\text{on}}$$

Solving for R_{on}:

$$R_{\text{on}} = \frac{P_{\text{sw}}}{I_{\text{L}}^2}$$

$$R_{\text{on}} = \frac{2.5}{5^2}$$

$$R_{\text{on}} = 0.1\,\Omega$$

5. Stay Tuned (15 points)

PG&E just announced another power outage and you desperately need a radio transmitter to battle the impending telecommunication doom! You need to build an antenna tuner, which is a variable resistor to control the power of the transmitter signal.

This tuner consists of two identical resistive bars (M_1 and M_2) of length L, and a cross-sectional area of A, as shown in Figure 5.1. The strips are made of a material with resistivity ρ. The resistive bars are connected with ideal electrical wires in the following configuration:

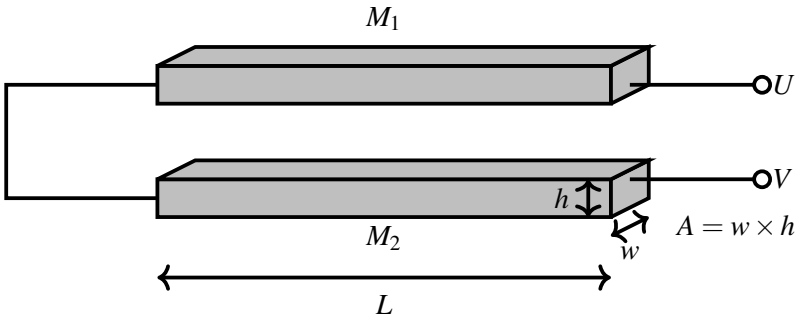


Figure 5.1: Resistive metal bars connected through ideal wires.

(a) (4 points) Let R_{UV} be the equivalent resistance between nodes U and V in Figure 5.1. **Write an expression for R_{UV} in terms of L, A, ρ and other numerical values.** Show your work.

Solution: M_1 and M_2 have the following resistances:

$$R_{M1} = \frac{\rho L}{A};$$

$$R_{M2} = \frac{\rho L}{A}.$$

These two resistors are connected in series. So the equivalent resistance is given by

$$R_{UV} = R_{M1} + R_{M2} = \frac{\rho L}{A} + \frac{\rho L}{A} = \frac{2\rho L}{A}.$$

(b) (6 points) The resistive bar M_1 is flexible, so if we press any point on it a contact is made between M_1 and M_2. As shown in Figure 5.2, a sliding contact is used to make a contact at position x_0.

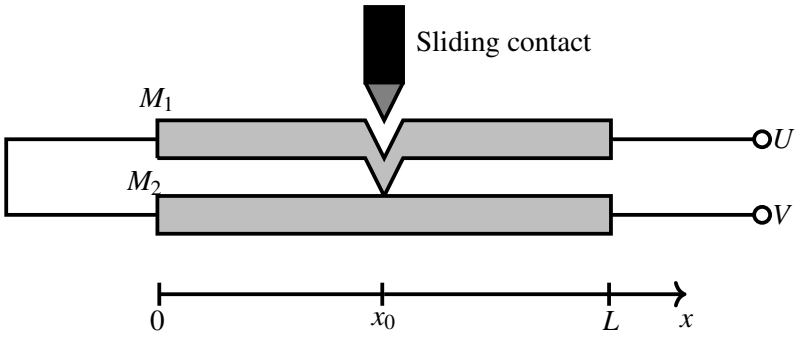


Figure 5.2: Sliding switch making a contact between M_1 and M_2.

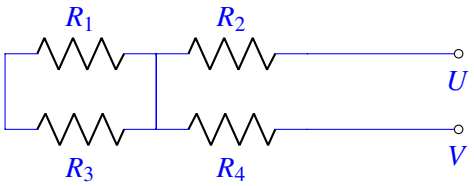
(i) **Draw a circuit diagram that represents the scenario in Figure 5.2. The sliding contact has no resistance and acts like a wire when the contact is made.** *Hint: Your diagram should have four resistors.*

(ii) **Express the equivalent resistance between nodes U and V, i.e., R_{UV} in terms of L, x_0, A, ρ and other numerical values, when the sliding contact is present**.

(iii) Assume $x_0 = 8\text{cm}$, $L = 10\text{cm}$, $A = 10^{-3}\text{cm}^2$, and $\rho = 5\times10^{-3}\Omega\text{cm}$. **Find the value of R_{UV} when the sliding contact is present. Show your work.**

Solution:

(i) The sliding contact can be modeled as a wire with no resistance. The segments of M_1 on both sides of the contact can be modeled as two resistors: R_1 and R_2. Similarly the segments of M_2 on both sides of the contact can be modeled as two resistors R_3 and R_4. So the circuit diagram representing the metal strips with sliding contact is the following:



(ii) The resistances in the diagram are given by:

$$R_1 = \frac{\rho x_0}{A}, \quad R_2 = \frac{\rho(L-x_0)}{A}, \quad R_3 = \frac{\rho x_0}{A}, \quad \text{and} \quad R_4 = \frac{\rho(L-x_0)}{A}$$

R_1 and R_3 are shorted by the sliding contact, so they are not not going to contribute to the equivalent resistance. This means that if we apply a voltage across terminals U and V, no current will go through R_1 and R_3, as the sliding contact offers a path with zero resistance. The equivalent resistance R_{UV} is given by the series combination of R_2 and R_4 only:

$$R_{UV} = R_2 + R_4 = \frac{\rho(L-x_0)}{A} + \frac{\rho(L-x_0)}{A} = \frac{2\rho(L-x_0)}{A}.$$

(iii) The value of R_{UV} can be found by plugging in $p = 8\text{cm}$ in the above equation:

$$R_{UV} = \frac{2\rho(L-8)}{A} = \frac{2\times5\times10^{-3}\Omega\text{cm}(10\text{cm}-8\text{cm})}{10^{-3}\text{cm}^2} = 20\Omega.$$

(c) (5 points) Now let us model the transmitter as a voltage source V_S, in series with a resistor R_S, while our antenna tuner is represented by R_{UV}. The circuit model is shown in Figure 5.3:

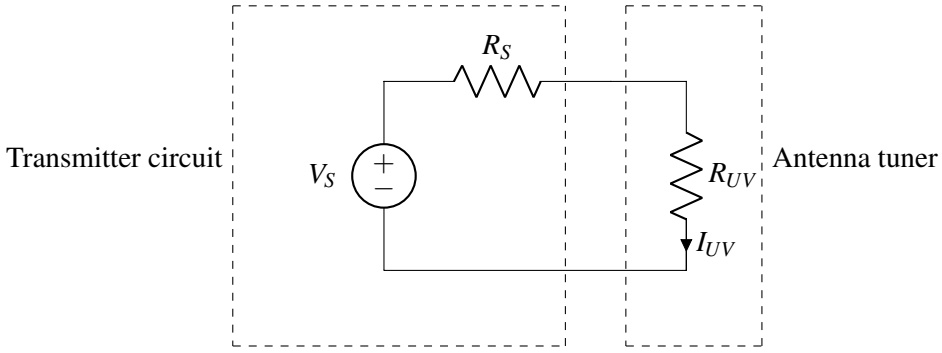


Figure 5.3: Circuit model for the radio transmitter.

In order to prevent damage to the tuner, we need to make sure that the current through R_{UV} never exceeds 0.1A. **Assuming** $20\Omega \leq R_{UV} \leq 80\Omega$ **and** $R_S = 50\Omega$**, find the maximum allowable value of** V_S**, so that** $I_{UV} \leq 0.1\text{A}$ **for the full range of** R_{UV}**. Show your work.**

Solution: Resistances R_S and R_{UV} are in series, so their equivalent is given by $R_{eq} = R_S + R_{UV}$. So using Ohm's law we can calculate I_{UV}:

$$I_{UV} = \frac{V_S}{R_{eq}}$$
$$\implies I_{UV} = \frac{V_S}{R_{UV} + R_S}$$

Now the current I_{UV} will be maximum when R_{eq} is minimum, i.e. when R_{UV} is minimum. So the minimum $I_{UV,max} = 0.1A$ will occur when $R_{UV} = R_{UV,min} = 20\Omega$. So we have:

$$I_{UV,max} = \frac{V_{S,max}}{R_{UV,min} + R_S}$$
$$\implies 0.1\text{A} = \frac{V_{S,max}}{20\Omega + 50\Omega}$$
$$\implies V_{S,max} = 7\text{V}$$

6. Resistive Touchscreens (15 points)

We have an H-shaped grid of resistors as shown in Fig. 6.1 that we would like to use as a touchscreen. Points P_{00}, P_{10}, P_{01}, P_{11}, P_{02}, and P_{12} are depicted by the black dots. Throughout this question, **measuring a voltage at a certain point means connecting the + terminal of a voltmeter to the black dot corresponding to that point and the − terminal of the voltmeter to the ground node. Note that all resistors are 1kΩ.**

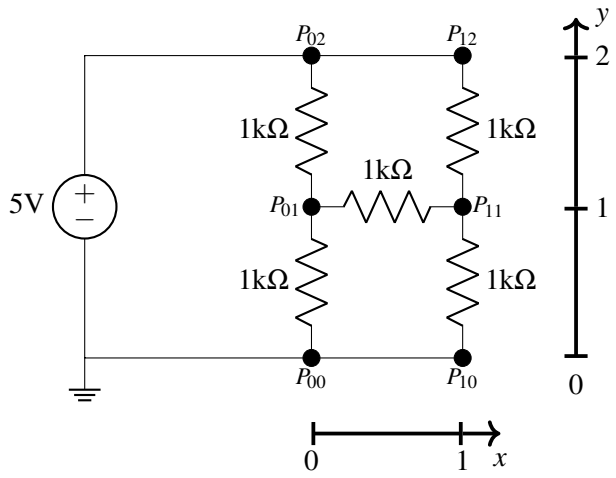


Figure 6.1: A schematic of the H-shaped resistive touchscreen.

(a) (3 points) **What are the voltages measured at each of the 6 points P_{00}, P_{10}, P_{01}, P_{11}, P_{02}, and P_{12} in Fig. 6.1? Show your work.**

Solution: P_{00} and P_{10} are connected to ground, so $P_{00} = P_{10} = 0V$. P_{02} and P_{12} are connected to the supply node, so $P_{02} = P_{12} = 5V$. Since all the resistor values are equal, we have symmetry in the circuit, and the voltages at the intermediate points P_{01} and P_{11} are the same. Therefore, there is no current flowing through the horizontal resistor, i.e. there is no voltage drop across that resistor. So we can remove it from our calculations. Doing so, we are simply left with voltage division: $P_{01} = P_{11} = 5V\frac{R}{R+R} = 2.5V$.

(b) (3 points) Can we determine the horizontal position (x-coordinate) of touch using this touchscreen in Fig. 6.1? Can we determine the vertical position (y-coordinate) of touch using this touchscreen? **For each direction, if you can, explain why. If you cannot, explain why not.** Note that the x and y axes are drawn on the figure for your convenience.

Solution: We cannot determine the horizontal position since the voltage does not change if we move between points horizontally. Specifically, $P_{00} = P_{10}$, $P_{01} = P_{11}$, and $P_{02} = P_{12}$, so the voltage does not change if we only change the x-coordinate.

We can determine determine the vertical position since the voltage changes if we move between points vertically. Specifically, $P_{00} \neq P_{01} \neq P_{02}$ and $P_{10} \neq P_{11} \neq P_{12}$, so we detect a voltage change if we change the y-coordinate.

Question continues on next page.

(c) (6 points) Your friend at Stanford proposes using a different resistive touchscreen shown in Fig. 6.2. **Note that there is a mix of** 1kΩ **and** 2kΩ **resistors, and they accidentally connected a wire between** P_{11} **and** P_{10}.

(i) Your friend claims to measure a voltage of 0V. Can you identify where the touch happened? If a point exists, write it. If multiple points exist, list them. If no points exist, say so. **Explain your answer.** Note that the measurement circuit is not shown in the figure.

(ii) Then your friend claims to measure a voltage of 2.5V. Can you identify where the touch happened? If a point exists, write it. If multiple points exist, list them. If no points exist, say so. **Explain your answer.** Note that the measurement circuit is not shown in the figure.

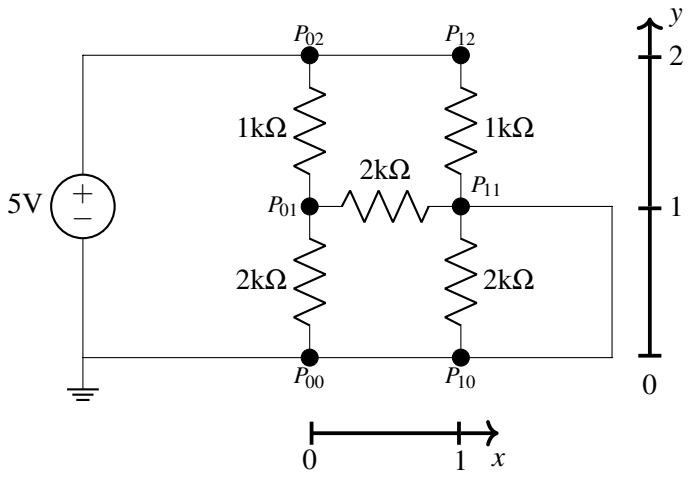
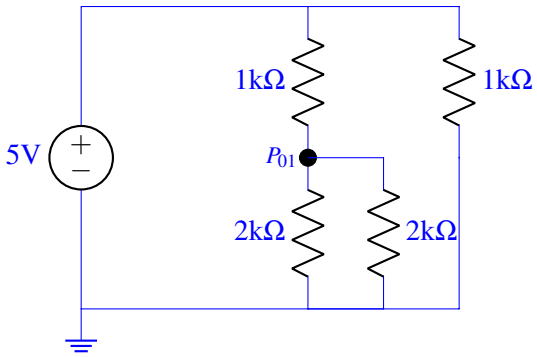


Figure 6.2: A touchscreen proposed by your Stanford friend for part (c).

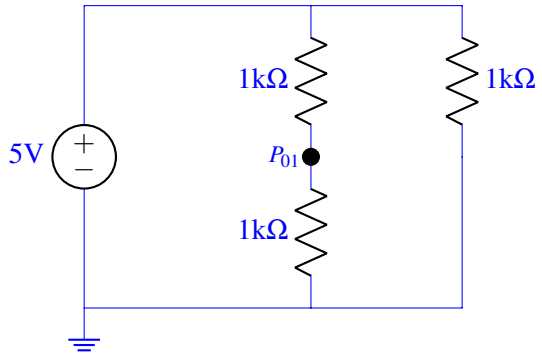
Solution:

(i) We can identify at which points the touch occurs, however we cannot identify the point uniquely since multiple points have a voltage of 0V. These points are P_{00}, P_{10}, and P_{11}, since they are all connected to ground (i.e. $P_{00} = P_{10} = P_{11} = 0V$).

(ii) We'd like to re-draw a simplified circuit. Note that the $2k\Omega$ resistor between P_{11} and P_{10} are connected to ground on both sides, so we can remove that resistor. We can also note that P_{11} is a ground node. We can re-draw the the circuit to solve for the voltage at P_{01}:



Note that we have two parallel resistors, each of $2k\Omega$, connecting P_{01} to ground. We can therefore re-draw the circuit as:



We can therefore solve for the voltage at P_{01} as a voltage division of 5V: $P_{01} = 5V \frac{1k\Omega}{1k\Omega+1k\Omega} = 2.5V$. No other point on the circuit has this voltage. Therefore, yes, we can identify where the touch happened, and we can do so uniquely as there is only one point that exists with this voltage: P_{01}.

(d) (3 points) You are now given the resistor grid shown in Fig. 6.3. Your goal is to uniquely determine the horizontal position (x-coordinate) of a touch. How would you connect your voltage source to do this? **In your answer sheet, redraw the full circuit with the voltage source terminals connected to the correct nodes.**

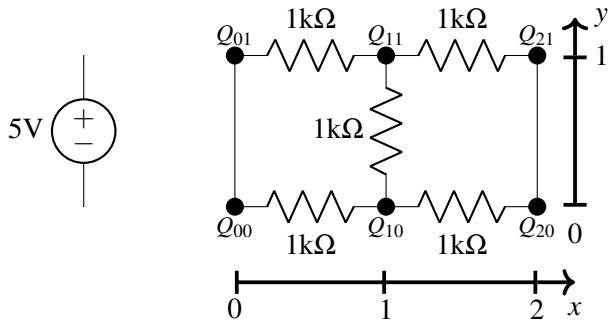
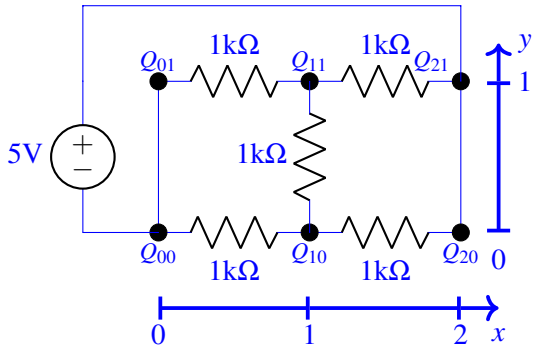


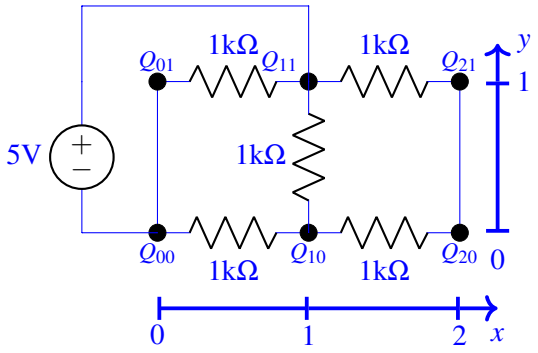
Figure 6.3: Resistor grid for part (d).

Solution:

Any connection that results in unique voltages along x-axis is valid. For this grid, this occurs when the terminals of the voltage source are connected to points with different x-coordinates. For example, in the solution below, voltages at x=2 (i.e. Q_{20} and Q_{21}) are all 5V, x=1 (i.e. Q_{10} and Q_{11}) are all 2.5V, and x=0 (i.e. Q_{00} and Q_{01}) are all 0V. Voltages in y-axis are ambiguous.



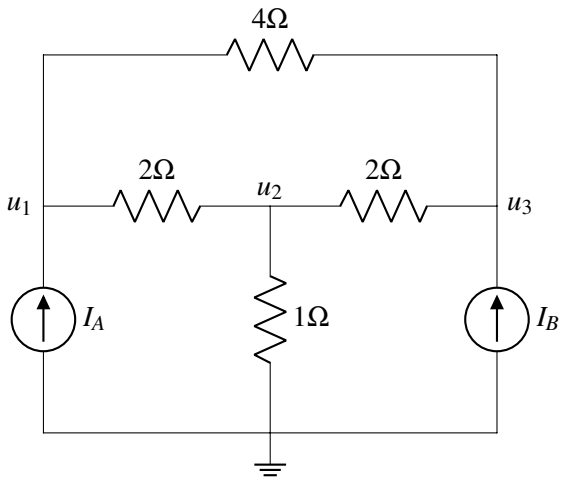
Another acceptable configuration is shown below. Voltages at x=2 (i.e. Q_{20} and Q_{21}) are all 4V and at x=0 (i.e. Q_{00} and Q_{01}) are all 0V. Voltages at x=1,y=0 (i.e. Q_{10}) is 3V and at x=1,y=1 (i.e. Q_{11}) is 5V. Note that each x-coordinate has at least one unique voltage, we we can determine the x-axis.



Any equivalent schematic of the two configurations above is acceptable.

7. Superposition (23 points)

For this question, we will analyze the circuit shown below with the two current sources of strength I_A and I_B as inputs. It may be observed that the network of resistors shown in the circuit is symmetric. We will first solve this circuit for symmetric inputs $I_A = I_B$, and then for anti-symmetric inputs $I_A = -I_B$. Using these two results, we we will solve the circuit for arbitrary inputs I_A, I_B.



(a) (6 points) Consider the following circuit in Fig. 7.1 with symmetric inputs, $I_A = I_B = 1\text{A}$. **Using superposition, solve for the node voltages at the nodes marked u_1, u_2 and u_3.** Show your work and justify your answer.

(*Hint: You should find that the node voltages u_1 and u_3 will be the same, that is, $u_1 = u_3$.*)

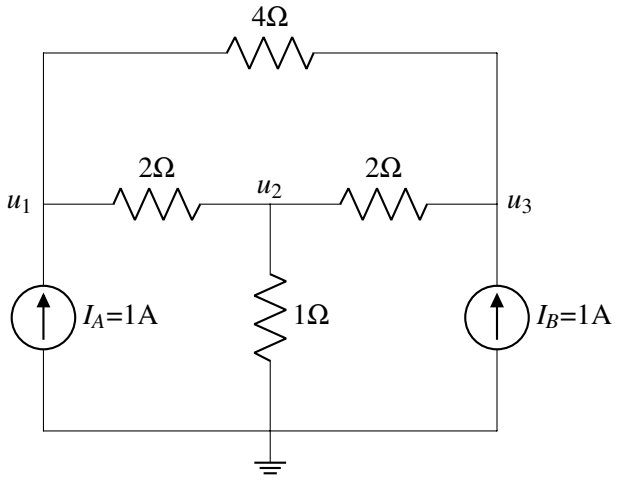
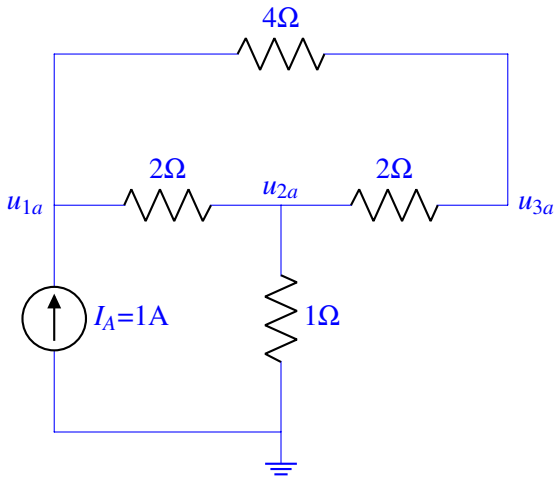


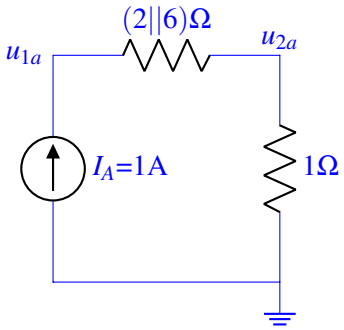
Figure 7.1: Schematic for part (a).

Solution:

Current source I_B zeroed out.



We show one solution approach using series/parallel equivalence and Ohm's law. We can redraw this circuit as follows:



Using Ohm's Law and noting that $2||6 = 1.5$ we find

$$\begin{aligned} u_{2a} &= I_A \cdot 1\,\Omega & &= 1\,\text{V} \\ u_{1a} &= u_{2a} + I_A \cdot 1.5\,\Omega & &= 2.5\,\text{V} \end{aligned}$$

To find u_{3a}, we note that the current flowing through the $4\,\Omega$ and $2\,\Omega$ resistors in the top branch clockwise is (using Ohm's Law):

$$I_{top} = \frac{(u_{1a} - u_{2a})\text{V}}{6\,\Omega} = \frac{1.5\,\text{V}}{6\,\Omega} = 0.25\,\text{A}.$$

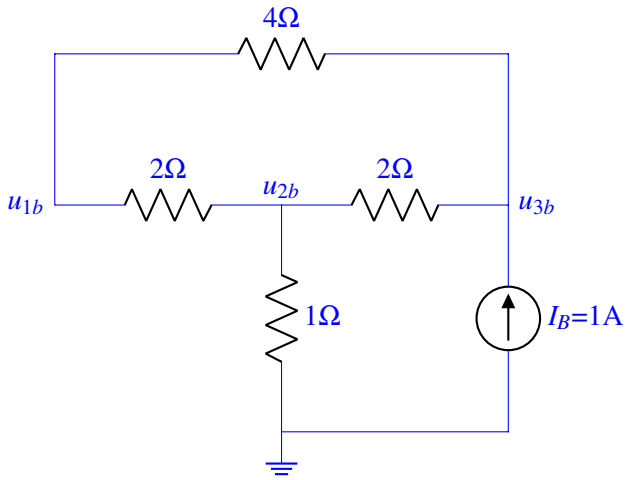
And then applying Ohm's Law again across the $4\,\Omega$ resistor, we find:

$$\begin{aligned} u_{1a} - u_{3a} &= I_{top} \cdot 4\,\Omega = 0.25\,\text{A} \cdot 4\,\Omega = 1\,\text{V} \\ \Rightarrow u_{3a} &= u_{1a} - 1\,\text{V} = 2.5\,\text{V} - 1\,\text{V} = 1.5\,\text{V}. \end{aligned}$$

So we have found:

$$\begin{aligned} u_{1a} &= 2.5\,\text{V} \\ u_{2a} &= 1\,\text{V} \\ u_{3a} &= 1.5\,\text{V}. \end{aligned}$$

Current source I_A zeroed out.



This circuit is very similar to when I_B is zeroed out, just with the relative positions of the nodes with respect to the active current source modified. So we can observe that:

$$\begin{aligned} u_{1b} = u_{3a} &= 1.5\,\text{V} \\ u_{2b} = u_{2a} &= 1\,\text{V} \\ u_{3b} = u_{1a} &= 2.5\,\text{V}. \end{aligned}$$

Both current sources I_A and I_B active. We simply find the sum to see what happens when both I_A and I_B are active.

$$\begin{aligned} u_1 = u_{1a} + u_{1b} &= 2.5\,\text{V} + 1.5\,\text{V} = 4\,\text{V} \\ u_2 = u_{2a} + u_{2b} &= 1\,\text{V} + 1\,\text{V} = 2\,\text{V} \\ u_3 = u_{3a} + u_{3b} &= 1.5\,\text{V} + 2.5\,\text{V} = 4\,\text{V}. \end{aligned}$$

(b) (6 points) Consider the following circuit in Fig. 7.2 with anti-symmetric inputs, $I_A = 1\,\text{A}$ and $I_B = -1\,\text{A}$. **Using superposition solve for the node voltages at the nodes marked u_1, u_2 and u_3.** Show your work and justify your answer.
(*Hint: You should find that $u_1 = -u_3$.*)

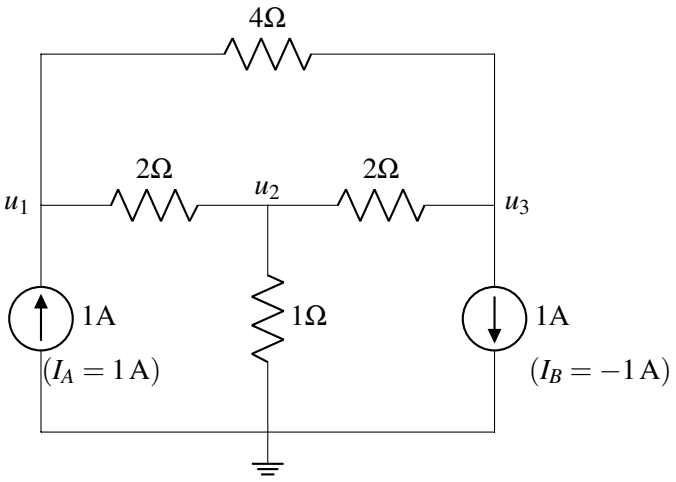
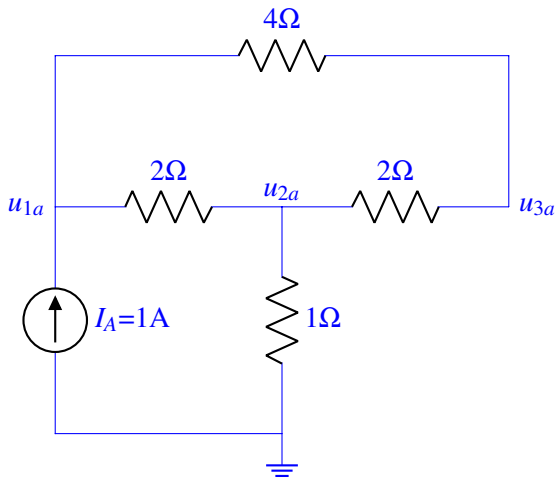


Figure 7.2: Schematic for part (b).

Solution: This solution mostly follows the same logic as in part (a). We simply need to account for the different direction of the current source I_B.

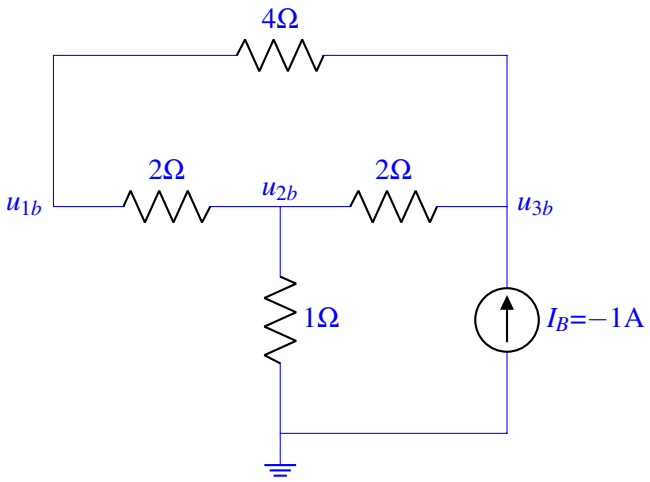
Current source I_B zeroed out.



We analyzed this same circuit in part (a) and arrive at the same results:

$$u_{1a} = 2.5\,\text{V}$$
$$u_{2a} = 1\,\text{V}$$
$$u_{3a} = 1.5\,\text{V}.$$

Current source I_A zeroed out.



As with part (a), due to symmetry, we can use the results from the case where only the current source I_A is active. However, since I_B is "flipped" relative to part (a) – i.e. the value of I_B is negative – we simply need to scale our answers from part (a) by -1. Taking the symmetry and sign information into account, we arrive at:

$$u_{1b} = -u_{3a} = -1.5\,\text{V}$$
$$u_{2b} = -u_{2a} = -1\,\text{V}$$
$$u_{3b} = -u_{1a} = -2.5\,\text{V}.$$

Both current sources I_A and I_B active. We simply find the sum to see what happens when both I_A and I_B are active.

$$\begin{aligned} u_1 &= u_{1a} + u_{1b} & &= 2.5\,\text{V} - 1.5\,\text{V} = 1\,\text{V} \\ u_2 &= u_{2a} + u_{2b} & &= 1\,\text{V} - 1\,\text{V} = 0\,\text{V} \\ u_3 &= u_{3a} + u_{3b} & &= 1.5\,\text{V} - 2.5\,\text{V} = -1\,\text{V}. \end{aligned}$$

(c) (3 points)

Now consider Fig. 7.3, where $I_A = 2\,\text{A}$ and $I_B = 2\,\text{A}$; in other words, we double the current sources from part (a). Here, as well as in the earlier circuits, the node voltages u_1, u_2 and u_3 can be represented by the vector $\vec{u} = \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix}$.

Assume that when $I_A = 1\,\text{A}$ and $I_B = 1\,\text{A}$ as part (a), the solution was given by $\vec{u} = \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix} = \begin{bmatrix} \alpha \\ \beta \\ \alpha \end{bmatrix}$.

What are the new node voltages, $\vec{u} = \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix}$, in Fig. 7.3, when $I_A = 2\,\text{A}$ and $I_B = 2\,\text{A}$? Write your answer in terms of α and β. You do not need to use any of the work from parts (a) and (b) to solve this part. Justify your answer.

Hint: It might be helpful to think of the circuit as being represented by a system of equations given as:

$$A\vec{u} = \vec{b},$$

where $\boldsymbol{A} \in \mathbb{R}^{3\times 3}$, $\vec{u} = \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix}$ *and* $\vec{b} = \begin{bmatrix} I_A \\ 0 \\ I_B \end{bmatrix}$. *However, you do not need to find* **A** *to solve this problem.*

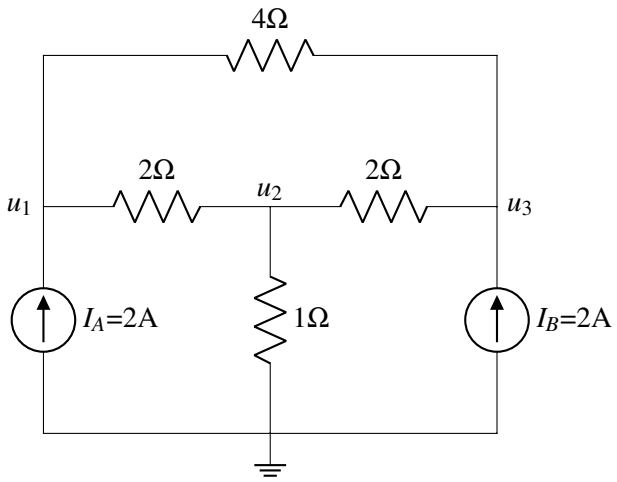


Figure 7.3: Schematic for part (c).

Solution: We were given that when $I_A = I_B = 1\text{A}$,

$$\vec{u} = \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix} = \begin{bmatrix} \alpha \\ \beta \\ \alpha \end{bmatrix} = \mathbf{A}^{-1} \begin{bmatrix} 1 \\ 0 \\ 1 \end{bmatrix}$$

Now when $I_A = I_B = 2\text{A}$ (that is, if we double the currents), then we find the following:

$$\vec{u} = \mathbf{A}^{-1} \begin{bmatrix} 2 \\ 0 \\ 2 \end{bmatrix} = 2\mathbf{A}^{-1} \begin{bmatrix} 1 \\ 0 \\ 1 \end{bmatrix} = 2 \begin{bmatrix} \alpha \\ \beta \\ \alpha \end{bmatrix}$$

(d) (8 points) Assume that when $I_A = 1\,\text{A}$ and $I_B = 1\,\text{A}$ (also known as "common mode"), the node voltages were given by $\vec{u}_{cm} = \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix} = \begin{bmatrix} \alpha \\ \beta \\ \alpha \end{bmatrix}$. Also, assume that when $I_A = 1\,\text{A}$ and $I_B = -1\,\text{A}$ (also known as "differential mode"), the node voltages were given by $\vec{u}_{dm} = \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix} = \begin{bmatrix} \gamma \\ 0 \\ -\gamma \end{bmatrix}$.

Consider the circuit shown below in Fig. 7.4, **with current sources of strengths $I_A = 6\text{A}$ and $I_B = 2\text{A}$. Find the node voltages, $\vec{u} = \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix}$, in terms of α, β and γ. You do not need to use any of the work from parts (a) and (b) to solve this part.** Show your work and justify your answer. You do not have to use to NVA to solve this part, there is an easier solution.

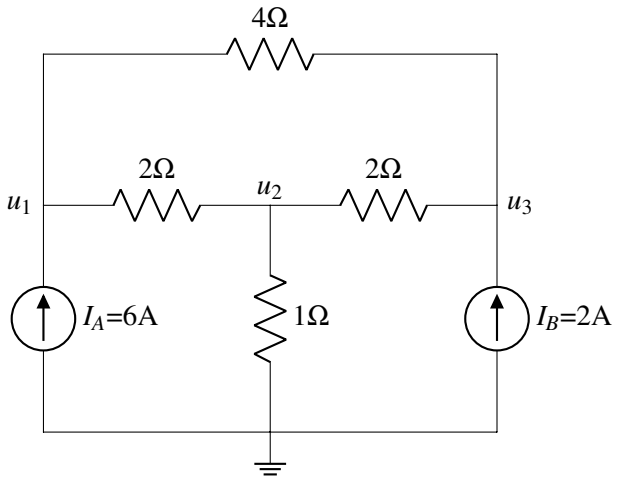


Figure 7.4: Schematic for part (d).

Hint: Again, as before, it might be helpful to think of the circuit as being represented by a system of equations given as:

$$A\vec{u} = \vec{b},$$

where $\mathbf{A} \in \mathbb{R}^{3\times 3}$, $\vec{u} = \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix}$ *and* $\vec{b} = \begin{bmatrix} I_A \\ 0 \\ I_B \end{bmatrix}$. *However, you do not need to find* $\mathbf{A}$ *to solve this problem.*

Can you write $\vec{b}$ ***as a linear combination of two vectors that correspond to the circuits you have already solved?***

Solution: We are given the following facts:

$$\vec{u_{cm}} = \mathbf{A}^{-1}\begin{bmatrix} 1 \\ 0 \\ 1 \end{bmatrix} = \begin{bmatrix} \alpha \\ \beta \\ \alpha \end{bmatrix}$$

$$\vec{u_{dm}} = \mathbf{A}^{-1}\begin{bmatrix} 1 \\ 0 \\ -1 \end{bmatrix} = \begin{bmatrix} \gamma \\ 0 \\ -\gamma \end{bmatrix}$$

Using the provided hint, we can decompose the current sources $I_A = 6\,\text{A}$ and $I_B = 2\,\text{A}$ into common and differential mode components as follows:

$$\begin{bmatrix} 6 \\ 0 \\ 2 \end{bmatrix} = \begin{bmatrix} 4 \\ 0 \\ 4 \end{bmatrix} + \begin{bmatrix} 2 \\ 0 \\ -2 \end{bmatrix}.$$

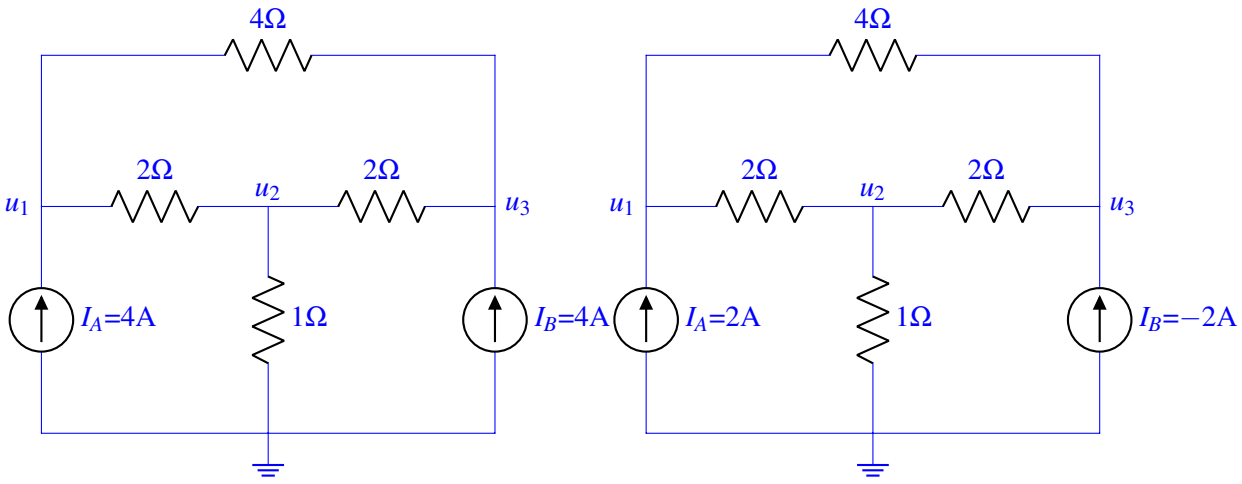
So that means that we can find the node potentials $\vec{u}$ as follows:

$$\vec{u} = \mathbf{A}^{-1}\left(\begin{bmatrix} 4 \\ 0 \\ 4 \end{bmatrix} + \begin{bmatrix} 2 \\ 0 \\ -2 \end{bmatrix}\right) = 4\mathbf{A}^{-1}\begin{bmatrix} 1 \\ 0 \\ 1 \end{bmatrix} + 2\mathbf{A}^{-1}\begin{bmatrix} 1 \\ 0 \\ -1 \end{bmatrix} = 4\vec{u_{cm}} + 2\vec{u_{dm}}$$

So we arrive at the final answer:

$$\vec{u} = \begin{bmatrix} 4\alpha + 2\gamma \\ 4\beta \\ 4\alpha - 2\gamma \end{bmatrix}.$$

Note that this corresponds to solving the following two circuits, and superposing their solutions.



8. DRAM (Dynamic Random Access Memory) Cell (28 points)

You are on a research team investigating the design of Dynamic Random Access Memory (DRAM) cells to improve their performance!

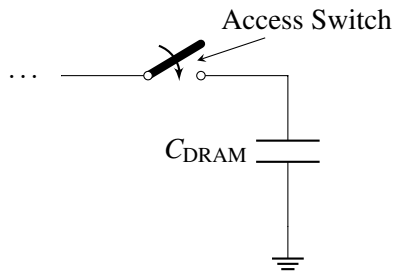


Figure 8.1: A DRAM cell consisting of an access switch and a capacitive storage element, C_{DRAM}.

(a) (3 points) You are making a capacitor with a new insulating material between the DRAM capacitor plates. The DRAM capacitor has the following properties:

- C_{DRAM} plate area, $A = 1\,\mu\text{m} \times 10\,\mu\text{m} = 10^{-11}\text{m}^2$,
- Distance between C_{DRAM} plates, $d = 40\,\text{nm} = 4 \times 10^{-8}\text{m}$,
- Permittivity of the material between the C_{DRAM} plates, $\varepsilon = 40\varepsilon_0$ F/m, where ε_0 is the permittivity of free space.

What is the capacitance of a DRAM capacitor, C_{DRAM}, in terms of ε_0 and other numerical values. Show your work. You do not need to substitute the value of ε_0.

Solution: Applying the capacitance formula, we obtain:

$$\begin{aligned} C_{DRAM} = \frac{\varepsilon A}{d} = \frac{40\varepsilon_0 A}{d} &= (40) \cdot \varepsilon_0 \cdot \frac{1\,\mu\text{m} \times 10\,\mu\text{m}}{40\,\text{nm}} \\ &= 40 \cdot \varepsilon_0 \cdot \frac{(1 \times 10^{-6})(1 \times 10^{-5})}{4 \times 10^{-8}} \\ &= 10 \cdot \varepsilon_0 \cdot (1 \times 10^{-3}) \\ &= 0.01\varepsilon_0 \end{aligned}$$

(b) (3 points) Now let's consider the case in Figure 8.2, which is the setup after the switch in Figure 8.1 is closed at time $t = 0$. When the switch is closed it starts conducting a current I_{switch}, as shown in Figure 8.2.

Assume that C_{DRAM} has no charge stored on it at $t = 0$ seconds, i.e. it has no initial charge. Let $I_{\text{switch}} = 90\,\text{pA} = 9 \times 10^{-11}\text{A}$, and $C_{\text{DRAM}} = 90\,\text{fF} = 9 \times 10^{-14}\text{F}$.

Find the value of V_{out} at $t = 1\,\text{ms} = 10^{-3}\text{s}$. Show your work.

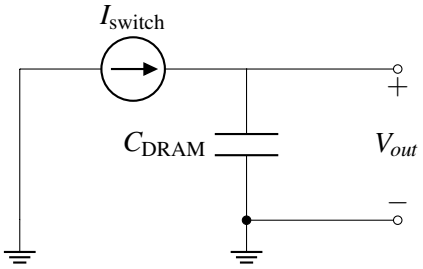
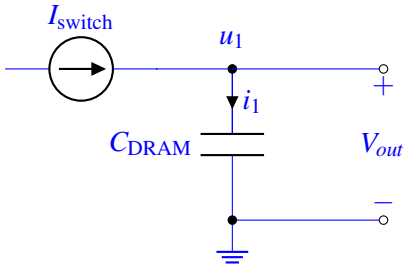


Figure 8.2: Ideal DRAM cell.

Solution:

Recall the basic capacitor-charge-voltage relationship $Q = VC$. Differentiating both sides with respect to time, we obtain $\frac{dQ}{dt} = C\frac{dV}{dt}$.



A single KCL equation at node u_1 gives $I_{\text{switch}} = i_1$, where $i_1 = \frac{dQ}{dt} = C_{DRAM}\frac{dV_{out}}{dt}$.
We integrate and solve for $V_{out}(t)$ at $t = 1\,\text{ms}$ as follows:

$$\begin{aligned} I_{\text{switch}} &= C_{DRAM}\frac{dV_{out}}{dt} \\ \implies \frac{dV_{out}}{dt} &= \frac{I_{\text{switch}}}{C_{DRAM}} \\ \int \frac{dV_{out}}{dt} &= \int_0^t \frac{I_{\text{switch}}}{C_{DRAM}} d\tau \\ \therefore V_{out}(t) &= \frac{I_{\text{switch}}}{C_{DRAM}} t + V_{out}(0) = \frac{I_{\text{switch}}}{C_{DRAM}} t \end{aligned}$$

$$\begin{aligned} V_{out}(t = 1\,\text{ms}) &= \frac{I_{\text{switch}}}{C_{\text{DRAM}}} \times 1\,\text{ms} \\ &= \frac{90\,\text{pA}}{90\,\text{fF}} \times 1\,\text{ms} \\ &= 1\,\text{V} \end{aligned}$$

(c) (5 points) Unfortunately, in reality, our access switch is not ideal and has a *parasitic capacitance* C_{switch}, which gets added to the circuit when the switch is closed. C_{switch} affects the DRAM write speed, i.e. how fast C_{DRAM} can be charged.

Find rate of change of V_{out}, i.e. $\frac{dV_{out}}{dt}$, as a function of C_{DRAM}, C_{switch} and I_{switch} for both (i) the ideal circuit circuit without C_{switch}, as shown in the left side of Figure 8.3 and (ii) the non-ideal circuit circuit with C_{switch}, as shown in the right side of Figure 8.3. Show your work.

Then compare $\frac{dV_{out}}{dt}$ values for both circuits. A larger $\frac{dV_{out}}{dt}$ means faster write speed.

Which circuit has faster write speed? Justify your answer.

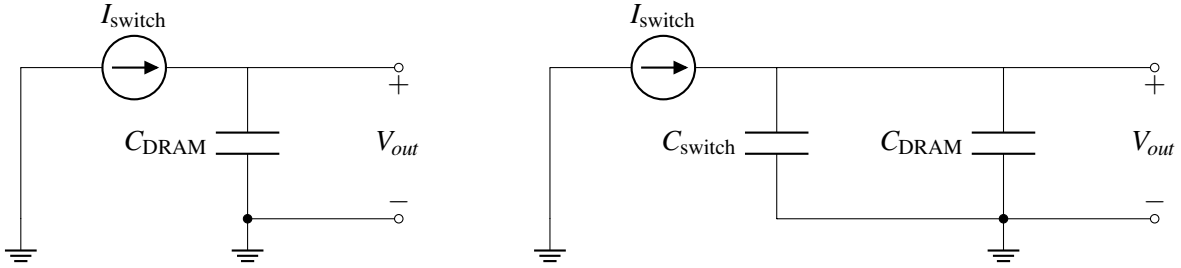


Figure 8.3: Left: Circuit without parasitic capacitance. Right: Circuit with parasitic capacitance.

Solution: We rewrite the $\frac{dV_{out}}{dt}$ from the previous parts as follows.

Without the effect of C_{switch}:

$$\frac{dV_{out}}{dt} = \frac{I_{\text{switch}}}{C_{\text{DRAM}}}$$

With the effect of switch capacitance: The equivalent capacitance is given by $C_{eq} = C_{\text{switch}} + C_{\text{DRAM}}$, since C_{switch} and C_{DRAM} are in parallel.

$$\frac{dV_{out}}{dt} = \frac{I_{\text{switch}}}{C_{\text{switch}} + C_{\text{DRAM}}}$$

Clearly, if a switch capacitance C_{switch} is present, then $\frac{dV_{out}}{dt}$ will be smaller as the fraction in the expression will have a larger denominator, hence the change in the output voltage will be slower. This implies that the write speed will be reduced if C_{switch} is present.

(d) (3 points) Assume you want to build an array of DRAM capacitors. You start by connecting two DRAM capacitors in parallel and charging them with a voltage source with value V_{DD}, as shown in Figure 8.4. Each DRAM capacitor has a capacitance value of C_{DRAM}.

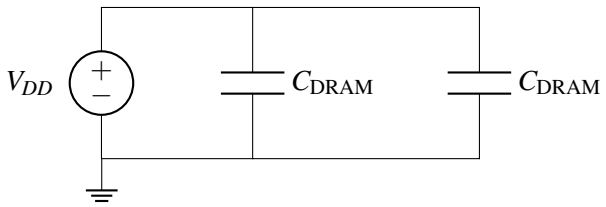


Figure 8.4: DRAM capacitors in parallel are charged.

When the capacitors are charged, how much total energy is going to be stored in both DRAM capacitors together? Show your work. Your answer should be a function of C_{DRAM} and V_{DD}.

Solution:

Here, we apply the equation $E = \frac{1}{2}CV^2$ to find the energy stored on a capacitor. So the energy stored on both capacitors is given by:

Method I: Energy stored on the capacitors are: $E_1 = C_{\text{DRAM}} \cdot (V_{DD})^2$ and $E_2 = C_{\text{DRAM}} \cdot (V_{DD})^2$. So we can find the total energy by

$$\begin{aligned} E_{tot} &= E_1 + E_2 = 2 \cdot \frac{1}{2} C_{\text{DRAM}} \cdot (V_{DD})^2 \\ &= C_{\text{DRAM}} \cdot (V_{DD})^2 \end{aligned}$$

Method II: The capacitors are in parallel, so the equivalent capacitance is given by $C_{eq} = C_{\text{DRAM}} + C_{\text{DRAM}} = 2C_{\text{DRAM}}$. The voltage across the parallel combination is V_{DD}. So the energy stored in C_{eq} is given by:

$$\begin{aligned} E_{tot} &= \frac{1}{2} C_{\text{eq}} \cdot (V_{DD})^2 \\ &= \frac{1}{2} \times 2C_{\text{DRAM}} \cdot (V_{DD})^2 \\ &= C_{\text{DRAM}} \cdot (V_{DD})^2 \end{aligned}$$

(e) (6 points) Finally! You make it to the lab! Unfortunately, you accidentally wind up introducing an additional capacitive component, C_{mistake}.

Before your grad student mentor finds out your mistake, you'd like to quickly add an additional capacitor C_{fix}, as shown in in Figure 8.5, so that the equivalent capacitance between nodes a and b becomes the same as C_{DRAM}.

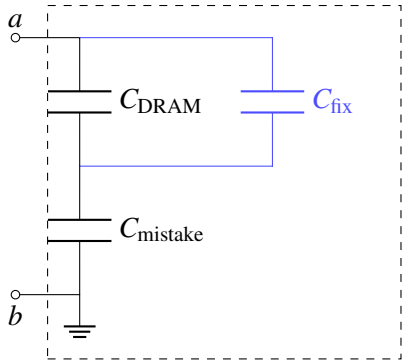


Figure 8.5: Your fabricated DRAM cell with an additional mistake capacitance, C_{mistake}, and a capacitance intentionally added to fix the mistake, C_{fix}.

Find the expression for C_{fix} so that the equivalent capacitance between nodes a and b is C_{DRAM}. Assume $C_{\text{mistake}} > C_{\text{DRAM}}$. Show your work. Your answer should be in terms of C_{DRAM} and C_{mistake}.

Hint: You can start by expressing equivalent capacitance of the network in the dashed box as a function of C_{DRAM}, C_{fix} and $C_{mistake}$.

Solution:

The key here is to recognize the series + parallel combination of all three capacitances in the picture, and to equate the result to the desired equivalent capacitance (in this case, $C_{equiv} = C_{\text{DRAM}}$). Therefore, we will set up the expression for equivalent capacitance C_{equiv} and rearrange to solve for C_{fix}.

$$C_{equiv} = \left(\frac{1}{C_{\text{mistake}}} + \frac{1}{C_{\text{DRAM}} + C_{\text{fix}}}\right)^{-1}$$
$$\implies C_{\text{DRAM}} = \left(\frac{1}{C_{\text{mistake}}} + \frac{1}{C_{\text{DRAM}} + C_{\text{fix}}}\right)^{-1}$$

Rearranging and solving for C_{fix}:

$$C_{\text{DRAM}} = \frac{(C_{\text{DRAM}} + C_{\text{fix}}) \cdot C_{\text{mistake}}}{C_{\text{DRAM}} + C_{\text{fix}} + C_{\text{mistake}}}$$
$$C_{\text{DRAM}}C_{\text{mistake}} + C_{\text{DRAM}}^2 + C_{\text{DRAM}}C_{\text{fix}} = C_{\text{DRAM}}C_{\text{mistake}} + C_{\text{fix}}C_{\text{mistake}}$$
$$C_{\text{DRAM}}^2 = C_{\text{fix}}(C_{\text{mistake}} - C_{\text{DRAM}})$$
$$C_{\text{fix}} = \frac{C_{\text{DRAM}}^2}{C_{\text{mistake}} - C_{\text{DRAM}}}$$

Based on this final expression for C_{fix}, it is clear that we will be able to adjust for the additional mistake capacitance since $C_{\text{mistake}} > C_{\text{DRAM}}$, hence the expression of C_{fix} will give us a positive value. (Note that we consider resistance and capacitance to be non-negative quantities for this class.)

(f) (8 points) You made two DRAM cells, but due to some unfortunate error you end up with: $C_1 = \frac{C_{\text{DRAM}}}{4}$ and $C_2 = C_{\text{DRAM}}$. You charge up C_1 to test it and have placed initial voltage $V_1(0) = V_{DD}$ on it. The second capacitor C_2 has not been charged yet and the initial voltage on C_2 is $V_2(0) = 0\,\text{V}$.

Now you close S_2 at $t = 0$ so that C_2 can share charge from C_1, while S_1 remains closed, as in Fig. 8.6. **Find V_1 and V_2 at steady-state after switch S_2 is closed and switch S_1 remains closed. Your final answer should be in terms of C_{DRAM} and V_{DD}. Show your work and justify your answer.**

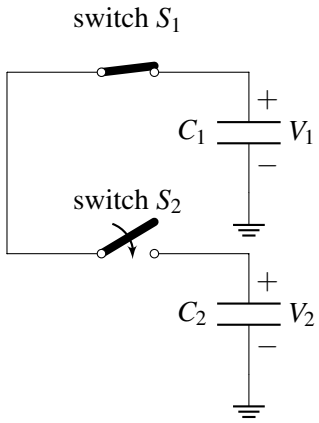


Figure 8.6: Two DRAM cells in parallel. Switch S_1 is closed (can be thought of as a wire), and switch S_2 is closing.

Solution:

We will apply the property of charge conservation to solve for the final voltage on the two DRAM capacitors. Prior to switch S_2 closing, the initial charges on both capacitors are given by:

$$Q_{1,i} = C_1 V_{DD}; \quad Q_{2,i} = C_2(0\,\text{V}). \tag{1}$$

We can write the following equation of charge conservation:

$$Q_{1,i} + Q_{2,i} = = Q_{1,f} + Q_{2,f} \tag{2}$$
$$C_1 V_{DD} + C_2(0\,\text{V}) = Q_{1,f} + Q_{2,f} \tag{3}$$
$$\implies \frac{C_{\text{DRAM}}}{4} V_{DD} = Q_{1,f} + Q_{2,f} \tag{4}$$

where $Q_{1,f}$ represents the final charge on C_1 and $Q_{2,f}$ represents the final charge on C_2 after switch S_2 is closed.

After switch S_2 is closed, notice that both capacitors are then in *parallel*. This means that the final steady stage voltage on both should be equal to one another, i.e. $V_1 = V_2$. We can therefore write a second equation based on this condition:

$$V_1 = \frac{Q_{1,f}}{C_1} = V_2 = \frac{Q_{2,f}}{C_2} \tag{5}$$
$$\implies Q_{1,f} = C_1 V_1 = \frac{C_{\text{DRAM}}}{4} V_1 \tag{6}$$
$$Q_{2,f} = C_2 V_2 = C_{\text{DRAM}} V_2 \tag{7}$$

Let's now substitute in the results of equations (6) and (7) into equation (4), keeping in mind that $V_1 = V_2$ after S_2 is closed. We can solve for V_1 first:

$$\frac{C_{\text{DRAM}}}{4} V_{DD} = \frac{C_{\text{DRAM}}}{4} V_1 + C_{\text{DRAM}} V_2 \tag{8}$$

$$\implies \frac{C_{\text{DRAM}}}{4} V_{DD} = \frac{C_{\text{DRAM}}}{4} V_1 + C_{\text{DRAM}} V_1 \tag{9}$$

$$\implies \frac{C_{\text{DRAM}}}{4} V_{DD} = \frac{5}{4} C_{\text{DRAM}} V_1 \tag{10}$$

$$\implies V_1 = \frac{V_{DD}}{5}. \tag{11}$$

Since $V_1 = V_2$ we have:

$$V_2 = \frac{V_{DD}}{5}.$$