EECS 16A Designing Information Devices and Systems I
Spring 2020 Midterm 2 Instructions

Read the following instructions before the exam.

Format & How to Submit Answers

There are 13 problems (4 introductory questions, and 9 exam questions, comprising 34 subparts total) of varying numbers of points. The problems are of varying difficulty, so pace yourself accordingly and avoid spending too much time on any one question until you have gotten all of the other points you can. Don't get bogged down in calculations; if you are having trouble with one problem, there may be easier points available later in the exam!

All answers will be submitted to the Gradescope "Midterm 2" Assignment (`https://www.gradescope.com/courses/83747/assignments/427941`). All questions, except introductory questions, are multiple choice and are **worth 4 points each**. **There are 125 points possible on the exam, but your final score will be taken out of 100 points**. This means that a score of 75/125, normally 60%, will be bumped up to 75/100, or 75%. You cannot score more than 100% on this exam.

Partial credit may be given for certain incorrect answer choices for some problems. There is no penalty for incorrect answers.

Post any content or clarifying questions privately on Piazza. There will be no exam clarifications; if we find a bug on the exam, that sub-question will be omitted from grading.

Timing & Penalties

You have 120 minutes for the exam, with a 5 minute grace period. After the 5 minute grace period ends, exam scores will be penalized exponentially as follows: an exam that is submitted N minutes after the end of the grace period will lose 2^N points. **The exam will become available at your personalized link at 8:10 pm PT; the grace period will expire at 10:15 pm PT.** If your submission is timestamped at 10:16 pm PT, you will lose 2 points; if it is timestamped at 10:18 pm PT, you will lose 8 points.

We will count the latest time at which you submit any question as your exam timestamp. Do NOT edit or resubmit your answers after the deadline. We recommend having all of your answers input and submitted by 10:10 pm; it is your responsibility to submit the exam on time.

If you cannot access your exam at your link by 8:15 pm, please email eecs16a@berkeley.edu. If you are having technical difficulties submitting your exam, you can email your answers (either typed or scanned) to eecs16a@berkeley.edu.

Academic Honesty

This is an open-note, open-book, open-internet, and **closed-neighbor** exam. You may use any calculator or calculation software that you wish, including Wolfram-Alpha and Mathematica. **No collaboration is allowed, and do not attempt to cheat in any way. Cheating will not be tolerated.**

We have zero tolerance against violation of the Berkeley Honor Code. Given supporting evidence of cheating, we reserve the right to automatically fail all students involved and report the instance to the student conduct committee. Feel free to report suspicious activity through this form. (`https://forms.gle/akhBsHVr1WG29Ufg9`).

Our advice to you: if you can't solve a particular problem, move on to another, or state and solve a simpler one that captures at least some of its essence. You will perhaps find yourself on a path to the solution.

Good luck!

EECS 16A Designing Information Devices and Systems I
Spring 2020 Midterm 2

1. **Pledge of Academic Integrity (2 points)**
   By my honor, I affirm that:

   (1) this document, which I will produce for the evaluation of my performance, will reflect my original, bona fide work;

   (2) as a member of the UC Berkeley community, I have acted and will act with honesty, integrity, and respect for others;

   (3) I have not violated—nor aided or abetted anyone else to violate—nor will I—the instructions for this exam given by the course staff, including, but not limited to, those on the cover page of this document; and

   (4) I have not committed, nor will I commit, any act that violates—nor aided or abetted anyone else to violate—the UC Berkeley Code of Student Conduct.

   Write your name and the current date as an acknowledgement of the above. (See Gradescope)

2. **Administrivia (1 point)**
   I know that I will lose 2^n points for every n minutes I submit after the exam submission grace period is over.

   For example, if the exam becomes available at my personalized link at 8:10 p.m. PT; the grace period will expire at 10:15 p.m. PT. If my submission is timestamped at 10:16 p.m. PT, I will lose 2 points; if it is timestamped at 10:18 p.m. PT, I will lose 8 points.

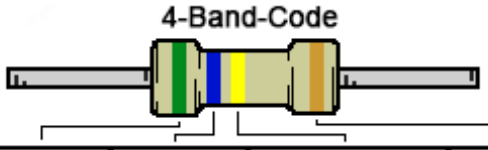
   ○ Yes

3. **What is one of your hobbies? (1 point)**

4. **Tell us about something you're proud of this semester. (1 point)**

5. Fun with Resistors (12 points)

(a) Your partner hands you an old beat-up four-band resistor, $R_{mystery}$ where the second band has been worn off with time. You can see that the first band is **orange**, the third band is **yellow**, and the fourth band is **gold**. Which of the following ranges does the nominal value of this unknown resistance, $R_{mystery}$, fall in? Do not consider the range allowed by the tolerance.
There is a resistor color code chart below:



COLOR	1ST BAND	2ND BAND	MULTIPLIER	TOLERANCE
Black	0	0	1Ω	
Brown	1	1	10Ω	± 1% (F)
Red	2	2	100Ω	± 2% (G)
Orange	3	3	1KΩ	
Yellow	4	4	10KΩ	
Green	5	5	100KΩ	± 0.5% (D)
Blue	6	6	1MΩ	± 0.25% (C)
Violet	7	7	10MΩ	± 0.10% (B)
Grey	8	8	100MΩ	± 0.05%
White	9	9	1GΩ	
Gold			0.1Ω	± 5% (J)
Silver			0.01Ω	± 10% (K)

Figure 1: Resistor Color Chart.

Figure 2: $R_{mystery}$.

Solution:

From the chart, we see that the mystery resistor will be of the form: $3k \times 10\,\text{k}\Omega$, where k represents a digit. Therefore, we have:

$$300\ k\Omega \leq R_{mystery} \leq 390\ k\Omega$$

For the rest of this problem, assume that you have an **infinite supply** of 5Ω and 20Ω resistors.

(b) What is the minimum number of resistors you need to create a resistor network with an equivalent resistance equal to 4Ω?

Solution:

We note that $4\Omega = 5\Omega||20\Omega$. Therefore, we need **2** resistors.

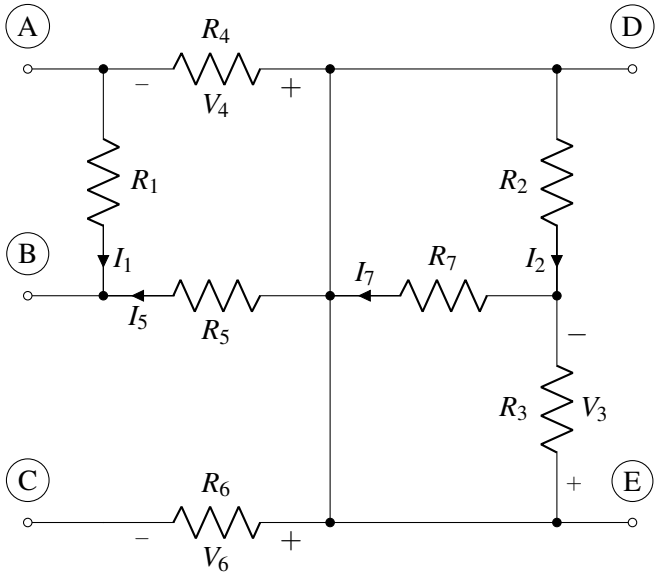
(c) What is the minimum number of resistors you need to create a resistor network with an equivalent resistance equal to 9Ω?

Solution:

We note that $9\Omega = 5\Omega + 5\Omega||20\Omega$. Therefore, we need **3** resistors.

6. (16 points) Analyzing a Resistor Network

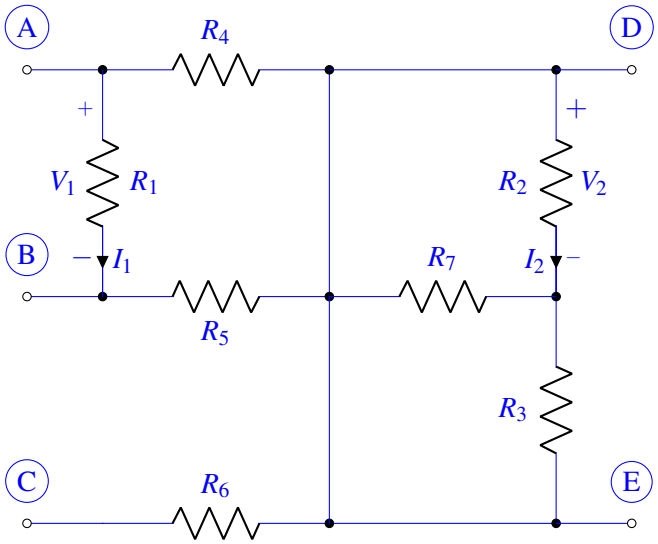
Consider the following circuit.



(a) Each branch in the circuit is either labelled with a branch current direction or a branch voltage polarity, but not both. For the branches corresponding to R_1 and R_2, label the missing quantity according to passive sign convention.

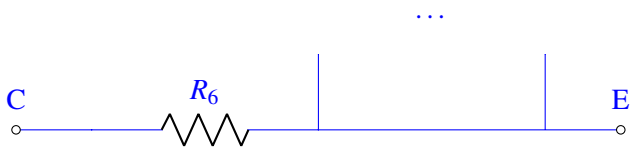
Solution:

We note that in passive sign convention that the current flows from the positive branch polarity to the negative branch polarity. Thus, R_1 and R_2 should be labelled as:

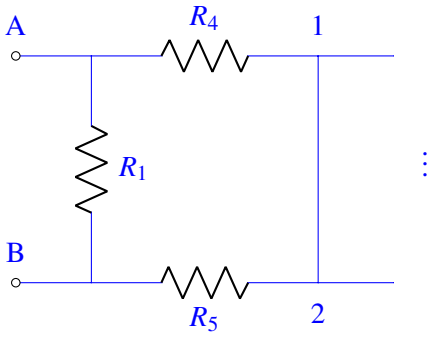


(b) All resistors have a value of $72R$. Find the equivalent resistance between terminals C and E, R_{CE}, in terms of R, and also find the equivalent resistance between terminals A and B, R_{AB}, in terms of R. Assume that when finding the equivalent resistance between two terminals, all the other terminals are left as is, with nothing attached to them.

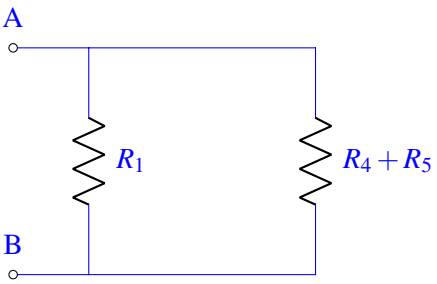
Solution: $R_{CE} = 72R$, as there is a short from the side of resistor R_5 to the terminal E. Whatever is parallel to that short will not matter: $0\Omega || R_{anything} = 0\Omega$.



$R_{AB} = \frac{2}{3}(72R) = 48R$. To see that this is the case, do the following reductions:
Whatever is parallel to the short between 1 and 2 will not matter, for the same reasoning as before:

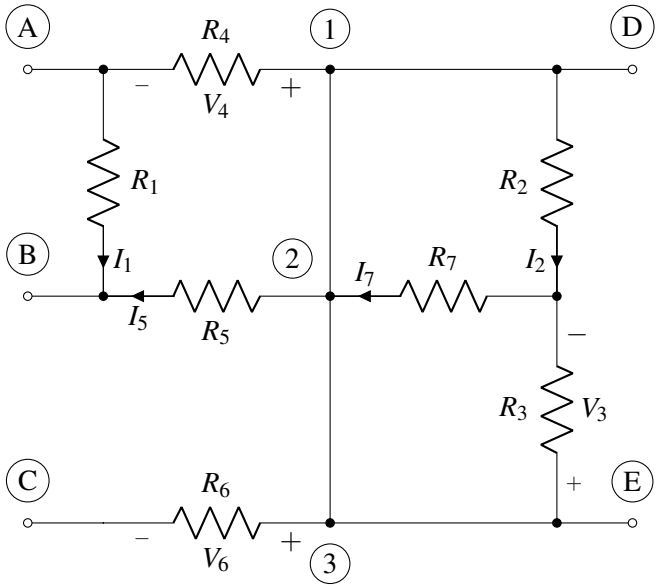


So we can combine series resistors R_4 and R_5:



This leaves us with $R_{AB} = R_1 || (R_4 + R_5) = 72R || 144R = 48R$.

The circuit has been duplicated again here for your convenience for parts (c) and (d). The labels (1), (2), and (3) correspond to locations in the circuit schematic.



(c) Write the KVL equation equation for the loop (A)-(1)-(D)-(E)-(3)-(2)-(B)-(A) in terms of V_1 to V_7 using passive sign convention.

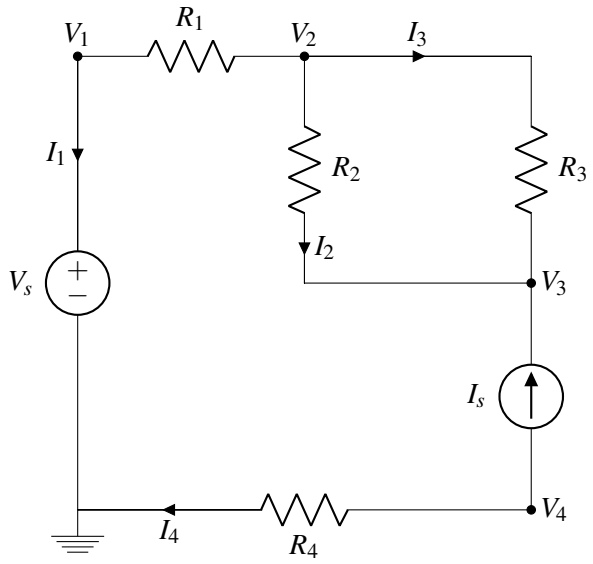
Solution: $0 = +V_4 - V_2 + V_3 - V_5 + V_1$.

(d) Write the KCL equation for the node associated with terminal (E) in terms of the currents I_1 to I_7 using passive sign convention.

Solution: $0 = -I_2 - I_3 - I_4 - I_5 - I_6 + I_7$

7. (8 points) Linearity of circuits

Consider the following circuit with resistor values $R_1 = 9\Omega$, $R_2 = 1\Omega$, $R_3 = 6\Omega$, and $R_4 = 4\Omega$.



(a) In order to analyze this circuit, Nirmaan wrote down a system of equations for the circuit and then cast it into matrix-vector form. However, some of the entries of the matrix were smudged, and Nirmaan needs your help filling in the missing entries. Fill in the missing values in the matrix below. *Hint: Rows (2)-(4) correspond to KCL equations. Rows (5) - (8) correspond to Ohm's Law equations.*

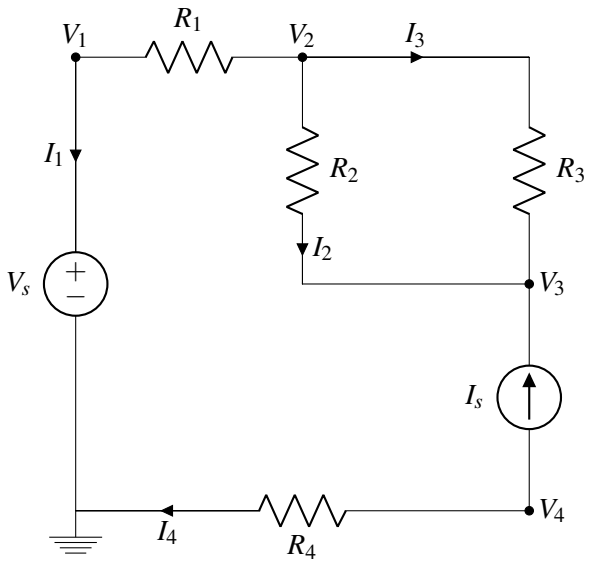
$$\begin{bmatrix} 0 & 0 & 0 & 0 & (C_1) & 0 & 0 & 0 \\ 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & (C_2) & (C_2) & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ (C_3) & 0 & 0 & 0 & 1 & -1 & 0 & 0 \\ 0 & (C_4) & 0 & 0 & 0 & -1 & 1 & 0 \\ 0 & 0 & (C_5) & 0 & 0 & -1 & 1 & 0 \\ 0 & 0 & 0 & (C_6) & 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = \begin{bmatrix} V_s \\ 0 \\ I_s \\ -I_s \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

Solution:

Working our way through each row:

- **Row 1:** This row maps to the equation: $C_1 V_1 = V_s$. Since $V_1 = V_s$, $C_1 = 1$.
- **Row 3:** This row maps to the equation: $C_2(I_2 + I_3) = I_s$. By KCL at the node labelled by V_3, $I_s + I_1 + I_2 = 0$. That implies that $C_2 = -1$.
- **Row 5:** This row maps to the equation: $C_3 I_1 + V_1 - V_2 - 0$. As given in the hint, this row corresponds to an Ohm's Law equation. We note that I_1 is the current flowing through R_1. Ohm's law for R_1, following passive sign convention, is $V_2 - V_1 = I_1 R_1$. Thus, $C_3 = R_1$.
- **Rows 6-8:** Similar analysis as row 5. We get that $C_4 = R_2$, $C_5 = R_3$, and $C_6 = R_4$.

(b) Now consider the same circuit, except with different resistor values.



When $V_s = 15V$, $I_s = -8A$, and $R_1 = R_2 = R_3 = R_4 = 4\,\Omega$, we have that the solution to the above system of equations is the vector:

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = \begin{bmatrix} -8 \\ 4 \\ 4 \\ 8 \\ 15 \\ -17 \\ -33 \\ 32 \end{bmatrix}$$

What is the power dissipated across the voltage source, V_s? What is the power dissipated across the resistor R_3?

Solution:

The power dissipated across the voltage source is given by:

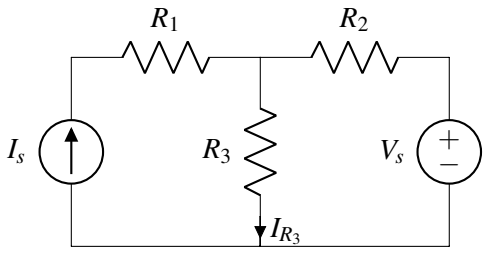
$$P_{V_s} = I_1 V_s = (-8\,\text{A})(15\,\text{V}) = -120\,\text{W}$$

The power dissipated across R_3 is given by:

$$P_{R_3} = I_3(V_2 - V_3) = (4\,\text{A})(16\,\text{V}) = 64\,\text{W}$$

8. Superposition (12 points)

Consider the following circuit:



Let $R_1 = 15.0\Omega$, $R_2 = 25.0\Omega$, $R_3 = 35.0\Omega$, $I_s = 1.0\text{A}$, and $V_s = 4.0\text{V}$.

(a) With the current source turned on and the voltage source turned off, find the current I_{R_3}.

Solution:

We note that that I_s is split between R_2 and R_3 and therefore we can use the current divider relation (here the notation I_{R_3,I_s} represents the current across R_3 with only I_s turned on.):

$$I_{R_3,I_s} = \frac{I_s R_2}{R_2 + R_3} = \frac{(1\,\text{A})(25\Omega)}{25\Omega + 35\Omega} = 0.42\,\text{A}.$$

(b) With the voltage source turned on and the current source turned off, find the voltage drop across R_3, V_{R_3}.

Solution:

We note that when the current source is turn off it becomes an open circuit. Thus, we are left with a voltage divider.

$$V_{R_3,V_s} = \frac{V_s R_3}{R_2 + R_3} = \frac{(4\,\text{V})(35\Omega)}{25\Omega + 35\Omega} = 2.33\,\text{V}$$

(c) With both sources turned on, find the power dissipated across R_3.

Solution:

Note that since power is not a linear quantity, you **cannot** add the powers dissipated through the resistor with only one source on.

Thus, we first find the missing quantities. The voltage drop across R_3 when the current source is on is given by:

$$V_{R_3,I_s} = I_{R_3,I_s} R_3 = \frac{I_s R_2 R_3}{R_2 + R_3}$$
$$I_{R_3,V_s} = \frac{V_{R_3,V_s}}{R_3} = \frac{V_s}{R_2 + R_3}$$

Thus, we have:

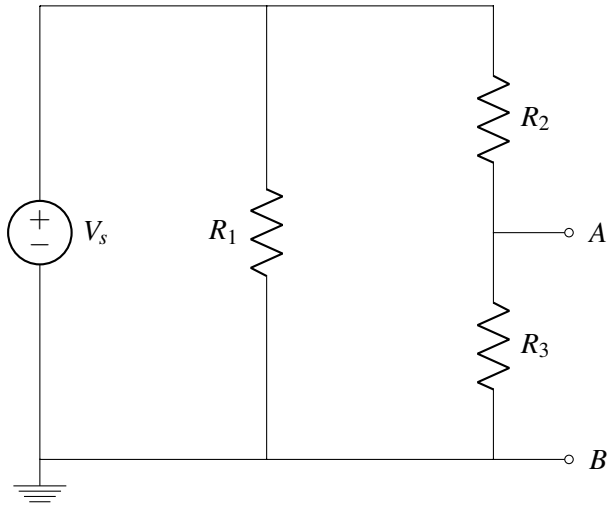
$$V_{R_3} = V_{R_3,V_s} + V_{R_3,I_s} = \frac{V_s R_3 + I_s R_2 R_3}{R_2 + R_3}$$
$$I_{R_3} = I_{R_3,V_s} + I_{R_3,I_s} = \frac{I_s R_2 + V_s}{R_2 + R_3}$$

Thus, the power dissipated is:

$$P_{R_3} = I_{R_3} V_{R_3} = \frac{R_3 (I_s R_2 + V_s)^2}{(R_2 + R_3)^2} = \frac{(35\Omega)((1\,\text{A})(25\Omega) + 4\,\text{V})^2}{(25\Omega + 35\Omega)^2} = 8.18\,\text{W}$$

9. Thévenin Equivalence (12 points)

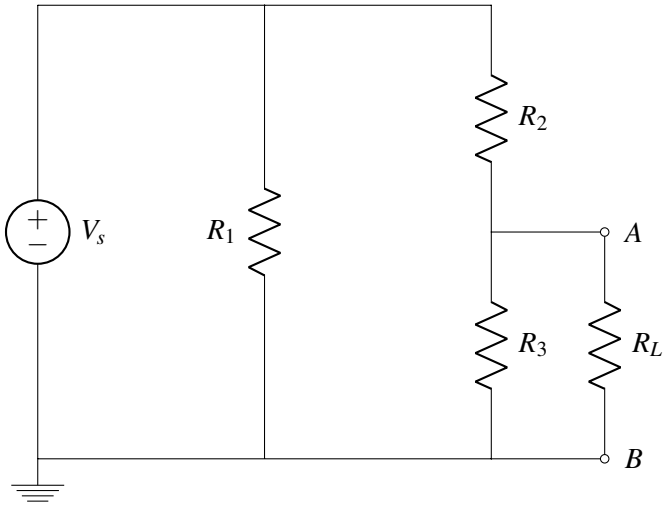
(a) Find the Thévenin resistance R_{th} of the circuit shown below, with respect to its terminals A and B. Assume that $R_1 = 4R$, $R_2 = R$ and $R_3 = 9R$.



Solution: To find the Thévenin resistance, we null out the voltage source (which shorts out R_1) and find the equivalent resistance which is simply:

$$R_{th} = R_2 \parallel R_3 = \frac{(9R)(R)}{9R+R} = \frac{9}{10}R$$

(b) Now a load resistor, $R_L = 9R$, is connected across terminals A and B as shown in the circuit below. Find the supply voltage, V_s, such that 1 mW is dissipated across the load resistor. Let $R = 36\text{k}\Omega$.

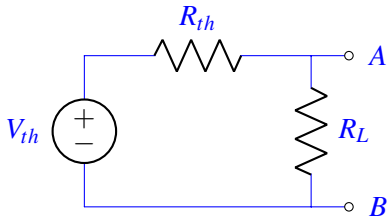


Solution:

To help simplify the analysis, we replace the circuit by its Thévenin equivalent circuit. In order to do so, we first need to finds the Thévenin voltage. That is simply the open circuit voltage, V_{AB}, in the original circuit, which is simply a voltage divider:

$$V_{th} = \frac{R_3}{R_2+R_3}V_s = \frac{9R}{9R+R}V_s = 0.9V_s$$

Thus, the circuit can be simplified to:



The power through the load resistor is given by:

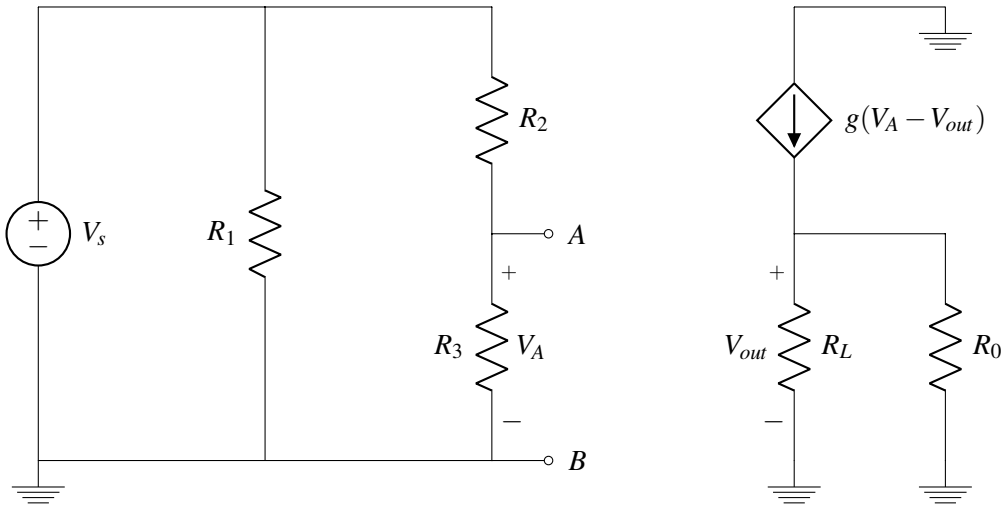
$$P_{R_L} = \left(\frac{V_{th}}{R_L + R_{th}}\right)^2 R_L = \left(\frac{\frac{R_3}{R_2+R_3}V_s}{R_L + (R_2||R_3)}\right)^2 R_L$$

Solving for V_s, we get:

$$V_s = \sqrt{P_{R_L}}\frac{R_L + (R_2||R_3)}{\sqrt{R_L}\frac{R_3}{R_2+R_3}} = \sqrt{P_{R_L}}\frac{9.9R}{3\sqrt{R}(0.9)} = \frac{11}{3}\sqrt{P_{R_L}R}$$

Substituting numerical values, we get, $V_s = \frac{11}{3}\sqrt{(1\,\text{mW})(36\,\text{k}\Omega)} = 22\,\text{V}$.

(c) We modify the circuit as shown below:



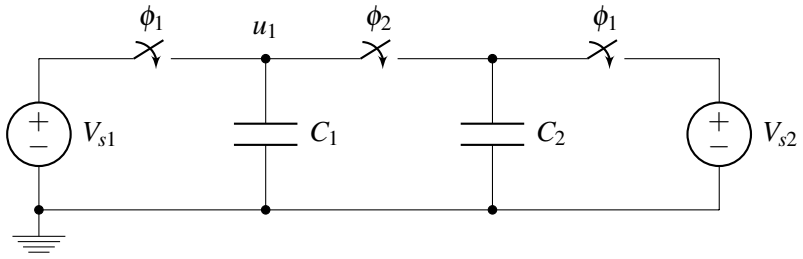
Find a symbolic expression for V_{out} as a function of V_s.

Solution:

We note that V_{AB} simply equals $V_{th} = \frac{R_3}{R_3+R_2}V_s = 0.9V_s$. Then, noting that R_0 and R_L are in parallel, we have that $V_{out} = g(0.9V_s - V_{out})(R_0 \parallel R_L)$. Solving for V_{out}, we get:

$$V_{out} = 0.9V_s\frac{gR_L \parallel R_0}{1 + gR_L \parallel R_0}$$

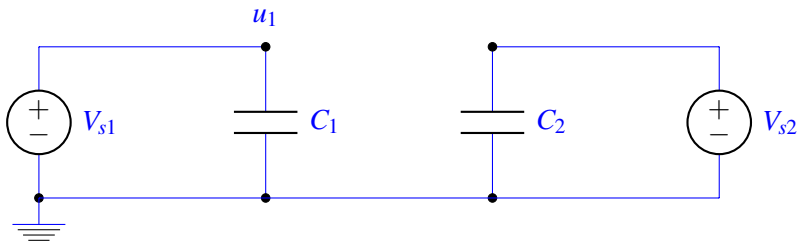
10. Capacitive Charge Sharing (16 points)



(a) Consider the circuit above with $C_1 = 6\mu F$ and $C_2 = 9\mu F$. Suppose that initially the ϕ_1 switches are closed and the ϕ_2 switch is open such that C_1 and C_2 are charged through the corresponding voltage sources $V_{s1} = 6V$ and $V_{s2} = 17V$. How much charge is on C_1 and C_2?

Solution:

In phase 1, the circuit is given by:



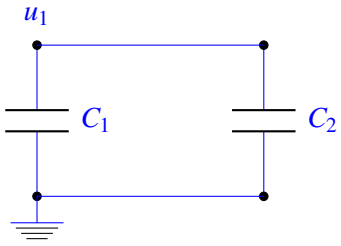
Since the charge on a capacitor plate is given by $Q = CV$, we have:

$$q_1 = C_1 V_{s1} = (6\mu F)(6\,V) = 36\mu C$$
$$q_2 = C_2 V_{s2} = (9\mu F)(17\,V) = 153\mu C$$

(b) Now suppose that some time later, the ϕ_1 switches open and the ϕ_2 switch closes. What is the value of voltage u_1 at steady state?

Solution:

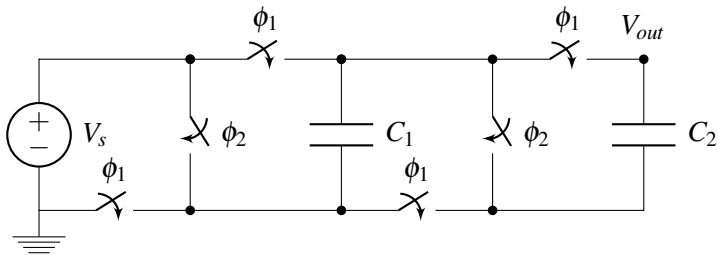
The circuit in phase 2 is given by:



The total charge on capacitors C_1 and C_2 will be conserved after switch ϕ_1 is opened. That charge is $Q_{tot} = q_1 + q_2$. Also note that during phase 2 the capacitors are connected in parallel so they will both have $V_{C1} = V_{C2} = u_1$. Therefore,

$$Q_{tot} = C_1 V_{s1} + C_2 V_{s2}$$
$$u_1 = \frac{Q_{tot}}{C_1 + C_2} = \frac{C_1 V_{s1} + C_2 V_{s2}}{C_1 + C_2} = \frac{(6\mu F)(6\,V) + (9\mu F)(17\,V)}{6\mu F + 9\mu F} = 12.6\,V$$

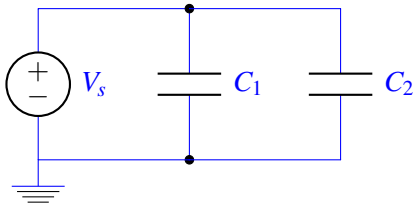
(c) Now let's look at the following circuit. Once again, let $C_1 = 6\,\mu\text{F}$ and $C_2 = 9\,\mu\text{F}$. Let $V_s = 7\text{V}$.



Suppose that initially the ϕ_1 switches are closed and the ϕ_2 switches are open. How much charge is on C_1 and C_2?

Solution:

Rewriting the circuit in phase 1 we have:

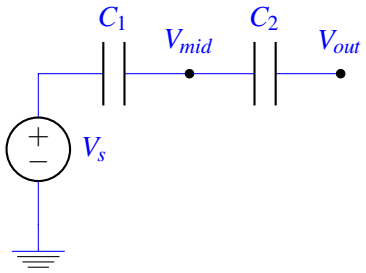


Therefore the charge on each capacitor is simply:

$$q_1 = C_1 V_s = (6\,\mu\text{F})(7\,\text{V}) = 42\,\mu\text{C}$$
$$q_2 = C_2 V_s = (9\,\mu\text{F})(7\,\text{V}) = 63\,\mu\text{C}$$

(d) Now suppose that some time later, the ϕ_1 switches open and the ϕ_2 switches close. What is the value of voltage V_{out} at steady state?

Solution: Rewriting the circuit in phase 2 we have:



Notice that the charge will be conserved on nodes V_{out}, V_{mid}.

Identifying all the capacitor plates that are connected on those nodes during phase 1 and calculating the charge onto them in phase 1 we have that:

Node V_{mid}:

$$Q^{\phi_1}_{V_{mid}} = (V_s - 0)C_1 - (V_s - 0)C_2$$

Node V_{out}:

$$Q^{\phi_1}_{V_{out}} = (V_s - 0)C_2$$

Looking at phase 2 and calculating the charge onto the same nodes we have: Node V_{mid}:

$$Q^{\phi_2}_{V_{mid}} = (V_{mid} - V_s)C_1 - (V_{out} - V_{mid})C_2$$

Node V_{out}:

$$Q^{\phi_2}_{V_{out}} = (V_{out} - V_{mid})C_2$$

Equating the charge on the corresponding plates for phases 1 and 2 we get a 2x2 system of linear equations:

$$V_sC_1 - V_sC_2 = (V_{mid} - V_s)C_1 - (V_{out} - V_{mid})C_2 \quad (1)$$

$$V_sC_2 = (V_{out} - V_{mid})C_2 \quad (2)$$

Substituting (2) into (1) yields:

$$V_sC_1 - V_sC_2 = (V_{mid} - V_s)C_1 - V_sC_2$$

$$V_{mid} = 2V_s$$

Finally substituting V_{mid} into (2):

$$V_{out} = 3V_s = 21\,\text{V}$$

Which means that we managed to create $3V_s$ with a voltage source of only V_s!

11. Flash Memory (16 points)

Solid state drives depend on charge to store information. In several integrated circuit applications, the charge is stored on a floating node of a transistor. A cartoon of such a transistor and its corresponding circuit model are shown below. *Note: You do not need to understand transistors in order to do this problem.*

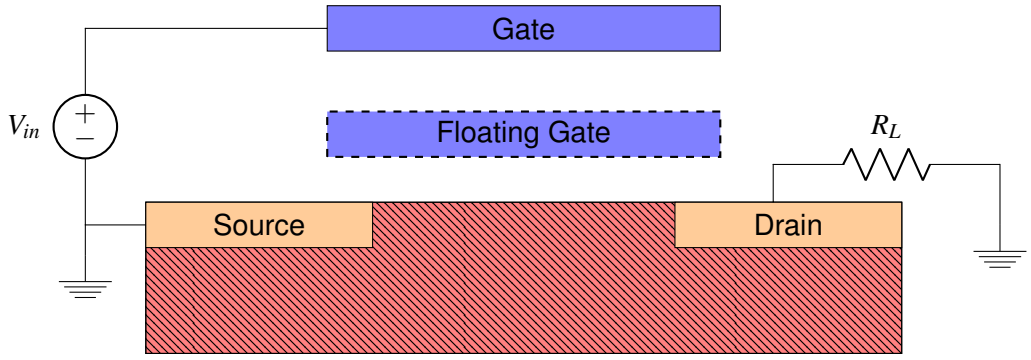


Figure 3: Transistor schematic for flash memory.

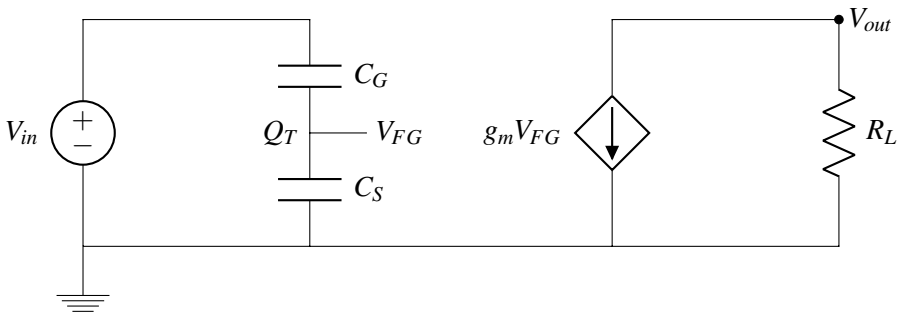


Figure 4: Corresponding circuit model for flash memory transistor from Figure 3.

Depending on the amount of charge on the floating node, the transistor is either storing a "0" bit or a "1" bit. In order to write a bit, electrons are added or removed from the "floating gate node" (labelled by V_{FG} in Figure 4), which is capacitively coupled to the gate and the source of the transistor as shown in Figure 3. Therefore, during transistor operation, there can be a net charge Q_T at the node V_{FG}.[1]

In each part of the problem, the values of each parameter do not change, and are given in the table below:

Component Parameters	
V_{in}	2.0V
C_G	35.0pF
C_S	3.0pF
g_m	300.0μA V^{-1}
R_L	35.0kΩ

[1]The method through which charge is added or removed from the floating gate is known as *Fowler-Nordheim* tunneling, where electrons are quantum mechanically tunnelled to the floating gate. In this problem, we will not worry about how the net charge is added to the floating gate node at the circuit level.

(a) Assuming that the floating gate node (V_{FG}) has no net charge ($Q_T = 0$). Find V_{FG} in terms of V_{in}, C_G, and C_S, and then plug in values from the table.

Solution:

Since there is no charge in the floating gate node, the C_G and C_S are in series. Thus, the equivalent capacitance is:

$$C_{\text{eq}} = \frac{C_G C_S}{C_G + C_S}$$

Additionally, since the capacitors are in series, the charges on both capacitors are the same:

$$Q_S = Q_G = C_{\text{eq}} V_{in}$$

Therefore, we have that V_{FG} is given by:

$$V_{FG} = \frac{Q_{\text{top}}}{C_S} = \frac{V_{in} C_{\text{eq}}}{C_S} = V_{in} \frac{C_G}{C_G + C_S}$$
$$= (2\,\text{V}) \frac{(35\,\text{pF})}{35\,\text{pF} + 3\,\text{pF}} = 1.842\,\text{V}$$

(b) Now let's assume there is a net charge of $Q_T = -20.0\text{pC}$ on the floating gate node. Find V_{FG} as a function of C_G, C_S, V_{in}, and Q_T and then plug in the numerical values. (*Hint: Use conservation of charge.*)

Solution:

By charge conservation at the floating gate node, we have:

$$Q_T = -C_G(V_{in} - V_{FG}) + C_S(V_{FG})$$

Solving for V_{FG}, we have:

$$V_{FG} = \frac{Q_T + C_G V_{in}}{C_G + C_S} = \frac{-20.0\,\text{pC} + (35\,\text{pF})(2\,\text{V})}{35\,\text{pF} + 3\,\text{pF}} = 1.316\,\text{V}$$

(c) Now, in order to read which bit the transistor is storing, we measure the value of V_{out}, which is the voltage drop across R_L, as shown in Figure 4. Assuming that the threshold for reading a "1" bit is $V_{out} \leq -1\,\text{V}$, what condition must V_{FG} satisfy? *(Note: This part is independent of the previous two subparts.)*

Solution:

The output voltage is given by:

$$V_{out} = -g_m V_{FG} R_L \leq -1\,\text{V}$$
$$V_{FG} \geq \frac{1}{g_m R_L} = \frac{1}{(300\,\mu\text{A}\,\text{V}^{-1})(35\,\text{k}\Omega)} = 0.095\,\text{V}$$

(d) Regardless of the answer you got in part (c), assume that the threshold for reading a "1" is $V_{FG} \geq 1\,\text{V}$. How much net charge, Q_T do you need on the floating gate node in order to read a "1"?

Solution:

From part (b), we have that:

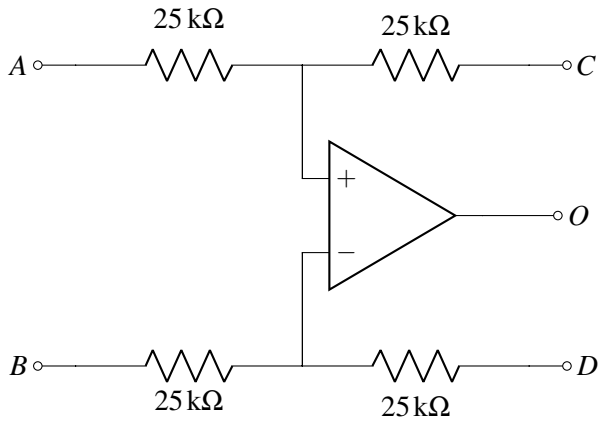
$$V_{FG} = \frac{Q_T + C_G V_{in}}{C_G + C_S} \geq 1\,\text{V}$$

This requires that:

$$Q_T \geq (1V)(C_G + C_S) - V_{in} C_G = -32\,\text{pC}$$

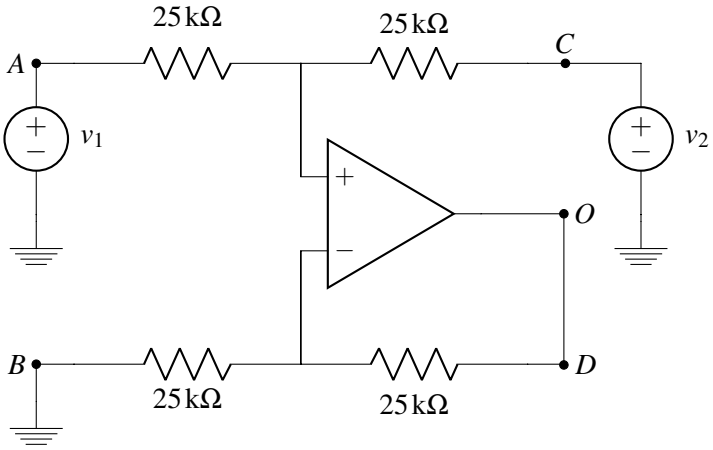
12. A Versatile Opamp Circuit (12 points)

The following circuit is a commonly used integrated circuit (IC) that can be configured in a variety of ways to achieve different functionalities. The main advantage of this IC is that it provides precise circuit functions without the need of a high precision resistor network.



In order to see this circuit's versatility, we will configure this circuit in different ways to achieve different functionalities. For each subpart, let $v_1 = 1.2\text{V}$ and $v_2 = 1.8\text{V}$

(a) Determine the voltage at O for the following configuration.



Solution:

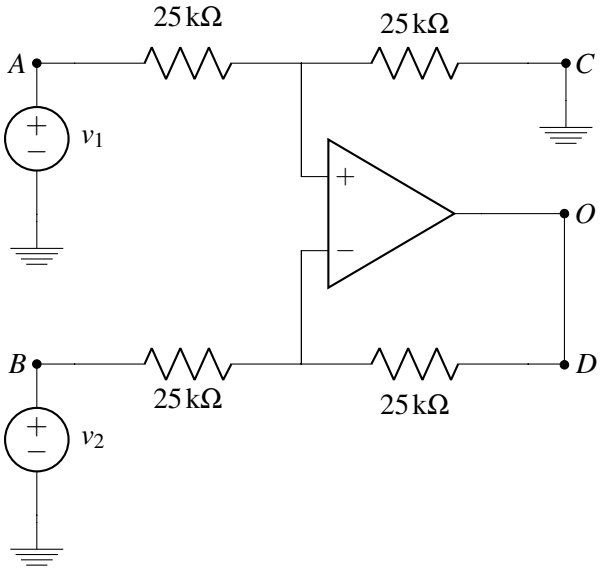
By superposition, we note that the voltage at V^+ is given by:

$$V^+ = \frac{v_1 + v_2}{2}$$

The rest of the circuit looks like a non-inverting amplifier with a gain of $1 + \frac{25\text{k}\Omega}{25\text{k}\Omega} = 2$. Therefore, the output voltage is:

$$V_O = 2V^+ = v_1 + v_2 = 1.2\,\text{V} + 1.8\,\text{V} = 3.0\,\text{V}$$

(b) Determine the voltage at O for the following configuration.



Solution:

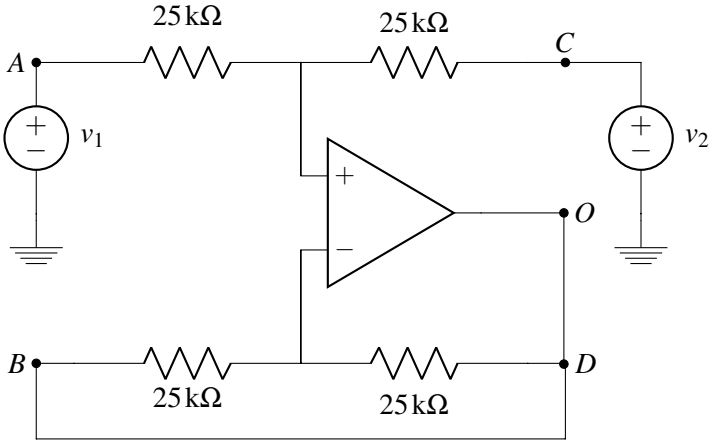
Through the voltage divider equation, we note that the voltages at the input terminals of the op-amp are given by:

$$V^+ = \frac{v_1}{2}$$
$$V^- = \frac{v_2 - V_O}{2}$$

By the Golden Rules, these must be equal to each other. Therefore,

$$\frac{v_1}{2} = \frac{v_2 - V_O}{2}$$
$$V_O = v_2 - v_1 = 1.2\,\text{V} - 1.8\,\text{V} = -0.6\,\text{V}$$

(c) Determine the voltage at O for the following configuration.



Solution:

Like in part (a), by superposition, we note that the voltage at V^+ is given by:

$$V^+ = \frac{v_1 + v_2}{2}$$

We note that the resistors connected to B and D do not affect the circuit as no current is flowing through them. Therefore, $V_O = V^- = V^+ = \frac{v_1+v_2}{2}$.

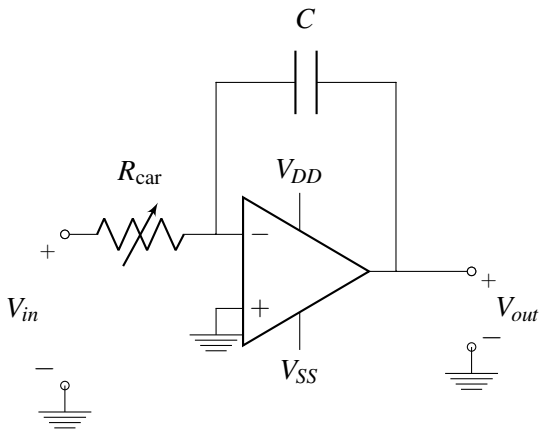
13. Odometer (16 points)

You are designing a circuit for an car odometer, which measures the distance the car has travelled. The main circuit element that you have is a resistor, whose resistance changes as a function of car velocity, which varies with time:

$$R_{\text{car}}(t) = \frac{4.0\alpha R_0}{v(t)}$$

where $R_0 = 100.0\text{k}\Omega$, $\alpha = 60.0\frac{\text{m}}{\text{s}}$, and v is the velocity of the car in $\frac{\text{m}}{\text{s}}$. Throughout the problem, assume that the capacitor is initially uncharged.

(a) Not knowing where to start, you ask a senior member of the design team, who went to Berkeley, and he gives you the following circuit to get you started.



As a first step, determine V_{out} in terms of t, V_{in}, α, R_0, $v(t)$, and C. (*Hint: Apply KCL and use the fact that* $I = C\frac{dV}{dt}$.)

Solution:

Let's write the KCL equation at V^- assuming all currents are leaving that node.

$$\begin{aligned}
i_{R_{\text{car}}} + i_C &= 0 \\
i_{R_{\text{car}}} &= -i_C \\
i_C &= C\frac{d(0 - V_{out}(t))}{dt} \\
\frac{0 - V_{in}}{R_{\text{car}}} &= C\frac{d(V_{out}(t) - 0)}{dt} \\
-\frac{V_{in}}{R_{\text{car}}C} &= \frac{dV_{out}(t)}{dt} \\
V_{out}(t) &= -\int_0^t \frac{V_{in}}{R_{\text{car}}C} d\tau \\
V_{out}(t) &= -\frac{1}{4\alpha R_0 C}\int_0^t V_{in} v(t) d\tau
\end{aligned}$$

(b) Regardless of the answer to part (a), the output of the above circuit is given by: $V_{out}(t) = -\frac{1}{\alpha R_0 C}\int_0^t V_{in} v(\tau) d\tau$. Now, you decide to set $V_{in} = 1\,\text{V}$. Your odometer increases its distance reading by 1 when the voltage, V_{out}, decreases by $0.1\,\text{V}$.

If you want the odometer to change its distance reading by 1 when the car travels 1 kilometer, what should C be? *Hint: The distance travelled by the car is given by* $\int_0^t v(\tau)\, d\tau$.

Solution:

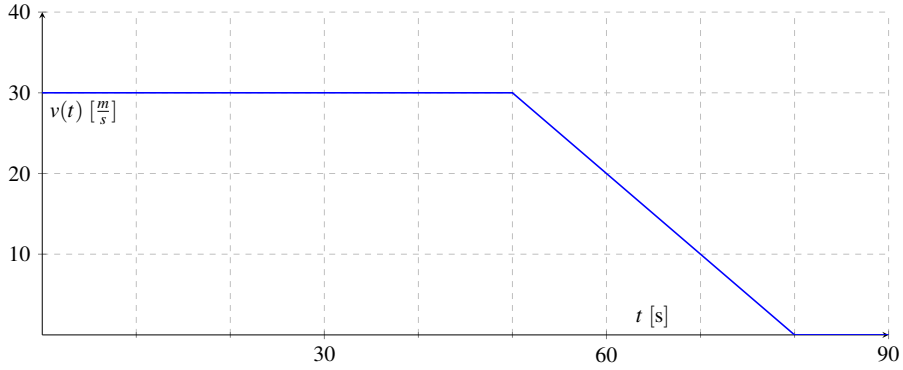
Substituting V_{in}, we have:

$$V_{out} = -\frac{1\,\text{V}}{\alpha R_0 C}\int_0^t v(t)d\tau$$

Since $\int_0^t v(t)d\tau$ represents the distance travelled by the car, we can set that to 1 km and set $V_{out} = -0.1\,\text{V}$ and solve for C.

$$C = \frac{10(1\,\text{km})}{\alpha R_0} = \frac{10(1\,\text{km})}{(60\,\text{m}\,\text{s}^{-1})(100\,\text{k}\Omega)} = 1.67\,\text{mF}$$

(c) Your car has the following velocity versus time graph. How much energy is dissipated through the car resistor, $R_{\text{car}}(t) = \frac{4.0\alpha R_0}{v(t)}$? Assume that V_{in} for the circuit given in part (a) is still 1 V.

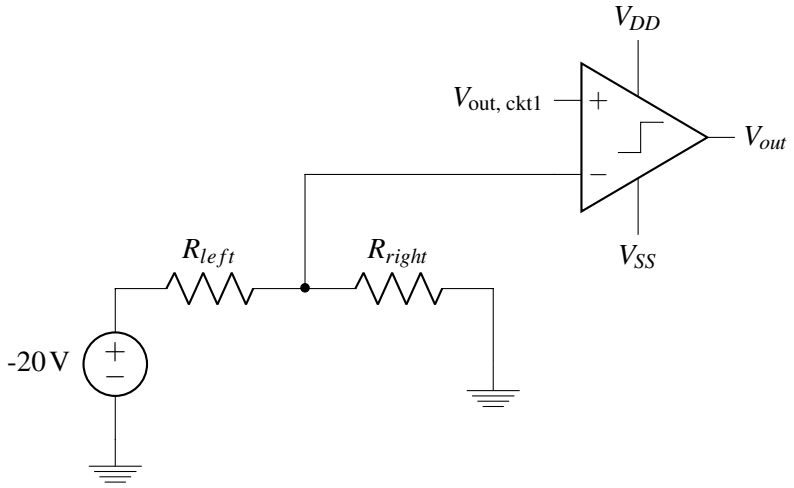


Solution:

The power through a resistor is given by $\frac{V^2}{R}$. We note that the potential difference across the resistor is fixed at 1 V. The total energy dissipated is given by $E = \int P(t)\, dt$. Therefore,

$$E = \int_0^{90} \frac{1\,\text{V}^2 v}{4\alpha R_0} d\tau = \frac{1}{4\alpha R_0}(50(30) + \frac{1}{2}(30)(30)) = \frac{1}{4\alpha R_0}(1950) = 81.25\,\mu\text{J}$$

(d) In order to add functionality, you want to add a comparator that will alert the driver when a certain number of kilometers has passed, using the odometer you designed in part (b). You do this with the following circuit:



$V_{\text{out, ckt1}} = -\frac{1}{\alpha R_0 C}\int_0^t V_{in} v(\tau) d\tau$ is the output of odometer circuit shown in part (a). If you want the comparator to change states after the car has driven 180.0km, given that we require $R_{left} + R_{right} = 70.0\text{k}\Omega$, what should the value of R_{left} be?

Solution:

The voltage at the negative terminal is given by:

$$V^- = \frac{(-20\,\text{V})R_{\text{right}}}{R_{\text{right}} + R_{\text{left}}}$$

180 km corresponds to a voltage output of -18 V from the first circuit. Thus, we want the voltage that the negative terminal of the op-amp to be at -18 V. This can be done by setting $R_{\text{left}} = 7\,\text{k}\Omega$.