**UNIVERSITY OF CALIFORNIA**
**College of Engineering**
**Department of Electrical Engineering and Computer Sciences**

EECS 130 Professor Chenming Hu
Spring 2005

# Final Exam
## May 17, 2005

**Name:** SOLUTION

**SID:** ____________________

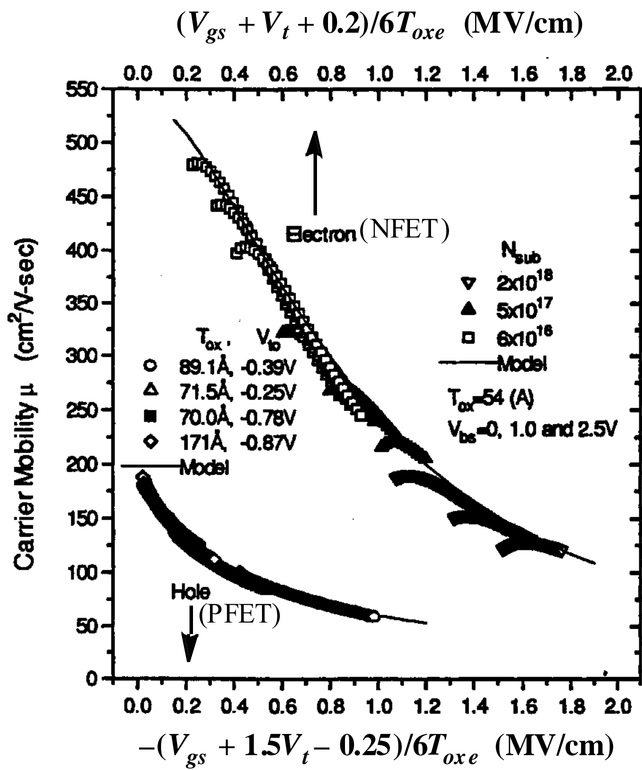
**Instructions:**

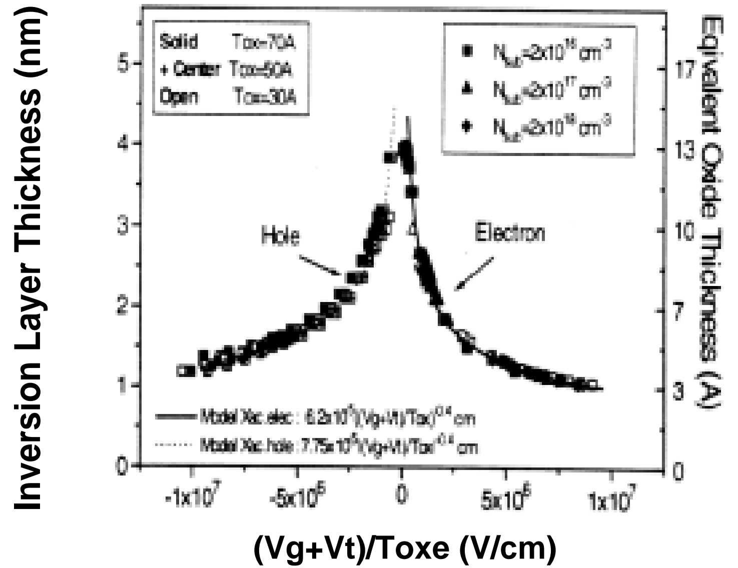
Print your name on the cover page CLEARLY now
Show major intermediate steps on exam pages to facilitate grading
Make sure your copy of the exam paper has 12 pages (including cover page)
Closed book. Three sheets of notes are allowed.

| | Score |
|---|---|
| Problem 1 | / 12 |
| Problem 2 | / 21 |
| Problem 3 | / 10 |
| Problem 4 | / 24 |
| Problem 5 | / 17 |
| Problem 6 | / 16 |
| Total | / 100 |

## Physical Constants

| | | |
|---|---|---|
| Electronic charge | q | $1.6 \times 10^{-19}$ C |
| Boltzmann's constant | k | $1.38 \times 10^{-23}$ J K$^{-1}$ |
| Permittivity of vacuum | $\varepsilon_0$ | $8.85 \times 10^{-14}$ F cm$^{-1}$ |
| Permittivity of oxide | $\varepsilon_{ox} = 3.9\ \varepsilon_o$ | |
| Permittivity of silicon | $\varepsilon_s = 11.7\ \varepsilon_o$ | |



**1. Explain the following in one or two sentences: (12pts.)**

(a) Why does larger $I_{dsat}$ lead to smaller circuit (such as inverter) delays? (3pts.)

**Faster charging/discharging of the capacitances in the circuit**

(b) What is the impact of reducing $V_T$ on circuit speed —increases the speed or decreases it? Why? (3pts.)

**Increase the speed due to higher $I_{dsat}$**

(c) Why can we **NOT** reduce $V_T$ to an arbitrarily low value? (3pts.)

**Lower Vt will have larger subthreshold leakage current => static power consumption increases.**

(d) Assume the electron and hole mobilities are increased 10 times. What is the impact on power consumption of CMOS inverters operating at a fixed frequency, f and $V_{dd}$? Why? (3pts.)

**Power consumption will be unaffected. Power= $CV_{dd}^2f$. Therefore, although $I_{dsat}$ increases due to enhanced mobility, the power consumption still remains identical.**

**2. MOSFET (21pts.)**

Consider a silicon n-channel MOSFET with an unknown metal as gate material. $T_{oxe}$=4nm, $V_{gs}$=2V, $V_T$=0.3V, $N_{sub} \approx 10^{17}cm^{-3}$, W=1μm, and the electron saturation velocity, $v_{sat}$, is $8\times10^6$cm/s.

*(Don't be discouraged if you can not answer some parts. The parts are independent of each other)*

(a) Estimate the body-effect factor, m. (3pts.)

$$\phi_B = kT/q \cdot \ln\left(\frac{N_{sub}}{n_i}\right) = 0.42eV$$

$$W_{d\max} = \sqrt{\frac{2\varepsilon_{si}2\phi_B}{qN_a}} = 1.04\times10^{-5}cm$$

$$m = 1 + \frac{3T_{oxe}}{W_{d\max}} = 1.12$$

(b) Estimate $\mu_s$. (3pts.)

**$E_{eff}=(V_{gs}+V_T+0.2)/6T_{oxe}$=1.04MV/cm. From the plot => $\mu_s$ ~230 $cm^2$/V-s**

(c) Suppose m=1.2 and L=0.1μm, estimate $V_{dsat}$ and $I_{dsat}$. Assume $\mu_s$ is 200$cm^2$/V-s regardless of your answer to part (b). (6pts.)

$$\varepsilon_{sat} = \frac{2v_{sat}}{\mu_s} = 8\times10^4 V/cm \Rightarrow \varepsilon_{sat}\cdot L = 0.8V$$

$$\frac{1}{V_{dsat}} = \frac{m}{V_g - V_t} + \frac{1}{\varepsilon_{sat}L} \Rightarrow V_{dsat} = 0.51V$$

$$I_{dsat} = \frac{W}{2mL} C_{oxe} \mu_s \frac{(V_{gs} - V_T)^2}{1 + \frac{V_{gs} - V_T}{m \varepsilon_{sat} L}}$$

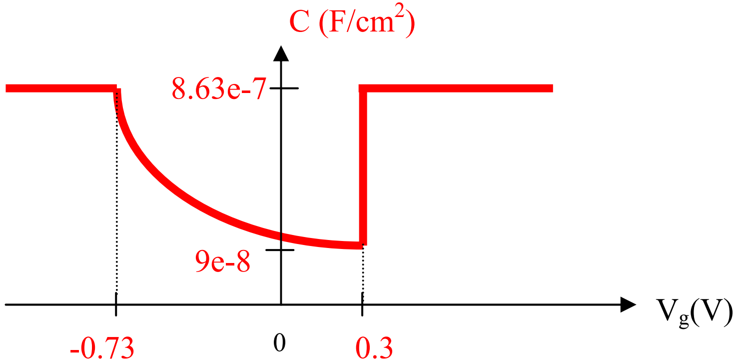
$$= \frac{1 \mu m}{2 \cdot 1.2 \cdot 0.1 \mu m} \times 8.63 \times 10^{-7} F/cm^2 \times 200 cm^2/V \cdot s \times \frac{(2-0.3)^2 V^2}{1 + \frac{(2-0.3)V}{1.2 \cdot 0.8V}}$$

$$= 7.5 \times 10^{-4} A$$

(d) Estimate the inversion layer thickness. (3pts.)

**$(V_g+V_t)/T_{oxe}=5.76\times10^6$ V/cm. From the plot, inversion layer thickness=1.2nm.**

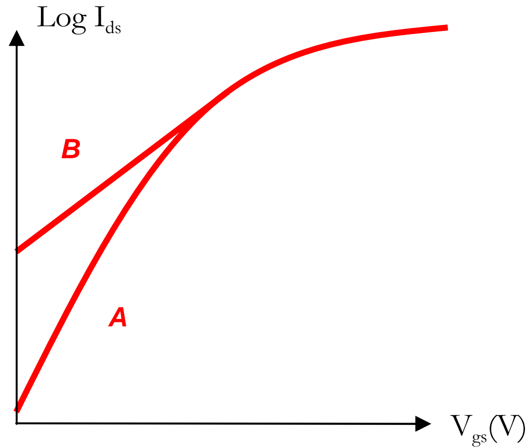
(e) Sketch the transistor CV curve. Mark $V_T$ and the estimated values of $V_{fb}$, and the estimated maximum and minimum values of C (in F/cm$^2$) in the plot. (6pts.)



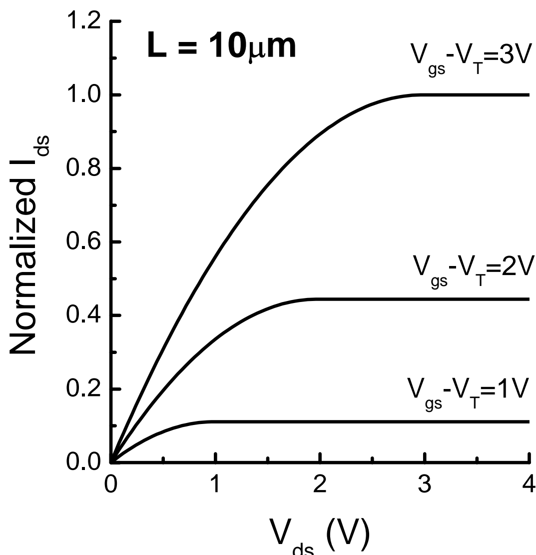
## 3. MOSFET I-V Characteristics (10pts.)

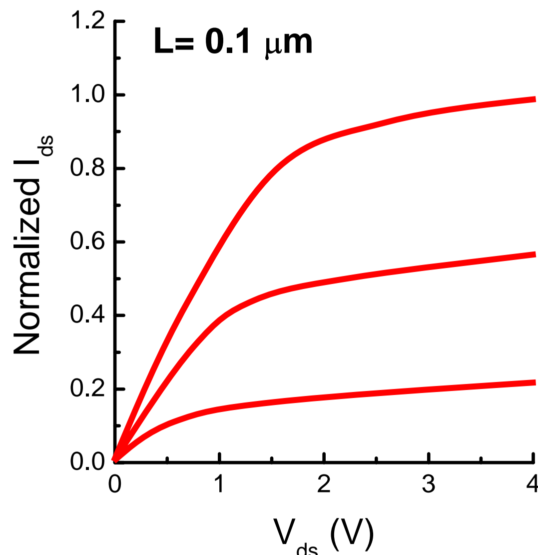
(a) Sketch the log $I_{ds}$ vs. $V_{gs}$ curve for an n-channel MOSFET. Label it A. (3pts.)

(b) In your plot in the previous part, add a second curve for another transistor. This second transistor has the same $V_T$ as A, but is less well designed so that its subthreshold current is larger than A. Label the second curve B. (3pts.)




(c) $I_{ds}$-$V_{ds}$ characteristics of a long channel n-channel MOSFET with L=10μm is shown below (the left hand side plot). The normalized Ids is defined as *$I_{ds}$/max current in the graph.* If the gate length is shortened to 0.1 μm, please redraw the $I_{ds}$-$V_{ds}$ characteristics in the right hand side graph below. (4pts.)



## 4. Semiconductor Physics and Diode (24pts.)

Consider InSb at room temperature, whose properties are given in the following table. Assume $N_c=N_v=10^{19}cm^{-3}$.

| Semiconductor | | Bandgap (eV) | | Mobility at 300 K ($cm^2/V\text{-}s$)[a] | |
|---|---|---|---|---|---|
| | | 300 K | 0 K | Elec. | Holes |
| Element | C | 5.47 | 5.48 | 1800 | 1200 |
| | Ge | 0.66 | 0.74 | 3900 | 1900 |
| | Si | 1.12 | 1.17 | 1500 | 450 |
| III–V | AlSb | 1.58 | 1.68 | 200 | 420 |
| | InSb | 0.17 | 0.23 | 80000 | 1250 |
| | GaAs | 1.42 | 1.52 | 8500 | 400 |

(a) Find the intrinsic carrier concentration, $n_i$. (3pts.)

$$n_i = \sqrt{N_c \cdot N_v} \cdot e^{-qE_g/2kT} = 3.8 \times 10^{17} cm^{-3}$$

(b) (i) Find $E_c$-$E_f$ for $n=5\times10^{18}cm^{-3}$. (ii) What is the hole concentration? (6pts.)

$$(i) n = N_c \cdot e^{-q(Ec-Ef)/kT} \Rightarrow 5 \times 10^{18} = 10^{19} \cdot e^{-q(Ec-Ef)/kT}$$
$$\Rightarrow E_c - E_f = 0.018eV$$

$$(ii) p = \frac{n_i^2}{n} = 2.9 \times 10^{16} cm^{-3}$$

(c) Find the conductivity of intrinsic InSb. (3pts.)

$$\sigma = qn\mu_n + qp\mu_p = qn_i\mu_n + qn_i\mu_p = 4.9 \times 10^3 S/cm \,(or\ 1/\Omega \cdot cm)$$

(d) It is possible to reduce the conductivity to a value below that in part (c) by doping the semiconductor. How would you dope (add donors or acceptors, and what concentration) InSb in order to make its conductivity as low as possible. Assume mobilities are not changed by the doping. (6pts.)

Assume the final *p-type* concetraion is "p"

$$\sigma(p) = qn\mu_n + qp\mu_p = q\frac{n_i^2}{p}\mu_n + qp\mu_p = q(1250 \cdot p + 80000 \cdot \frac{n_i^2}{p})$$

In order to find the minimum value of $\sigma$, differentiate the $\sigma$(p)

$$=> \frac{d\sigma(p)}{dp} = q \cdot 1250 \cdot \left(1 - 64 \cdot n_i^2 \cdot \frac{1}{p^2}\right) = 0 => \mathrm{p} = 8\mathrm{n_i}$$

From charge neutrality, $\mathrm{p} - \mathrm{N_a}^- - \mathrm{n} = 0 => 8\mathrm{n_i} - \mathrm{N_a}^- - \frac{\mathrm{n_i}^2}{8\mathrm{n_i}} = 0 => \mathrm{N_a}^- = 7.875\mathrm{n_i}$

Therefore, in order to make the lowest InSb conductivity,

we need to dope acceptors with concentration of $\mathrm{N_a} = 7.875\mathrm{n_i} = 3.0 \times 10^{18}\, cm^{-3}$

(e) Find the reverse leakage current, $I_0$, for an InSb $P^+N$ diode with an area=$10^{-7}$cm$^2$. Assume $\tau_p$=1μs and $N_d$=5×10$^{18}$cm$^{-3}$. Assume full ionization. (6pts.)

For one-sided junction, $I_0 = Aqn_i^2\left(\frac{D_p}{L_p N_d}\right)$

where, $D_p = \frac{kT}{q} \cdot \mu_p = 0.026 \times 1250 = 32.5 cm^2/s$

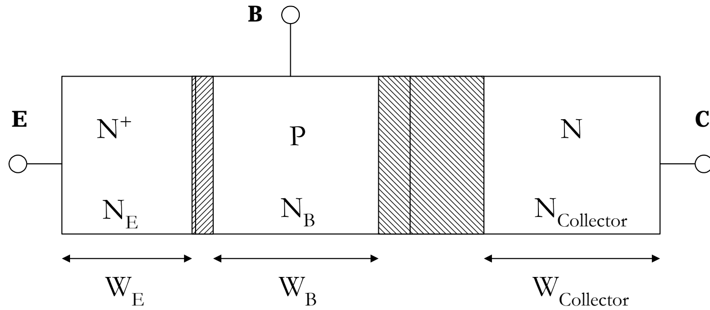
$L_p = \sqrt{D_p \tau_p} = \sqrt{32.5 \times 10^{-6}} = 5.7 \times 10^{-3}\, cm$

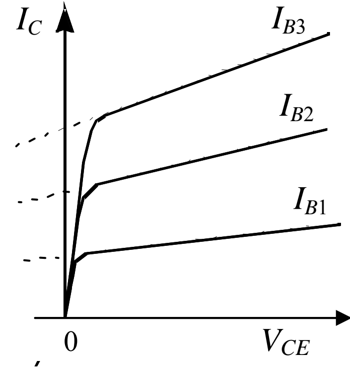
$$=> I_0 = 10^{-7}\, cm^2 \cdot 1.6 \times 10^{-19}\, coul \cdot (3.7 \times 10^{17}\, cm^{-3})^2 \cdot \left(\frac{32.5 cm^2/s}{5.7 \times 10^{-3}\, cm \cdot 5 \times 10^{18}\, cm^{-3}}\right)$$

$$= 2.64 \times 10^{-6}\, A$$

## 5. Bipolar Junction Transistor (17pts.)

Schematic NPN BJT is shown below.




Base-width modulation by collector voltage is responsible for the output conductance $dI_C/dV_{CE}$

(a) For a change in the top row parameters, what is the effect on the parameters in the left-column? Answer with ↑ to indicate "increase", ↓ for "decrease", and → for "no effect". $V_{BE}$ (forward bias) and $V_{CB}$ (reverse bias) remain constant (11pts.)

| | $W_B$↑ | $N_B$↑ | $W_E$↑ | $N_E$↑ | Base Bandgap is ***reduced*** |
|---|---|---|---|---|---|
| $I_C$ | ↓ | ↓ | | | ↑ |
| β | ↓ | ↓ | ↑ | ↑ | ↑ |
| $dI_C/dV_{CE}$ | ↓ | ↓ | | | |
| Base transit time | ↑ | | | | |

(b) Why is it desirable to introduce a built-in base field to aid the flow of electrons from the emitter to the collector? List two ways to introduce such a built-in base field. (3pts.)

**Base transit time will decrease.**

1. **Graded base doping, $N_B$ decreasing from emitter end to collector end.**
2. **Graded base bandgap, such as SiGe base, $E_{gB}$ decreasing from emitter end to collector end.**

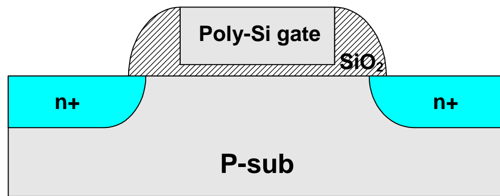
(c) Can one make a good bipolar transistor using metal as the emitter rather than $N^+$ semiconductor? Explain why in one or two sentences. (3pts.)

**No, since the current transport in Schottky junction is determined by majority carrier or since metal does not inject minority carriers into the semiconductor base.**

## 6. Process flow of "self-aligned silicided source/drain and gate" (16pts.)

(a) Please fill in the missing process steps by using available process options from the given menu. Note that **NOT** all the process steps need to be used and each step can be used more than once. (10pts.)

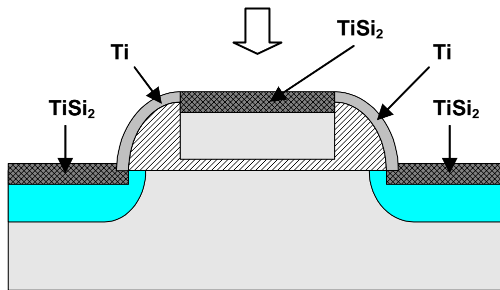
***Starting point***




***Fill in the missing steps***

- Sputter Ti
- Thermal Anneals to Create Silicide

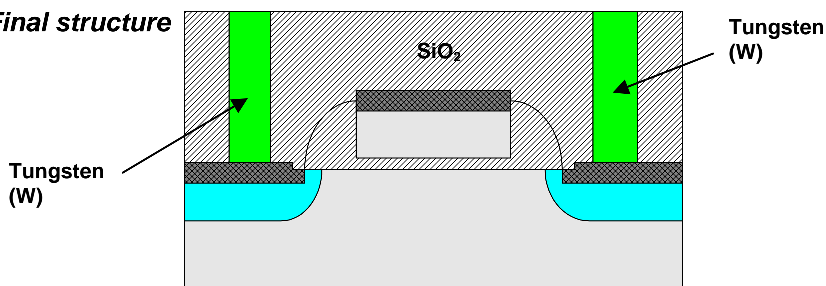
***Intermediate structure***




***Fill in the missing steps***

- Etch Ti
- CVD Oxide Deposition
- CMP (optional)
- Photolithography
- Oxide Etching
- W Deposition
- CMP

***Final structure***




| **Process Steps** |
|---|
| *Thermal Oxidation* |
| *CVD Oxide Deposition* |
| *Sputter Ti* |
| *Sputter $TiSi_2$* |
| *Thermal Anneals to Create Silicide* |
| *Etch Ti (does not attack $TiSi_2$)* |
| *Photolithography module* |
| *Oxide Etching* |
| *Tungsten (W) deposition* |
| *Chemical-Mechanical Polishing (CMP)* |

(b) Do you expect these $TiSi_2$-Si contacts to be ohmic or diode-like? Explain why in one or two sentences. (3pts.)

**Ohmic. Heavily-doped n+ will introduce quantum tunnelling due to very thin depletion layer.**

(c) If you could adjust the work function of $TiSi_2$ that is over the source/drain of this n-channel transistor, would you make it larger or smaller? Why? Explain in one or two sentences. (3pts.)

**Smaller work function. Ohmic resistance is proportional to** $e^{H\phi_B / \sqrt{N_d}}$ **.**