**University of California**
**College of Engineering**
**Department of Electrical Engineering**
**and Computer Sciences**

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**Thursday, November 4, 2010**
**6:30-8:00pm**

# EECS 141: FALL 2010—MIDTERM 2

**For all problems, you can assume that all transistors have a channel length of 100nm and the following parameters (unless otherwise mentioned):**

**NMOS:**
$V_{Tn}$ = 0.3V, $\mu_n$ = 400 cm$^2$/(V·s), $C_{oxn}$ = 1 μF/cm$^2$, $v_{sat}$ = 1e7 cm/s, $\lambda = 0$
**PMOS:**
$|V_{Tp}|$ = 0.3V, $\mu_p$ = 200 cm$^2$/(V·s), $C_{oxp}$ = 0.75 μF/cm$^2$, $v_{sat}$ = 1e7 cm/s, $\lambda = 0$

| **NAME** | Last First |
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**Problem 1: _____/ 24**

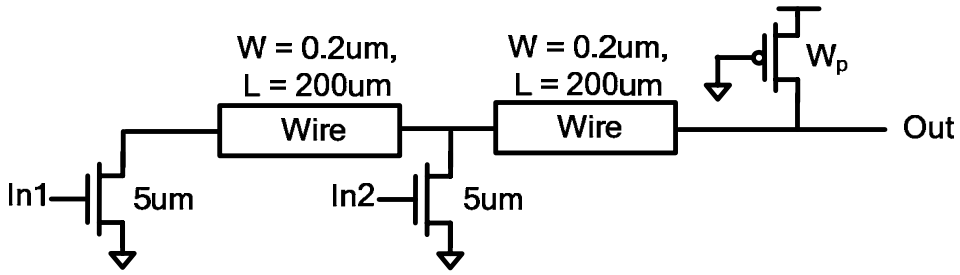
**Problem 2: _____/ 18**

**Problem 3: _____/ 24**

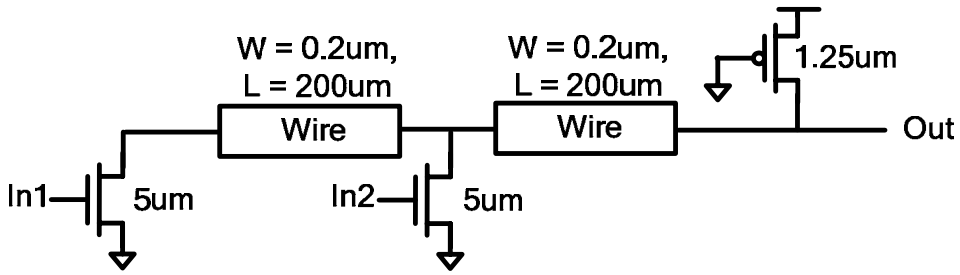
**Total: _____/ 66**

**PROBLEM 1. (22 pts) Wires, Delay, and Ratioed Logic**

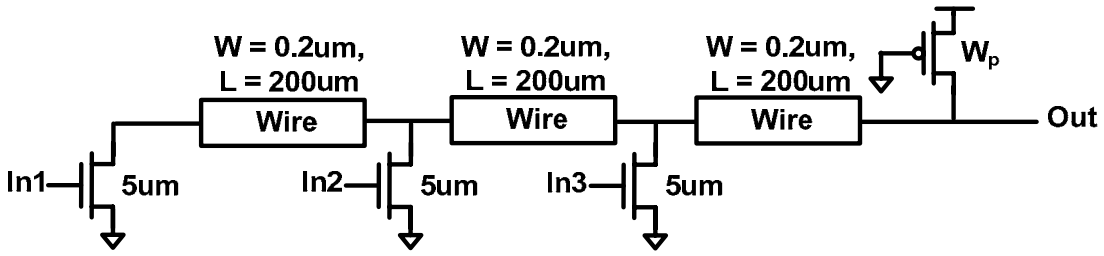
For this problem, you should assume that all of the transistors are minimum channel length (L=0.1μm) and have the following characteristics: $C_G = C_D = 2fF/\mu m$ and $R_{sqn} = R_{sqp}/2 = 10k\Omega/\square$. For the wires, you should assume that $C_{wpp} = 0.05fF/\mu m^2$, $C_{wfringe} = 0.075fF/\mu m/edge$, and $R_{sqw} = 0.1\Omega/\square$




**a) (6 pts)** For the circuit shown above, size the PMOS pull-up transistor (i.e., choose $W_p$) so that the pull-up resistance of the gate is equal to 4 times the worst-case pull-down resistance.



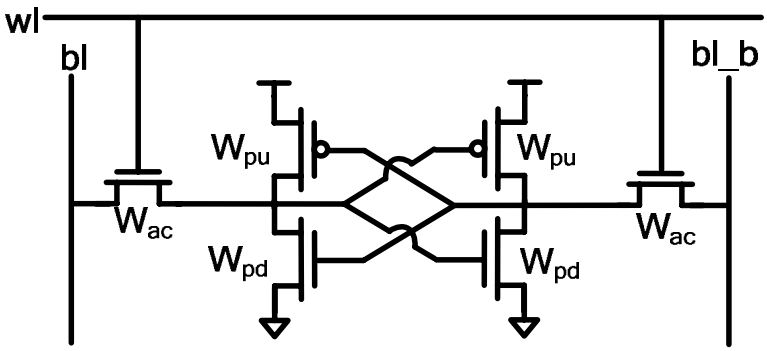

**b) (10 pts)** Assuming that you found that $W_p$ = 1.25um in order for the pull-up resistance to be 4 times larger than the worst-case pull-down resistance (as shown above – note that this may or may not be the right answer to part a) ), what is the worst-case ramp delay of the circuit?



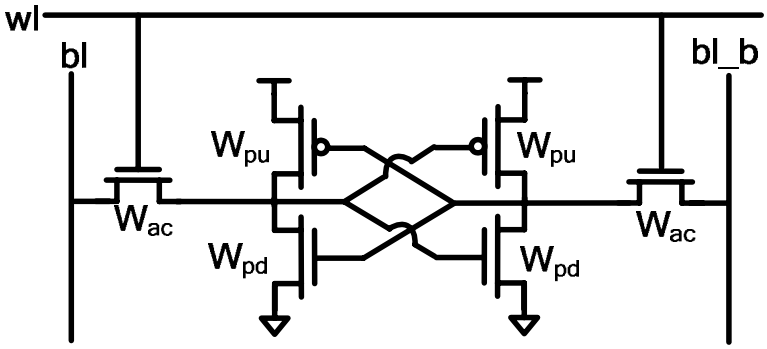

**c) (6 pts)** Assuming that every time you add another input to the circuit an additional 200um of wire is added as well (as shown above for 3 inputs), and that the pull-up transistor is always resized to make its resistance 4 times that of the worst-case pull-down resistance, what is the worst-case ramp delay of the circuit as a function of the number of inputs ($N_{in}$)?

**PROBLEM 2. (18 pts) Scaling and SRAM Design**

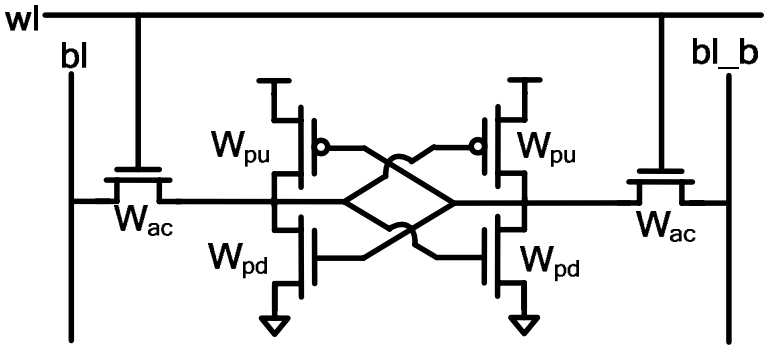
Unless otherwise specified, you should assume that $V_{DD}$ = 1.2V and use the velocity saturated model (with the parameters provided on the first page of the exam) throughout this problem.




a) **(6 pts)** Assuming that the $I_{DSAT}$ of the access transistor must be 1.5 times the $I_{DSAT}$ of the pull-up transistor (i.e., $I_{DSAT\_ac} = 1.5*I_{DSAT\_pu}$) in order to ensure sufficient write margin, what should $W_{pu}/W_{ac}$ be in our 100nm technology?



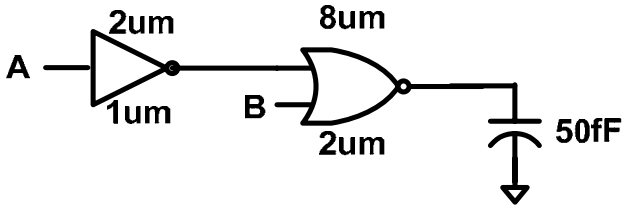

b) **(8 pts)** If we scale to a 50nm technology with fixed voltage scaling (i.e., $V_{DD}$ and $V_{TH}$ fixed), recalculate the $W_{pu}/W_{ac}$ required to maintain the same write margin as part a).



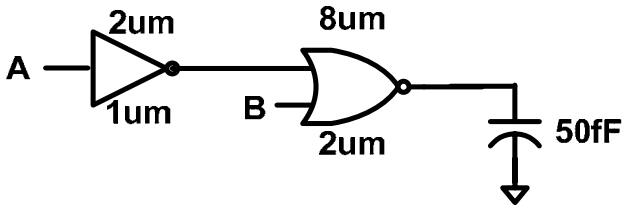

c) **(4 pts)** Given your answer to part b) and assuming that $W_{pd}/W_{ac}$ is set to 1.5 independent of technology and that the area of the SRAM cell is set by $W_{ac}*L+W_{pu}*L+W_{pd}*L$, how many times reduction in area is achieved by scaling the SRAM cell from the 100nm technology to the 50nm technology?

**PROBLEM 3. Power Consumption (24 points)**

This problem will deal with the circuit shown below. Unless otherwise specified, throughout this problem you can assume that $V_{DD}$ = 1.2V, $V_{THN}$ = $|V_{THP}|$ = 0.3V, $C_D$ = 0, $C_G$ = 2fF/μm, and $R_{sqn}$ = 2*$R_{sqp}$. You can also assume that leakage current is modeled by $(W/L)\,I_0 e^{(-V_{TH}/38mV)}$, where $I_{0,NMOS}$ = 10μA and $I_{0,PMOS}$ = 5μA.




a) **(8 pts)** Assuming that the A input is high half of the time, the B input is high 1/8 of the time, and that the circuit runs at a clock frequency of 400MHz, how dynamic much power is consumed by the circuit shown above? Don't forget to include the power consumed by driving the A and B inputs.




b) **(8 pts)** Under the same conditions as part a), how much leakage power does the circuit consume?

c) **(8 pts)** Given your answers to parts a) and b), if you could change both the $V_{DD}$ and $V_{TH}$ of the transistors in the circuit (but not any of the sizes), how would you change them in order to achieve lower total power consumption without increasing the delay? You do not need to provide any numerical answers – just an explanation of how you would change $V_{DD}$ and $V_{TH}$, and why you would change them that particular way. However, the more specific your answer, the more credit you will receive. (Hint: You can use the $V_T$* model to guide your answer when thinking about delay.)