EECS 16B Designing Information Devices and Systems II
Fall 2018 Elad Alon and Miki Lustig

Midterm 1

Name: _____

SID: _____

Discussion Section and TA (Monday): _____

Discussion Section and TA (Wednesday): _____

Lab Section and TA: _____

Name and SID of left neighbor: _____

Name and SID of right neighbor: _____

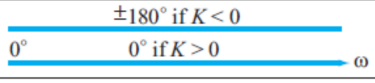
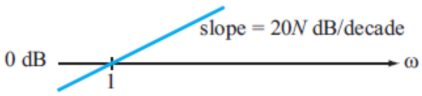
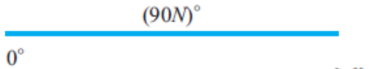
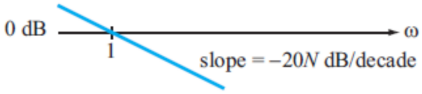
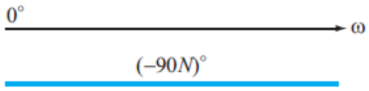
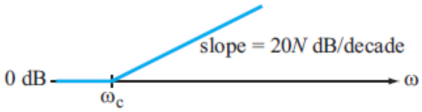
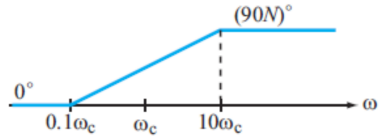
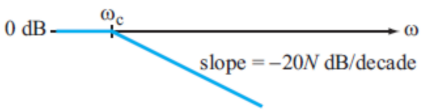
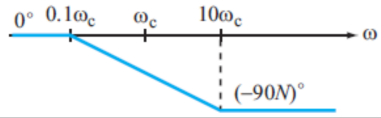
Instructions

- You have 120 minutes to complete this exam. Check that the exam contains 17 pages total.
- After the exam begins, write your SID in the top right corner of each page of the exam.
- Only the front pages will be scanned and graded; you can use the back pages as scratch paper.
- Do not remove any pages from the exam or unstaple the exam as this disrupts scanning. If needed, cross out any work you do not want to be graded.

Problem	Points
1	27
2	19
3	6
4	24
5	16

Table of Unit Prefixes

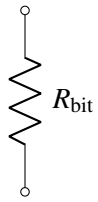
Prefix	M	k	m	μ	n	p	f
Value	10^6	10^3	10^{-3}	10^{-6}	10^{-9}	10^{-12}	10^{-15}

Factor	Bode Magnitude	Bode Phase
Constant K		
Zero @ Origin $(j\omega)^N$		
Pole @ Origin $(j\omega)^{-N}$		
Simple Zero $(1 + j\omega/\omega_c)^N$		
Simple Pole $\left(\frac{1}{1 + j\omega/\omega_c}\right)^N$		

1. Intelligent Memory (27 pts)

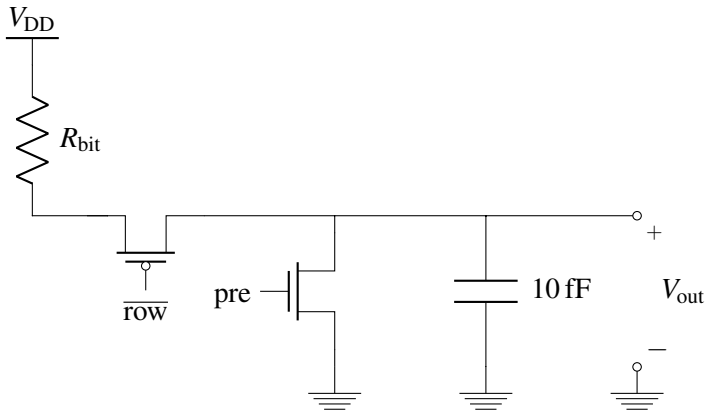
The performance of most machine learning applications is dominated by memory accesses, and hence many researchers are developing new types of memories that attempt to address this issue. In this problem, we will analyze a circuit that is relevant to an emerging type of memory known as "R-RAM" (Resistive RAM). R-RAM cells store information in the value of their internal resistance. For this problem, we will look at an R-RAM cell storing binary information – specifically:

R-RAM Cell



$$R_{\text{bit}} = \begin{cases} 1\,\text{M}\Omega, & \text{Cell stores a "0"} \\ 100\,\text{k}\Omega, & \text{Cell stores a "1"} \end{cases}$$

For the rest of this problem, consider the circuit (which is associated with reading out an R-RAM cell) shown below:



(a) (**8 pts**) Before analyzing the circuit directly, design a CMOS logic gate that implements the function $\overline{\text{row}} = \overline{A_0 \cdot A_1 \cdot A_2 \cdot A_3}$.
(Note that the A_0, A_1, A_2, and A_3 inputs are typically the address bits that decide which row within the memory to access.)

Now consider the case where $\overline{\text{row}} = \text{pre} = V_{\text{DD}}$ and the circuit is in steady state. At time $t = 0$, both the $\overline{\text{row}}$ and pre signals change their values to 0 V. We will read out the state of the R-RAM by measuring the voltage V_{out} at $t = 1$ ns after this transition occurs – i.e., by measuring $V_{\text{out}}(1\,\text{ns})$.

Note that throughout this problem, you can assume that the transistors are ideal – i.e., that their $R_{\text{on}} = 0\,\Omega$. You should also assume that $V_{\text{DD}} = 1$ V. Note that you do not need to provide a fully simplified numerical answer for any remaining sub-parts of this question. In particular, you can leave exponential terms (i.e. e^x) unsimplified.

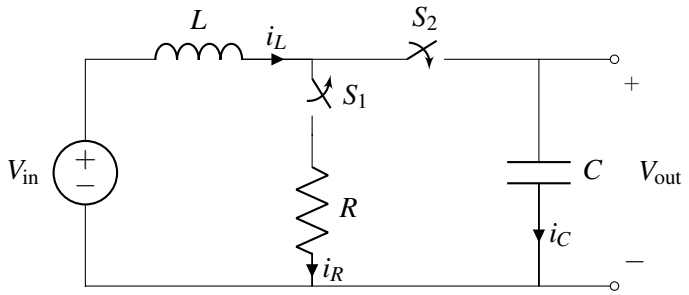
(b) (**8 pts**) What is the value of $V_{\text{out}}(1\,\text{ns})$ if the R-RAM stores a "0"?

(c) (**4 pts**) What is the value of $V_{\text{out}}(1\,\text{ns})$ if the R-RAM stores a "1"?

(d) (**7 pts**) How much energy has been delivered by the voltage source V_{DD} between $t = 0\,\text{ns}$ and $t = 1\,\text{ns}$ if the R-RAM is storing a "1"?

2. Mechanical Differential Equations (19 pts)

Consider the circuit shown below.



At $t < 0$, S_1 is on (short-circuited), and S_2 is off (open-circuited).
At $t \geq 0$, S_1 is off (open-circuited), and S_2 is on (short-circuited).

(a) **(4 pts)** Right after the switches change state (i.e., at $t = 0$), what is the value of i_L?

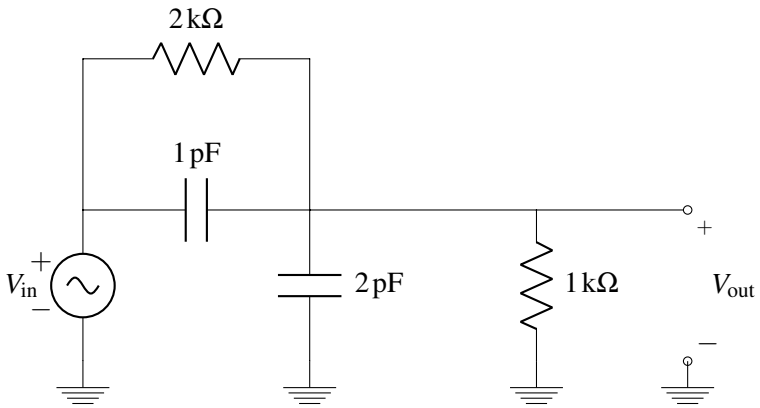
(b) **(5 pts)** Choosing the state variables as $\vec{x}(t) = \begin{bmatrix} V_{out}(t) \\ i_L(t) \end{bmatrix}$, derive the **A** matrix that captures the behavior of this circuit for $t \geq 0$ with the matrix differential equation $\frac{d\vec{x}(t)}{dt} = \mathbf{A}\vec{x}(t) + \vec{b}$, where $\vec{b}$ is a vector of constants.

(c) **(10 pts)** Assuming that $V_{\text{out}}(0) = 0\,\text{V}$, derive an expression for $V_{\text{out}}(t)$ for $t \geq 0$.

3. Phasor Gainz (6 pts)

Derive $H(j\omega) = \frac{\tilde{V}_{\text{out}}}{\tilde{V}_{\text{in}}}$ for the circuit shown below.

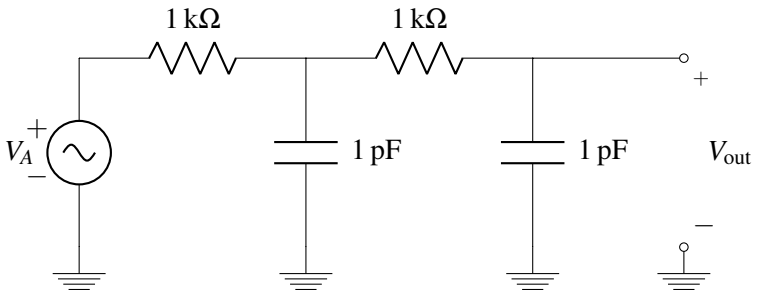
Hint: Simplifying your initial expressions should lead to a very compact result for $H(j\omega)$.



4. Equality for All Frequencies (24 pts)

Note: A Bode plot cheat sheet has been provided on page 2 of the exam.

(a) **(8 pts)** Imagine that we have two chips (chip A and chip B) trying to communicate a voltage signal from one chip to the other across a long wire. We will model this scenario with the circuit shown below, where V_A models a circuit inside of chip A that is creating the signal, and V_{out} is the voltage received by chip B.

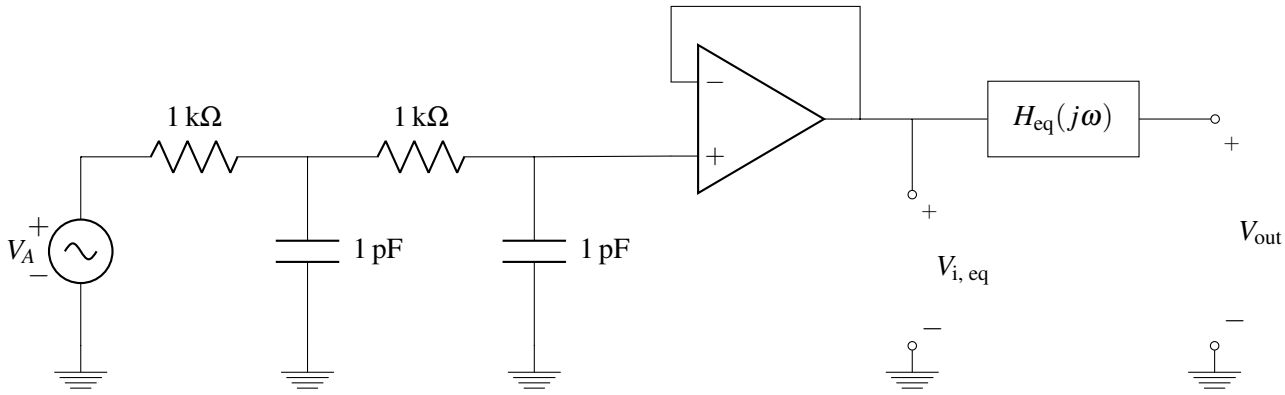


Note that for this circuit, you can assume that

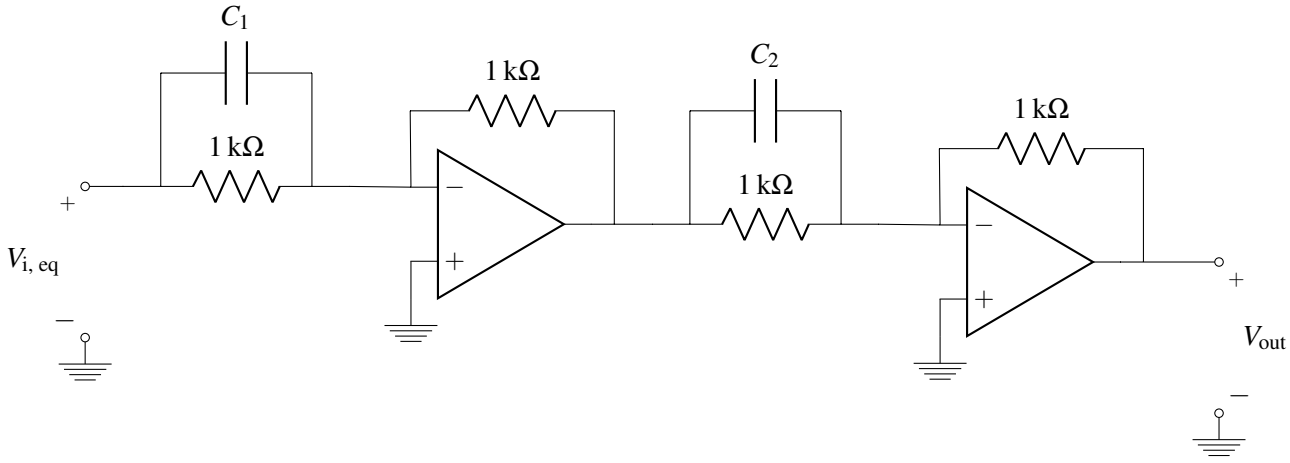
$$H(j\omega) = \frac{\tilde{V}_{\text{out}}}{\tilde{V}_A} = \frac{1}{(1 + j\omega \cdot 0.5 \cdot 10^{-9})(1 + j\omega \cdot 10^{-9})}.$$

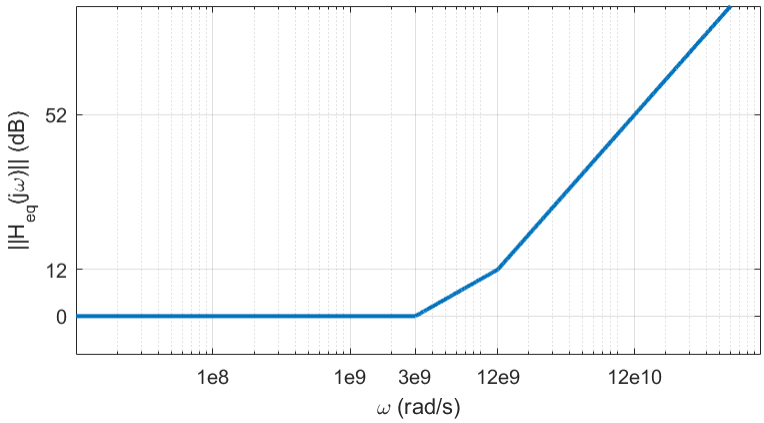
Sketch the magnitude and phase Bode plots of $H(j\omega)$. Be sure to **label** (a) the locations of each pole/zero, (b) the magnitude values at each pole/zero location, (c) the slopes (in dB/dec) of all segments of the magnitude plot, (d) the low-frequency ($\omega = 0$) and high-frequency ($\omega = \infty$) values of the phase, (e) the frequencies at which the slope of the phase changes. **Note that you do not need to specifically label the values of the phase at the pole/zero frequencies.**

(b) **(6 pts)** Now let's add an "equalizer" circuit to chip B, as modeled below. The goal of this equalizer is to make it so that $V_{\text{out}} = V_A$, which is equivalent to stating that $\frac{\tilde{V}_{\text{out}}}{\tilde{V}_A} = 1$. Sketch a magnitude Bode plot of what $|H_{\text{eq}}(j\omega)|$ would need to be in order to achieve the goal of making $\frac{\tilde{V}_{\text{out}}}{\tilde{V}_A} = 1$.



(c) **(10 pts)** Your colleague suggests the circuit shown below in order to realize $H_{\text{eq}}(j\omega)$. (I.e., the transfer function $\frac{\tilde{V}_{\text{out}}}{\tilde{V}_{\text{i, eq}}}$ of this circuit should be equal to $H_{\text{eq}}(j\omega)$.) Choose values for C_1 and C_2, such that the magnitude of the frequency response of this circuit matches the plot shown below (which may or may not be the correct answer to part (b)).

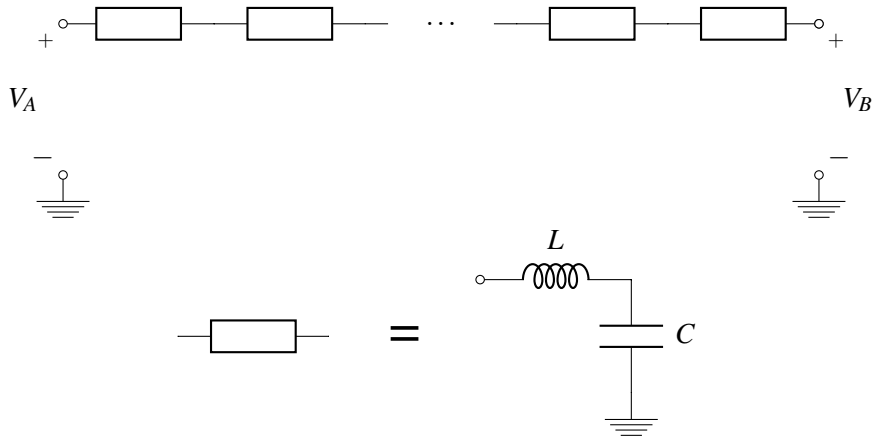




[ADDITIONAL SPACE FOR SOLUTION TO PART (C)]

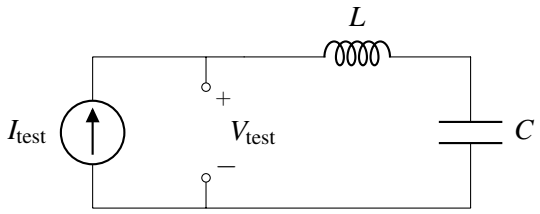
5. Circuits$^{\infty}$ (16 pts)

We sometimes model wires and other physical structures by decomposing them into an infinite number of (infinitely short) "sub-sections". In particular, long wires between two electrical circuits are often modeled as below:

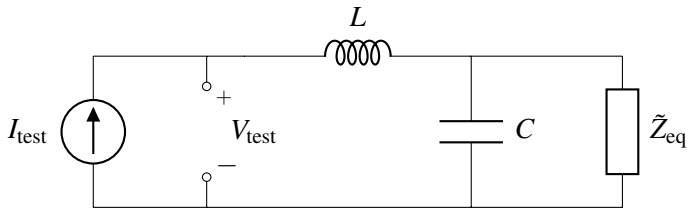


In this problem, we will examine the equivalent impedance of such a structure. As a reminder, the equivalent impedance $\tilde{Z}_{\text{eq}}$ of a circuit with some phasor voltage $\tilde{V}_{\text{test}}$ across it and some phasor current $\tilde{I}_{\text{test}}$ flowing through it is $\tilde{Z}_{\text{eq}} = \frac{\tilde{V}_{\text{test}}}{\tilde{I}_{\text{test}}}$.

(a) **(5 pts)** For the circuit shown below (which is a single sub-section in our wire model), derive $\tilde{Z}_{\text{eq}}$ using a test current source (as shown below). Your answer should be a function of L, C, and ω.



(b) **(8 pts)** Now let's compute the $\tilde{Z}_{\text{eq}}$ of the entire wire (which has an infinite number of sub-sections). **Note that this $\tilde{Z}_{\text{eq}}$ is not the same as your answer to part (a)**. The method we will use to do this relies on the idea that if we remove only one out of an infinite number of sections, the equivalent impedance of the remaining circuit (which still has an infinite number of sections, since $\infty - 1 = \infty$) should not change. This results in the circuit model shown below:



Using the fact that the $\tilde{Z}_{\text{eq}}$ of the circuit shown above (as a reminder, $\tilde{Z}_{\text{eq}} = \frac{\tilde{V}_{\text{test}}}{\tilde{I}_{\text{test}}}$) should be equal to the $\tilde{Z}_{\text{eq}}$ included within the circuit itself, solve for $\tilde{Z}_{\text{eq}}$ as a function of L, C, and ω.

(c) **(3 pts)** What is the DC value of $\tilde{Z}_{\text{eq}}$ – i.e., what is $\tilde{Z}_{\text{eq}}$ when $\omega = 0$?

[THIS PAGE IS INTENTIONALLY LEFT BLANK]