EECS 16A Designing Information Devices and Systems I Summer 2017 D. Aranki, F. Maksimovic, V. Swamy Midterm 2

Exam Location: 100 Genetics & Plant Bio

PRINT your student ID:								
PRINT AND SIGN your name:	, (last name)							
PRINT your discussion section and GSI(s) (the one you attend):								
Name and SID of the person to your left:								
Name and SID of the person to your right:								
Name and SID of the person in front of you:								
Name and SID of the person behind you:								
1. What do you enjoy most abou	ıt EE16A? (1 point)							

2. Write down a pun or a joke about circuits. (0 points)

Solution:

Can you handle all these puns in series? I know people are currently divided on this issue.

I'd write a pun, but it might shock you. Wire you even asking me this? I currently don't have the capacity for puns. I must resist with all my power. I've heard from independent sources that I get full points for this anyway. I hope this test doesn't short-circuit my brain, or I'm going to charge you with an unusual and cruel pun-ishment. You haven't seen my full potential. K, CL later.

Do not turn this page until the proctor tells you to do so. You may work on the questions above.

3. Cover Your Basis (7 points)

Consider the set $S = \left\{ \begin{bmatrix} \alpha - \beta \\ \alpha + 2\beta \\ -2\alpha + \beta \end{bmatrix} \middle| \alpha, \beta \in \mathbb{R} \right\}$. You are told that *S*, alongside the traditional vector addition and scalar vector multiplication, constitutes a vector space.

(a) (2 points) **Find a basis** for the vector space *S*. **Solution:**

$$\begin{bmatrix} \alpha - \beta \\ \alpha + 2\beta \\ -2\alpha + \beta \end{bmatrix} = \alpha \begin{bmatrix} 1 \\ 1 \\ -2 \end{bmatrix} + \beta \begin{bmatrix} -1 \\ 2 \\ 1 \end{bmatrix}$$
$$\mathscr{B}_{S} = \left\{ \begin{bmatrix} 1 \\ 1 \\ -2 \end{bmatrix}, \begin{bmatrix} -1 \\ 2 \\ 1 \end{bmatrix} \right\}$$

(b) (1 point) What is the dimension of the vector space S?Solution:

$$\dim(S) = 2$$

(c) (4 points) Consider a **new** vector space $S_{new} \subset \mathbb{R}^3$ with its basis being the columns of the matrix

$$\mathbf{B} = \begin{bmatrix} -1 & 1\\ -2 & 1\\ 1 & -3 \end{bmatrix}.$$

Write the coordinates of the vector $\vec{x} = \begin{bmatrix} 5\\9\\-7 \end{bmatrix}$ in the basis **B**. That is, calculate $[\vec{x}]_{\mathbf{B}}$.

Hint: $[\vec{x}]_{\mathbf{B}}$ is a vector in \mathbb{R}^2 . **Solution:**

$$\begin{bmatrix} -1 & 1 & | & 5 \\ -2 & 1 & | & 9 \\ 1 & -3 & | & -7 \end{bmatrix} \sim \begin{bmatrix} -1 & 1 & | & 5 \\ 0 & 1 & | & 1 \\ 0 & -2 & | & -2 \end{bmatrix} \sim \begin{bmatrix} 1 & 0 & | & -4 \\ 0 & 1 & | & 1 \\ 0 & 0 & | & 0 \end{bmatrix}$$
$$[\vec{x}]_{\mathbf{B}} = \begin{bmatrix} -4 \\ 1 \end{bmatrix}$$

4. Mechanical Circuits (15 points)

(a) (3 points) Find the equivalent resistance R_{eq} between the two terminals if $R_1 = 12.5 \Omega$, $R_2 = 5 \Omega$, $R_3 = 15 \Omega$, $R_4 = 5 \Omega$, and $R_5 = 5 \Omega$.



Solution:

$$R_{eq} = R_1 + R_3 \parallel (R_2 + R_4 + R_5)$$

= 12.5\Omega + 15\Omega \parallel 15\Omega
= 12.5\Omega + 7.5\Omega
= 20\Omega

(b) (4 points) Consider the following circuit below:



i. Find the voltage v_1 across R_1 if $R_1 = 10\Omega$ and $R_2 = 20\Omega$. Solution: Using the current divider formula, we get:

$$i_1 = \frac{20\Omega}{10\Omega + 20\Omega} \cdot 150 \,\mathrm{mA} = 100 \,\mathrm{mA}$$

Using Ohm's law, we get:

$$v_1 = 100 \,\mathrm{mA} \cdot 10 \,\Omega = 1 \,\mathrm{V}$$

ii. Calculate the power P_1 dissipated by R_1 if $R_1 = 10\Omega$ and $R_2 = 20\Omega$. Solution: From part (b)i., we know that $i_1 = 100$ mA and that $v_1 = 1$ V.

$$P_1 = i_1 v_1 = 100 \,\mathrm{mA} \cdot 1 \,\mathrm{V} = 100 \,\mathrm{mW}$$

(c) (8 points) Use nodal analysis to **find the voltage** v_{out} in the following circuit below.



Solution:



We first apply KCL at node 1.

$$\frac{v_R}{1} + 6 + 2v_R = 0$$
$$3v_R = -6 \implies v_R = -2$$

We then apply KCL at node 2.

$$-6 - 2v_R + \frac{v_{out}}{2} = 0$$
$$\frac{v_{out}}{2} = 6 - 4 = 2 \implies v_{out} = 4V$$

5. Taking the Super-L (12 points)

Consider the following circuit below:



In this problem, you will use *superposition* to find the voltage v_R across the 5 Ω resistor.

(a) (3 points) First, turn off all sources *except* V_{s_1} . Find v_{R_1} , the voltage across the 5 Ω resistor, if all sources *except* V_{s_1} are turned off. **Solution:**

We turn off all sources except V_{s_1} to get the following circuit:



Since the 5 Ω and the 20 Ω resistors are in series, we can use the voltage divider formula to find the voltage v_{R_1} across the 5 Ω resistor.

$$v_{R_1} = \frac{5\Omega}{5\Omega + 20\Omega} \cdot 5\mathrm{V} = 1\mathrm{V}$$



(b) (3 points) Now turn off all sources *except* I_{s_1} . Find v_{R_2} , the voltage across the 5 Ω resistor, if all sources *except* I_{s_1} are turned off.

Solution:

We turn off all sources except I_{s_1} to get the following circuit:



Since the 20 Ω and the 5 Ω resistors are in parallel, we can use the current divider formula to find the current i_{R_2} through the 5 Ω resistor.

$$i_{R_2} = -\frac{20\Omega}{20\Omega + 5\Omega} \cdot 1 \mathbf{A} = -0.8 \mathbf{A}$$
$$v_{R_2} = -0.8 \mathbf{A} \cdot 5\Omega = -4 \mathbf{V}$$



(c) (3 points) Now turn off all sources *except* I_{s_2} . Find v_{R_3} , the voltage across the 5 Ω resistor, if all sources *except* I_{s_2} are turned off.

Solution:

We turn off all sources except I_{s_2} to get the following circuit:



There is no current flowing through the 5 Ω resistor, so $v_{R_3} = 0$ V.

(d) (3 points) Now find the voltage v_R across the 5 Ω resistor if *all sources* are on. Solution:

We add up v_{R_1} , v_{R_2} , and v_{R_3} to get:

$$v_R = 1 V - 4 V + 0 V = -3 V$$

6. Golden Rules Op-Amps (14 points + 4 BONUS points)

(a) (2 points) Find the voltage $v_{out,a}$ as a function of the voltage V_s and *n*. Use the Golden Rules. Note: Pay careful attention to the polarity of the voltage $v_{out,a}$.



Solution:

$$v_{\text{out,a}} = \frac{nR_1}{R_1} \cdot V_s = nV_s$$

(b) (2 points) Find the voltage $v_{out,b}$ as a function of the voltage V_s and *m*. Use the Golden Rules.



Solution:

$$v_{\text{out,b}} = \left(1 + \frac{mR_2}{R_2}\right) \cdot V_s = (1+m)V_s$$

(c) (10 points) Find the currents labeled i_{s_1} , i_{f_1} , i_{f_2} , and i_{s_2} , and the voltage v_{out} , as a function of the voltage at the node v_1 only, **NOT** the source voltage V_s . Assume that the resistance $R = 1 \Omega$. Show your work in the subsections provided and fill in the table at the end with your results. Use the Golden *Rules*.



i. Find i_{s_1} as a function of v_1 . Solution:

$$i_{s_1} = \frac{v_1 - 0}{R} = v_1$$

ii. Find i_{f_1} as a function of v_1 . Solution:

 $i_{f_1} = i_{s_1} = v_1$

iii. Find v_{out} as a function of v_1 . **Solution:**

$$v_{\text{out}} = 0 - i_{f_1}R = -v_1$$

iv. Find i_{f_2} as a function of v_1 . Solution:

$$i_{f_2} = rac{v_1 - v_{\text{out}}}{R} = 2v_1$$

v. Find i_{s_2} as a function of v_1 . Solution:

$$i_{s_2} = i_{s_1} + i_{f_2} = 3v_1$$

<i>i</i> _{<i>s</i>₁}	i_{f_1}	v _{out}	i_{f_2}	i_{s_2}

Solution:

<i>i</i> _{<i>s</i>1}	i_{f_1}	<i>v</i> _{out}	i_{f_2}	i_{s_2}
<i>v</i> ₁	<i>v</i> ₁	$-v_1$	$2v_1$	3 <i>v</i> ₁

(d) (4 **BONUS** points) In the circuit, find v_{out} as a function of V_s . Assume that the resistance $R = 1 \Omega$. Use *the Golden Rules*.

Hint: This is the same circuit as in part (c). You may want to use your results from part (c).



Solution:

From part (c), we know that $i_{s_2} = 3v_1$. Using Ohm's law, we get:

$$\frac{V_s - v_1}{R} = 3v_1 \implies V_s - v_1 = 3v_1 \implies V_s = 4v_1$$

Furthermore, we know that $v_{out} = -v_1$.

$$V_s = 4v_1 = -4v_{\text{out}} \implies v_{\text{out}} = -\frac{V_s}{4}$$



7. Thévenin Rhymes with Almost Nothing (14 points)

Figure 7.1: Three stage resistor ladder.

(a) (4 points) This circuit has three sources v_0 , v_1 , and v_2 connected to a resistor network. What is the **Thévenin equivalent resistance** R_{th} of this circuit at the terminals labeled v_{out} ? Solution:

$$R_{\rm th} = R$$

We can see this by redrawing the circuit and noting that at each rung of the ladder, there is a resistance of 1R looking left. Simplifying the circuit, rung by rung, eventually leads to the Thévenin equivalent resistance equal to R at the output.







- (b) (4 points) Find the **Thévenin equivalent voltage** ($V_{\text{th}} = v_{\text{out}}$) of this circuit at the terminals labeled v_{out} . You are given the following information:
 - i. The output voltage when v_0 is **on** and *all other sources* are off is $\frac{v_0}{8}$.
 - ii. The output voltage when v_1 is **on** and *all other sources* are off is $\frac{v_1}{4}$.

Solution:

By a similar strategy to the solution to part (a), we can redraw the circuit and note that at each rung of the ladder, there is a resistance of 1*R* looking left. Simplifying the circuit, rung by rung, eventually leads to the Thévenin equivalent voltage, for example, of source v_0 . Likewise, by superposition we can add the voltage contributed by v_1 and v_2 :

$$V_{\rm th} = \frac{v_0}{8} + \frac{v_1}{4} + \frac{v_2}{2}$$



(c) (6 points) Now consider the case when we attach a resistor with resistance 3R to the output of our circuit. We set the voltage inputs so that $v_0 = 8V_{DD}$, $v_1 = 4V_{DD}$, and $v_2 = 2V_{DD}$. Calculate the current i_{out} through the load resistor as a function of V_{DD} and R.



Figure 7.2: Loaded resistor ladder.

Solution:

Using the Thévenin equivalent calculated in part (a) and (b), we see that we can calculate the current using the sum of 3R and the equivalent resistance R.

$$V_{\text{th}} = \frac{v_0}{8} + \frac{v_1}{4} + \frac{v_2}{2} = \frac{8V_{\text{DD}}}{8} + \frac{4V_{\text{DD}}}{4} + \frac{2V_{\text{DD}}}{2} = 3V_{\text{DD}}$$
$$i_{\text{out}} = \frac{V_{\text{th}}}{4R} = \frac{3}{4}\frac{V_{\text{DD}}}{R}$$

8. CompanEE-16A's Microcontroller (18 points)

A company in Berkeley called CompanEE-16A designs and manufactures microcontrollers for electrical engineers and hobbyists around the world. Their current microcontroller model, Version 1.6.A, is poorly documented. It's your job to find out how the microcontroller's pins behave when circuits are attached to them.



Figure 8.1: Microcontroller black box.

- (a) (4 points) First off, you need to find an *equivalent circuit* for the microcontroller's output pins. You have access to a voltmeter (an open circuit that measures the voltage across its terminals) and an ammeter (a short circuit that measures the current through it). You also have a voltage source that displays the current that it is supplying.
 - i. Describe qualitatively how you would find the Thévenin equivalent voltage between pin 1.0 and GND.
 - **Solution:**

Measure the voltage across pin 1.0 and GND with the voltmeter.



ii. Describe qualitatively how you would find the Norton equivalent current between pin 1.0 and GND.

Solution:

Measure the current across pin 1.0 and GND with the ammeter.



iii. Using these results V_{th} and I_{no} , and assuming that $V_{\text{th}} \neq 0$ and $I_{\text{no}} \neq 0$, write the expression that you would use to calculate the equivalent resistance between pin 1.0 and GND. Solution:

Divide V_{th} by I_{no} .

iv. Suppose that you measured $V_{\text{th}} = 0$ V and $I_{\text{no}} = 0$ A, describe what you would need to do to find the equivalent resistance.

Solution:

Apply the voltage source, measure the current, and divide the two results to find the equivalent resistance.

- (b) (4 points) After taking the appropriate measurements using the methods in part (a), you find that $V_{\text{voltmeter}} = 4 \text{ V}$ and $I_{\text{ammeter}} = 2 \text{ mA}$. Calculate V_{th} , R_{to} , and I_{no} .
 - i. *V*_{th} **Solution:**

 $V_{\rm th} = 4 \, {\rm V}$

ii. I_{no}

Solution:

 $I_{\rm no} = 2\,{\rm mA}$

iii. *R*_{th}

Solution:

$$R_{\rm th} = \frac{4\,\rm V}{2\,\rm mA} = 2\,\rm k\Omega$$

iv. *R*_{no} **Solution:**

$$R_{\rm no} = \frac{4\,\rm V}{2\,\rm mA} = 2\,\rm k\Omega$$

(c) (10 points) CompanEE-16A is so pleased with your work that they give you a Version 1.6.A microcontroller for free! Your friend saw your free microcontroller lying on your desk and thought that it was really interesting. He had been working on a mysterious circuit (shown below) for EE105 and wants to connect it onto your board. You connect terminal A of the mysterious circuit to pin 1.0 of the microcontroller and terminal B of the circuit to GND (shown below). **Find the voltage** V_{CD} between terminals C and D in terms of V_{th} .



Solution:

$$v_1 = \frac{3R_{\rm th}}{3R_{\rm th} + R_{\rm th}} \cdot V_{\rm th} = \frac{3}{4}V_{\rm th}$$

Using KCL at node C, we get:

$$\frac{5 \text{ V} - V_{\text{CD}}}{4} = \frac{V_{\text{CD}}}{4} + 4v_1$$

$$5 \text{ V} - V_{\text{CD}} = V_{\text{CD}} + 16v_1$$

$$V_{\text{CD}} = \frac{5 \text{ V} - 16v_1}{2} = \frac{5 \text{ V} - 16 \cdot \frac{3}{4}V_{\text{th}}}{2} = \frac{5}{2} \text{ V} - 6V_{\text{th}}$$

9. Touchy Currents (10 points)

In the capacitive touchscreen lab, you learned how a voltage source and a comparator can be used to determine whether a finger is touching a capacitive touchscreen. In this problem, you will explore how a current source can be used to detect touch.

(a) (4 points) The capacitor C_{screen} is connected to a current source with a constant value I_S as shown in the circuit below. The capacitor is initially uncharged. At time t = 0, the current source switches on. For time $t \ge 0$, the plot of the capacitor voltage $v_1(t)$ is a line. Find the slope of this line in terms of I_s and C_{screen} .



Solution:

 $I_{s} = C_{\text{screen}} \frac{dv_{1}(t)}{dt}$ $\frac{dv_{1}(t)}{dt} = \frac{I_{s}}{C_{\text{screen}}}$

(b) (2 points) Suppose that instead, at time t < 0, a capacitor $C_{\text{finger}} > 0$ is placed in parallel with C_{screen} as shown in the circuit below. Both capacitors are initially uncharged. At time t = 0s, the current source switches on.



Circle the correct plot of $v_1(t)$ and $v_2(t)$, where $v_1(t)$ is the voltage over time when there is no touch and $v_2(t)$ is the voltage over time when there is touch. If the capacitive touch screen is being touched, it is being touched for the entire duration shown in the plot.



Solution:

The slope of $v_2(t)$ should be smaller than the slope of $v_1(t)$.



(c) (4 points) You connect the circuit to a comparator, as shown here:



On the following set of axes, **label the lines** $v_1(t)$ and $v_2(t)$ corresponding to the plot you chose in part (b) and **draw a horizontal line** that represents an appropriate reference voltage V_{ref} that could be used to detect the presence of a touch at a time $t = t_0$.



Solution:





10. Sorry, I don't make puns free of charge. (22 points)

Because of size constraints in modern semiconductor processes, circuit designers often use switches and capacitors instead of resistors to perform certain functions. We will investigate how charge sharing can be used to replace standard resistive circuits. In all parts of this question, assume that there is no leakage and that the capacitors reach steady state in each phase.

(a) (4 points) Consider the following two-phase circuit switched capacitor circuit:



In phase ϕ_1 , find the **voltage across** and the **charge on** *each capacitor* C_1 and C_2 in terms of the input source voltage V_{s_1} and the capacitances C_1 and C_2 .

Solution:

In phase ϕ_1 , the only capacitor connected to V_{s_1} is C_1 . At steady state, its voltage will be equal to V_{s_1} , and its charge will be related to its capacitance C_1 :

$$V_{C_1,\phi_1} = V_{s_1}$$
 $Q_{C_1,\phi_1} = C_1 V_{s_1}$

In phase ϕ_1 , both of the plates of C_2 are connected to ground, so:

$$v_{C_2,\phi_1} = 0$$
 $Q_{C_2,\phi_1} = 0$

(b) (4 points) Now the switches change state, and we look at what happens in phase ϕ_2 . Calculate the **voltage across** both capacitors C_1 and C_2 in terms of the input source voltage V_{s_1} and the capacitances C_1 and C_2 .

Solution:

After switching from phase ϕ_1 to phase ϕ_2 , there is no additional charge added to the system, so the total charge from phase ϕ_1 must equal the total charge in phase ϕ_2 . More specifically, we can describe this using our result from part (a):

$$Q_{\phi_1} = Q_{\phi_2} \implies Q_{\phi_2} = C_1 V_{s_1}$$

Since we know that charge is conserved, we can express our total charge in phase $\phi_2 Q_{\phi_2}$ as a sum of the charges on each capacitor, giving us:

$$Q_{\phi_2} = Q_{C_1,\phi_2} + Q_{C_2,\phi_2}$$

We know that C_1 and C_2 are in parallel, so the voltage across C_1 and C_2 is equal to v_{out_1} .

$$Q_{\phi_2} = C_1 v_{\text{out}_1} + C_2 v_{\text{out}_1}$$

Substituting our previous expression $Q_{\phi_2} = C_1 V_{s_1}$ into our equation, we can solve for the voltage across each capacitor.

$$C_1 V_{s_1} = C_1 v_{\text{out}_1} + C_2 v_{\text{out}_1} \implies v_{\text{out}_1} = v_{C_1,\phi_2} = v_{C_2,\phi_2} = \frac{C_1 V_{s_1}}{C_1 + C_2}$$

(c) (4 points) In the following circuit, first, all switches labeled ϕ_1 are closed, and all switches labeled ϕ_2 are opened. Some time after the circuit reaches steady state, all switches labeled ϕ_2 are closed, and all switches labeled ϕ_1 are opened. Find the voltage v_{out_2} at steady state only in the second phase ϕ_2 as a function of the input source voltage V_{s_2} and the capacitances C_3 and C_4 .



Solution:

In phase ϕ_1 , C_3 is connected to V_{s_2} , so its voltage will be equal to V_{s_2} , and its charge will be equal to $Q_{C_3,\phi_1} = C_3 V_{s_2}$. C_4 is shorted, so its charge will be equal to $Q_{C_4,\phi_1} = 0$. In phase ϕ_2 , both plates of C_3 are connected to ground, so its voltage is zero. Therefore, $Q_{C_3,\phi_2} = 0$.

However, since charge is conserved, all of the negative charges on the right plate of C_3 must have been transferred to the left plate of C_4 in phase ϕ_2 . Therefore,

$$Q_{C_4,\phi_2} = Q_{C_3,\phi_1} = C_3 V_{s_2} \implies v_{\text{out}_2} = \frac{Q_{C_4,\phi_2}}{C_4} = \frac{C_3 V_{s_2}}{C_4}.$$

(d) (10 points) Now we combine both of the previous circuits into one. First, all switches labeled ϕ_1 are closed, and all switches labeled ϕ_2 are opened. Some time after the circuit reaches steady state, all switches labeled ϕ_2 are closed, and all switches labeled ϕ_1 are opened. Find the voltage v_{out} at steady state only in the second phase ϕ_2 as a function of the input source voltages V_{s_1} and V_{s_2} and the capacitances C_1, C_2, C_3 , and C_4 .



Solution:

In phase ϕ_1 , we know from part (c) that $Q_{3,\phi_1} = C_3 V_{s_2}$. Using the sign convention for C_3 and C_4 that the plates connected to the negative terminal of the op-amp are negative, we get $Q_{3,\phi_1} = Q_{3,\phi_2} + Q_{4,\phi_2}$ since charge is conserved.

In phase ϕ_2 , we know from part (b) that $V^+ = \frac{C_1 V_{s_1}}{C_1 + C_2}$. Applying the Golden Rules, we know that $V^- = \frac{C_1 V_{s_1}}{C_1 + C_2}$.

$$Q_{3,\phi_2} = C_3(0 - V^-) = C_3 \left(0 - \frac{C_1 V_{s_1}}{C_1 + C_2} \right)$$
$$Q_{4,\phi_2} = C_4(v_{\text{out}} - V^-) = C_4 \left(v_{\text{out}} - \frac{C_1 V_{s_1}}{C_1 + C_2} \right)$$

$$Q_{3,\phi_1} = Q_{3,\phi_2} + Q_{4,\phi_2}$$

$$C_3 V_{s_2} = C_3 \left(0 - \frac{C_1 V_{s_1}}{C_1 + C_2} \right) + C_4 \left(v_{\text{out}} - \frac{C_1 V_{s_1}}{C_1 + C_2} \right)$$

$$C_3 V_{s_2} + (C_3 + C_4) \frac{C_1 V_{s_1}}{C_1 + C_2} = C_4 v_{\text{out}}$$

$$v_{\text{out}} = \frac{C_3 V_{s_2}}{C_4} + \left(1 + \frac{C_3}{C_4} \right) \frac{C_1 V_{s_1}}{C_1 + C_2}$$

Extra page for scratchwork.

If you want any work on this page to be graded, please refer to this page on the problem's main page.