UNIVERSITY OF CALIFORNIA, BERKELEY
College of Engineering
Department of Electrical Engineering and Computer Sciences
Fall 2015

EE 105: Microelectronic Devices and Circuits — Prof. Ming Wu

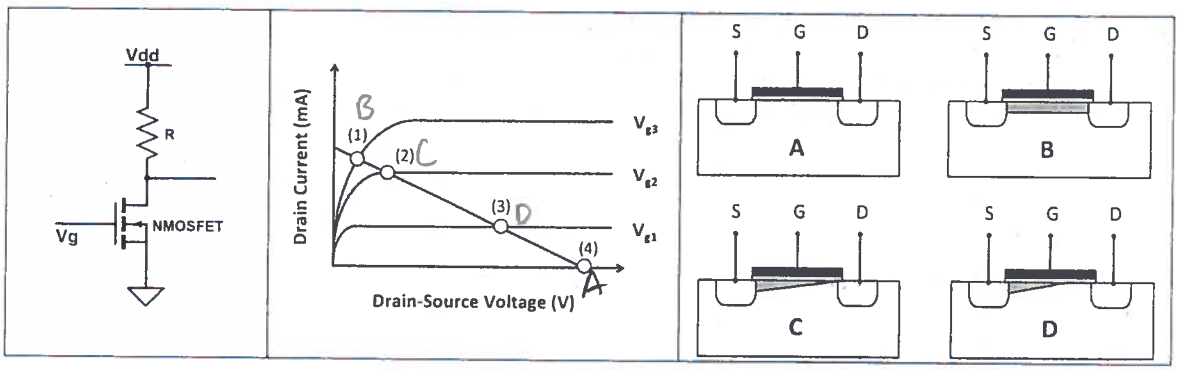
Final EXAMINATION
Time allotted: 180 minutes

INSTRUCTIONS:
1. **SHOW YOUR WORK. (Make your methods clear to the grader!)**
2. **Clearly mark (underline or box) your answers.**
3. **Specify the units of your answer to receive full credit.**
4. **Unless stated in the problem, use the values of physical constants provided below.**
5. **You can use approximations within 10% accuracy any time (unless stated otherwise).**

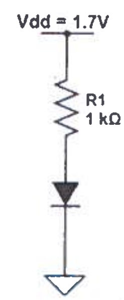
Commonly used constants and physical parameters:		
Electronic charge	q	1.6×10^{-19} C
Boltzmann's constant	k	8.62×10^{-5} eV/K
Thermal voltage at 300K	$V_T = kT/q$	0.025 V
Intrinsic carrier concentration of Si	n_i	$1.5\text{x}10^{10}$ cm^{-3}
Relative permittivity of Si	$\epsilon_{r,Si}$	11.7
Relative permittivity of SiO_2	$\epsilon_{r,ox}$	3.9
Vacuum permittivity	ϵ_0	$8.854\text{x}10^{-14}$ F/cm

Problems	Points	Grade
1	10	
2	10	
3	15	
4	25	
5	30	
6	20	
7	10	
8	15	
9	15	
Total	150	

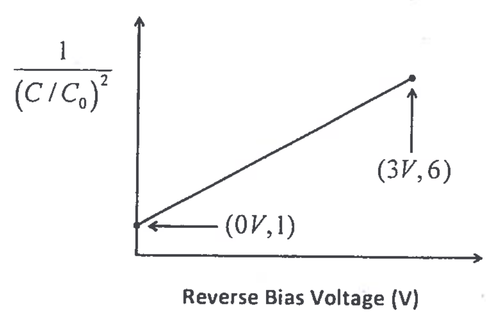
1. A simple MOSFET CS amplifier circuit, the measured I-V curves of MOSFET and the load line of the resistor are shown below. The intercept points indicate the bias points, from (1) to (4), depending on the gate bias. Also shown are the schematic illustrations of electron distributions in an NMOSFET under various bias conditions, from A to D. For each question below, select a bias point from the I-V curve, e.g., (1), (2), …, and an electron distribution from the schematics, e.g., A, B, …, that corresponds to the MOSFET's region of operation:
   a. MOSFET in cut-off
   b. MOSFET in saturation region
   c. MOSFET at pinch off point
   d. MOSFET in triode region



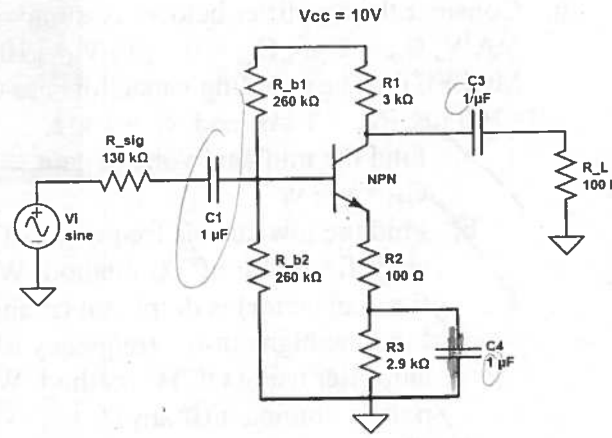
2. Consider the diode circuit on the right.
   a. Find the current through diode. Assume the voltage drop across the diode is 0.7V.
   b. For more precise calculation, use the diode equation with $I_D = I_S e^{V/V_T}$, where $I_S = 10^{-16} A$ (reverse saturation current). Find the voltage drop across the diode and the current. (*The voltage should be accurate to < 5 mV, and current should be accurate to within 10 μA).*



3. The built-in potential of a pn junction can be extracted from capacitance measurement. The data on the right shows the measured $1/C^2$ versus reverse bias voltage, V_R. The capacitance has been normalized to the zero-bias capacitance, C_0.
   a. Find the built-in potential of the pn junction.
   b. If the doping concentrations of both n- and p-type semiconductors are increased by 10x, how much does the built-in voltage change (in V)?
   c. What is the ratio of the zero-bias capacitances for the new and original pn junctions?



4. The BJT below has a current gain of $\beta = 100$, an Early voltage of $V_A = 100V$, and $v_{CE,SAT} = 0.3\ V$.



a. What is the amplifier configuration?

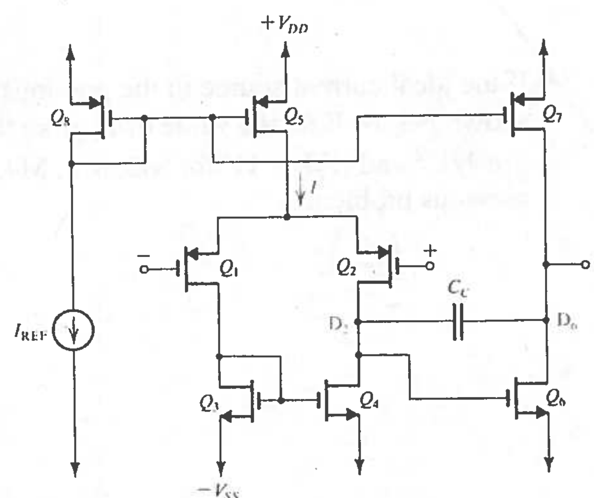
b. Find the DC bias current of the BJT and the collector-emitter voltage. You can assume $V_A = \infty$ for DC analysis.

c. What is the input resistance of the amplifier (not including the signal resistance)?

d. What is the overall gain of the amplifier including the signal resistance and load resistance?

e. What is the maximum output voltage swing? (*Note: output swing is defined as the smaller of the upward and downward voltage swings*)

5. Consider the circuit below. Let $I_{REF} = 100\ \mu A$, $|V_t| = 1$ V for all devices, $\mu_n C_{ox} = 200\ \mu A/V^2$, $\mu_p C_{ox} = 50\ \mu A/V^2$, $|V_A| = 10$ V for all devices, $V_{DD} = V_{SS} = 5$ V. Assume the W/L of all transistors are 10/1. Neglect the effect of V_A on the bias currents.



a. Find the overdrive voltage of all transistors.

b. Find the voltage gain of the differential stage (first stage, output at D_2).

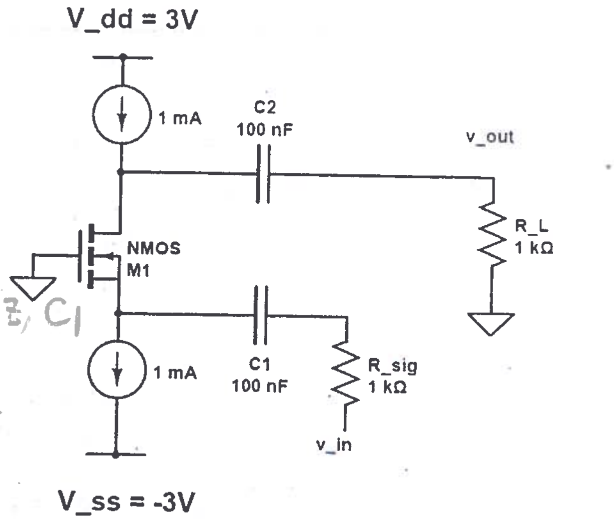
c. Find the voltage gain of the second stage (output at D_6).

d. Find the total gain.

e. Find the range of common mode voltage applied to the inputs (+ and – terminals).

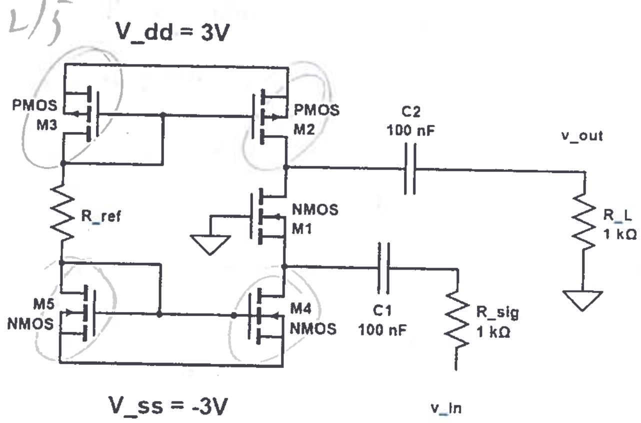
f. If the DC voltages at both inputs (+ and –) are 0 V, what is the maximum output voltage swing at D_2?

6. Consider the amplifier below. Assume $g_m = 1$ mA/V, $C_{gs} = 2$ pF, $C_{gd} = 0.2$ pF, $V_A = 10$V for all MOSFETs. The coupling capacitors are $C_1 = C_2$ =100 nF, $R_{sig} = 1$ kΩ, and $R_L = 1$ kΩ.
   a. Find the midband voltage gain, $G_V = v_o / v_i$
   b. Find the low cut-off frequency of the amplifier using SCTC method. Which pole (i.e., capacitor) is dominant (if any)? 4.7KHz, C_1
   c. Find the high cut-off frequency of the amplifier using OCTC method. Which pole is dominant (if any)? 1GHz, C_{gd}.
   d. Plot the frequency response of the amplifier showing the low-cutoff, and high cutoff response. The vertical axis should be dB, and horizontal axis should be in Hz.

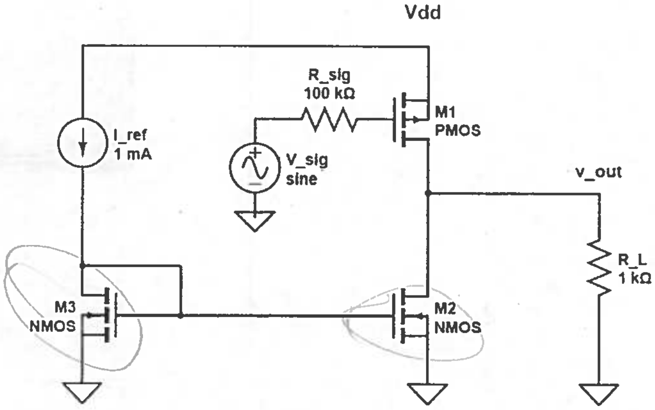


7. If the ideal current source in the previous Problem is replaced by MOSFET current source, as shown below. Find the value of R_{ref} so the bias current in M1 is 1 mA. Assume $k_n = k_p = 2mA/V^2$ and $|V_t| = 1V$ for M2, M3, M4, and M5. Other parameters are the same as the previous problem.

$\left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_3 = \cdots = \left(\frac{W}{L}\right)_5$



8. This problem deals with high frequency response of the following amplifier. Assume all transistors have $C_{gs} = 4$ pF, $C_{gd} = 0.2$ pF, $g_m = 1mA/V$ and $r_o = 20k\Omega$. $R_{sig} =$ 100 kΩ, and $R_L = 1$ kΩ.
   a. What configuration is this amplifier?
   b. What is the low frequency gain of the amplifier?
   c. What is the high cut-off frequency of the amplifier? Which pole is dominant (if any)?



9. For the circuit here, $\mu_n C_{ox} = 400$ μA/V², $\mu_p C_{ox} = 100$ μA/V², $|V_A| = 10$ V and $|V_t| = 1$ V for both M1 and M2, V_{DD} =5 V. W/L = 10 for M1, and W/L = 40 for M2. Neglect the effect of V_A on the bias currents.
   a. What configuration is this amplifier?
   b. Find the voltage gain.
   c. Find the output resistance.