UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
and Computer Sciences

	Final	**EECS 240**
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*Clearly **mark results** with box around. No credit for ambiguous solutions. Show derivations. Do all calculations on exam sheet and return exam sheet. Exam is "open book, open notes". Good luck!*

Device Parameters (all problems unless otherwise noted):

C	NMOS/NPN	PMOS/PNP
C_{ox}	2 fF/μm^2	2 fF/μm^2
μ	μ_n = 500 cm^2/V-s	μ_p = 200 cm^2/V-s
V_{TH}	1 V	-1 V
λ at L = 1μm	0.1 V^{-1}	0.1 V^{-1}
K_f	10^{-24} V^{2}F	0.5 x 10^{-24} V^{2}F
C_{ol}	0 fF/μm	0 fF/μm
$V_{BE(on)}$	0.7V	-0.7V
$V_{CE(sat)}$	200mV	-200mV
r_b	0Ω	0Ω
β_f	100	100

Assume square-law characteristics for the MOS devices.

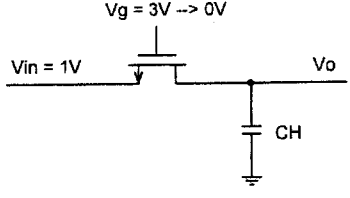
Name: _____ (1 point)

Problem	Score
1	
2	
3	
4	
Total	

1. **MOS Sample & Hold**

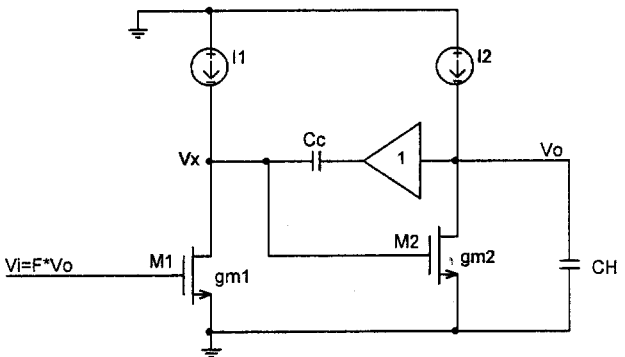
Calculate the minimum cutoff frequency f_T required for the sampling transistor for a 50MHz acquisition bandwidth and 20mV charge injection onto C_H. Assume worst-case conditions, i.e. that all channel charge is injected onto C_H.

Give both an algebraic expression and numerical value for the cutoff fequency.



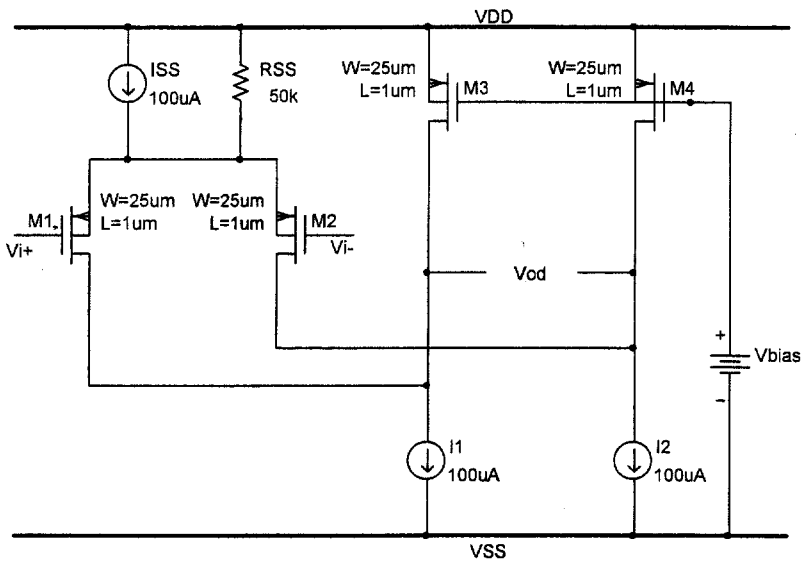
2. **Amplifier Output Noise**

Derive an expression for the standard deviation of the noise voltage on node V_O (integrated over all frequencies) that is due to the thermal drain current noise from M2. Ignore all other noise sources, transistor output resistance, and all capacitors except C_C and C_L. The unity-gain buffer has the characteristics of an ideal source follower.



3. **Power-Supply Rejection Ratio**

Calculate the worst-case power supply rejection ratio (PSRR) at low frequency with respect to V_{DD} of the folded cascode shown below assuming a threshold voltage mismatch of 10mV between all nominally matched pairs of transistors (i.e. M1-M2 and M3-M4).
Assume $V_{i+}=V_{i-}$. The common-mode feedback circuit is not shown (but assume it's there).
Give both an algebraic expression for the PSRR (in terms of g_m, Δg_m, R_{SS}), and the numerical value.

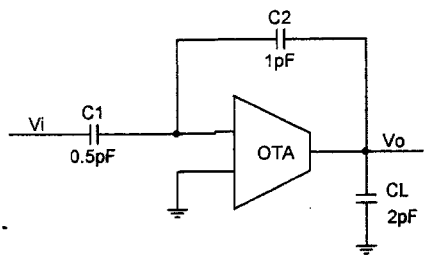


4. **Settling Time**

In the circuit shown below, capacitors C1 and C2 are discharged, then a 4V step is applied at the input V_i.

a) What is the relative error of the output when all transients have died?

b) Compute the settling time for 0.1% settling accuracy assuming infinite open-loop gain. Assume that the entire biasing current I_{SS} is available for slewing and that the transition between slewing and linear settling is abrupt.



Single-Stage
OTA Specifications:

avo = 1000

gm1=gm2 = 1mS

Iss = 200uA

Cin = 1pF