| Prob. | Score |
|---|---|
| 1A | /10 |
| 1B | /20 |
| 1C | /20 |
| 2 | /15 |
| 3 | /35 |
| Total | |

EECS140
Fall 2009
Midterm 2

Name KEY

SID_____

For this test, assume the standard ee140 device process parameters unless otherwise indicated.

1_) In some non-standard process you have a two-stage CMOS op-amp with the following specs:

- $R_{o1}$= 100k, $G_{m1}$=1ms, $C_1$=100f
- $R_{o2}$ = 10k, $G_{m2}$=10mS, $C_2$=1pF

You want to use the amplifier in unity gain feedback.

1A) If the compensation capacitor $C_C$ is zero, what is the frequency of the first and second poles? What is the unity gain frequency? What is the phase margin?

| | | |
|---|---|---|
| 2 | $\omega_{p1}$ | 100M rad/sec |
| 2 | $\omega_{p2}$ | 100M rad/sec |
| 3 | $\omega_u$ | 10 G rad/sec |
| 3 | PM | 0 |

$G_{m1}R_{o1} = 100$

$G_{m2}R_{o2} = 100$

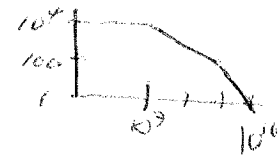
1B) If you were to add 10fF to $C_C$, what is the change in the two pole frequencies, and the unity gain frequency that would result? (I want an exact answer in radians/sec) In this case, what is the feedback factor f for which this amplifier has 45 degrees of phase margin?

| | | |
|---|---|---|
| S | $\omega_{p1}$ | $10^7$ or $9\times10^6$ w/ $C_1$ |
| S | $\omega_{p2}$ | $10^9$ or $9\times10^8$ w/ $C_1$ and $C_2$ |
| S | $\omega_u$ | $10^{10}$ or $9\times10^9$ |
| S | f | 0.01 |

$(10f)(10i) = 100pF$

$10^5 \cdot 10^{-12} = 10^{-7}$ s

$\omega_{p1} \to 10^7$

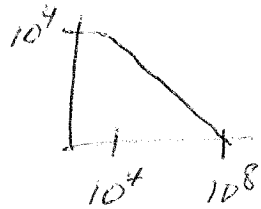



1C) Starting from the original $C_C$=0 case again, if you want to get 45 degrees of phase margin in unity gain feedback, you can add capacitance to one of three nodes. How much capacitance would you need to add to $C_1$ to get 45 degrees of phase margin? What if you only added capacitance to $C_2$? What if you only added capacitance to $C_c$, with a series resistor $R_Z$? What value should you use for $R_Z$?

$\omega_{p1} = 10^5$

$\omega_{p2} = 10^8$

| | | |
|---|---|---|
| S | Add to $C_1$ | 1,000 pF = 1nF |
| S | Add to $C_2$ | 10nF |
| S | Add to $C_c$ | ~~10pF~~ 100fF |
| S | $R_Z$ | $\frac{1}{C\omega_{mn}} = 100\ \Omega$ |




$R_{z_1} = 10^5$

$10^5 \cdot C_1 = 10^{-4}$

$C_1 = 10^{-9}$

2_) You are designing a two-stage CMOS op-amp, and you need a gain error of less than 1% in unity gain feedback at 10MHz. Your amp needs to drive a load capacitance of 10pF, and you have found that you need a 2pF compensation capacitor which gives you a phase margin of 60 degrees. All transistors are biased with 0.5V $V_{DSAT}$, and all have the same channel length.
What is the minimum unity gain frequency of your amplifier?
What is the minimum tail current of your differential pair?
What is the minimum channel length for your transistors if you want an overall gain of 2500?

| | | |
|---|---|---|
| 5 | $\omega_{u,\,min}$ | $10^9 \cdot 2\pi$ |
| 5 | $I_{tail,\,min}$ | $1mA \cdot 2\pi$ |
| 5 | $L_{min}$ | $2.5\,\mu m$ |

$C_L = 10p$

$C_c = 2p$

$\frac{1}{AF} = 1\%$ @ $10^7$ Hz $\quad f=1 \Rightarrow \omega_u = 10^9 \cdot 2\pi$

$g_{m1,min} = \omega_u C_c = 2\pi 10^9 \cdot 2\times10^{-12} = 2\pi 2mS = \frac{2I_D}{V_{dsat}}$

$I_{d1,min} = \frac{V_{dsat}}{2} \times 2mS = 0.5mA$

$I_{tail} = 2 I_{d1,min}$

$A_{v1} = \frac{1}{\lambda V_{dsat}} = 20 \cdot \frac{L}{1\mu m}$

$A_{v2} = \frac{1}{\lambda V_{dsat}}$

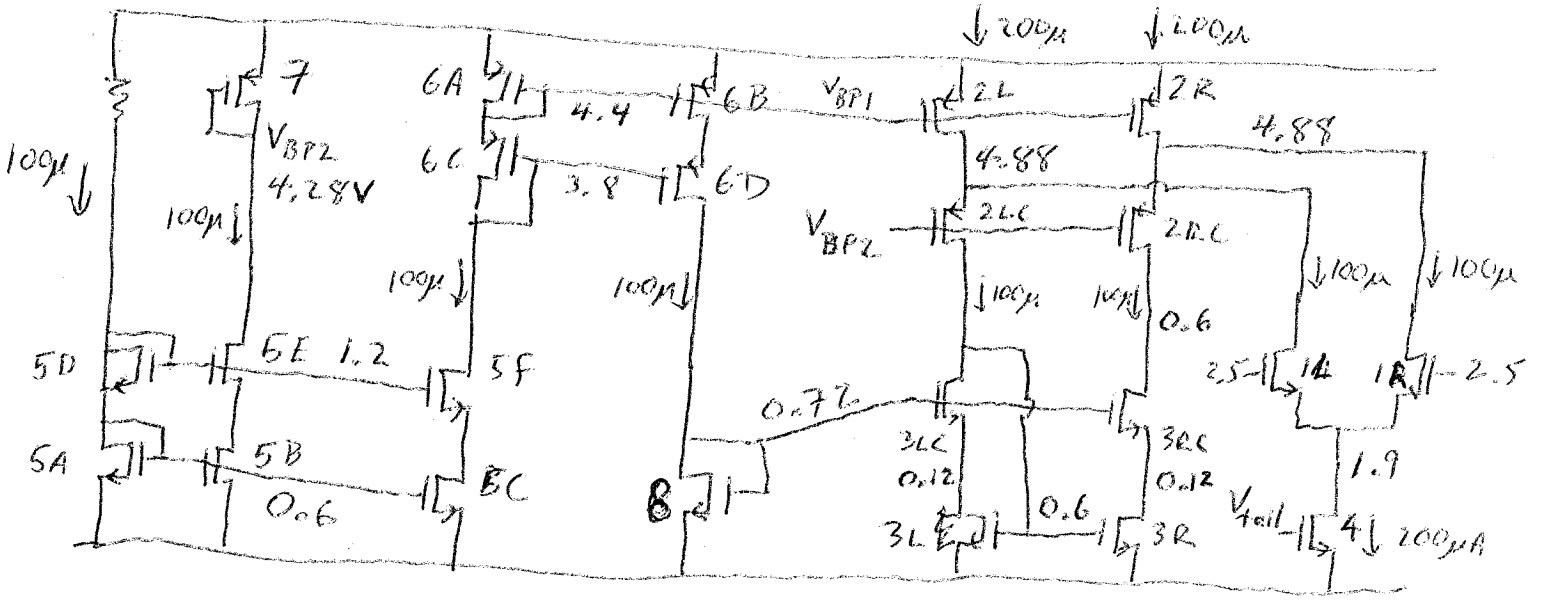
3_) Design a CMOS folded cascode amplifier with the following specs:

- Input common mode range includes the top rail
- Output swing to within 300mV of both rails
- 100uA drain current in all transistors in the signal path
- 5V single-sided supply
- all channels are 1um Long ($L = 1\mu m$)

You may use one resistor in the bias circuit for your design. All other devices must be transistors.

Draw your amplifier and it's complete bias circuit. Maybe draw it on scratch paper first so that you can draw it neatly here!

Assume that the input common mode is biased at 2.5V, and **label all node voltages and all branch currents**.




choose $|V_{dsat}| = 100mV$ for 1L/R, 2L/R, 2LC/RC, 3L/R/LC/RC
5 A/B/C/D/E/F, 6 A B C D

$|V_{dsat}| = \sqrt{5}\,100mV$ for 7, 8

$= (2.24)mV$

For each device (or pair of devices if they are identical) in your design, calculate the device width, drain current, saturation voltage, transconductance, and output resistance. LABEL YOUR CIRCUIT DIAGRAM with W/L and $V_{DSAT}$ values for each transistor.

| name | W | $I_d$ | $V_{DSAT}$ | $g_m$ | $r_o$ |
|---|---|---|---|---|---|
| M1 L/R | 100µ | 100µ | 100m | 0.2mS | 100K |
| 3L,R,4,5RC | 100µ | 100µ | 100m | 0.2mS | 100K |
| 4 | 200µ | 200µ | 100m | 0.4mS | 50K |
| 5 * | 100µ | 100µ | 100m | 0.2mS | 100K |
| 8 | 20 | 100µ | 22.4m | 90µS | 100K |
| 2LC,RC | 200 | 100µ | -100m | 0.2m | 100K |
| 6ABCD | 200 | 100µ | -100m | 0.2m | 100K |
| 2L,2R | 400µ | 200µ | -100m | 0.4m | 50K |
| 7 | 80 | 100µ | -22.4m | 90µS | 100K |
| | | | | | |

↑ 10x value shown

What is the output impedance of your op-amp?
What is the gain of your op-amp?

for NMOS, $I_d = 100\mu$, $V_{dsat} = 100mV \Rightarrow \frac{W}{L} = 100$

this applies to 1&R, 3L, R, 4, 5, RC and 5ABCDEFG

M4 needs 2x the current
M8 chosen to be 5x smaller

for PMOS $I_d = 100\mu$ $V_{dsat} = 100mV \Rightarrow \frac{W}{L} = 200$

this applies to 2LC, RC and 6ABCD

M2L, 2R need to be 2x bigger

M7 chosen 5x smaller