University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Sciences

EECS151/251A — V. Stojanovic, J. Wawrzynek
Fall 2015 — 10/13/15

Midterm Exam

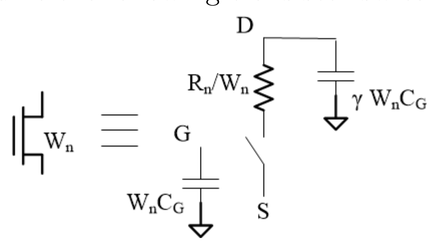
Name: ______________________________

ID number: ______________________________

Class (EECS151 or EECS251A): ______________________________

This is a *closed-book* exam, but you are allowed a single sheet of notes. No calculators, phones, pads, or laptops. Each question is marked with its number of points (one point per expected minute of time), in the form "[EECS151 points / EECS251A points]" Start by answering the easier questions then move on to the more difficult ones. You can tear off the spare pages at the end of the booklet and/or use the backs of the pages to work out your answers. Neatly copy your answer to the allocated places. **Neatness counts.** We will deduct points if we need to work hard to understand your answer.

For all relevant problems, assume the following transistor switch model:



Put your name and SID on each page.

problem	151 max	251A max	score
1	10pts	14pts	
2	7pts	7pts	
3	8pts	12pts	
4	6pts	10pts	
5	9pts	9pts	
6	7pts	11pts	
7	10pts	10pts	
8	10pts	15pts	
Total	67pts	88pts	

1. [10pts/14pts] Combinational Logic Design.

Consider the design of the combinational logic block that takes as input a 3-bit two's-complement integer, X, and produces as output another 3-bit two's-complement integer representing the *absolute value of* X. Assume that the input integer is in the range of $-3 \le X \le 3$.

(a) [4pts] In the space below draw the truth-table that represents the values of the output signals, y_2 (the most significant bit), y_1, and y_0 (the least significant bit) as a function of the inputs x_2, x_1, x_0. Beneath your truth table, write the sum-of-products canonical form for the output signals.

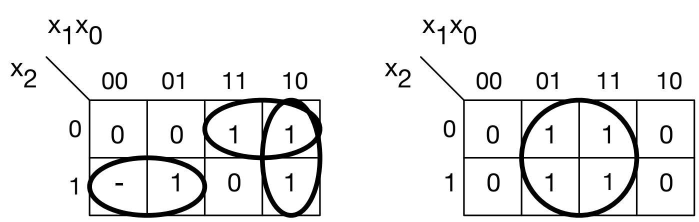
$x_2x_1x_0$	$y_2y_1y_0$
000	000
001	001
010	010
011	011
100	- - -
101	011
110	010
111	001

$y_0 = x_2'x_1'x_0 + x_2'x_1x_0 + x_2x_1'x_0 + x_2x_1x_0$

$y_1 = x_2'x_1x_0' + x_2'x_1x_0 + x_2x_1'x_0 + x_2x_1x_0'$

$y_2 = 0$

(b) [6pts] In the space below use K-maps to derive minimized sum-of-product forms for the output signals.



$y_1 = x_2'x_1 + x_1x_0' + x_2x_1'$ $\qquad$ $y_0 = x_0$

(c) [4pts] **For 251A students only:** Starting from the canonical forms use algebraic manipulation to find the optimized logic equations.

$$
\begin{aligned}
y_0 &= \bar{x_2}\bar{x_1}x_0 + \bar{x_2}x_1x_0 + x_2\bar{x_1}x_0 + x_2x_1x_0 \\
&= \bar{x_2}x_0(\bar{x_1} + x_1) + x_2x_0(\bar{x_1} + x_1) \\
&= \bar{x_2}x_0 + x_2x_0 \\
&= x_0(\bar{x_2} + x_2) \\
&= x_0
\end{aligned}
$$

For y_1 we can assume that $x_2\bar{x_1}\bar{x_0} = 1$ because it is a “don’t care”.

$$
\begin{aligned}
y_1 &= \bar{x_2}x_1\bar{x_0} + \bar{x_2}x_1x_0 + x_2\bar{x_1}x_0 + x_2x_1\bar{x_0} \\
&= \bar{x_2}x_1\bar{x_0} + \bar{x_2}x_1x_0 + x_2\bar{x_1}x_0 + x_2x_1\bar{x_0} + (\bar{x_2}x_1\bar{x_0} + x_2\bar{x_1}\bar{x_0}) \\
&= \bar{x_2}x_1\bar{x_0} + \bar{x_2}x_1x_0 + x_2x_1\bar{x_0} + \bar{x_2}x_1\bar{x_0} + x_2\bar{x_1}x_0 + x_2\bar{x_1}\bar{x_0} \\
&= \bar{x_2}x_1(\bar{x_0} + x_0) + (\bar{x_2} + x_2)x_1\bar{x_0} + x_2\bar{x_1}(x_0 + \bar{x_0}) \\
&= \bar{x_2}x_1 + x_1\bar{x_0} + x_2\bar{x_1}
\end{aligned}
$$

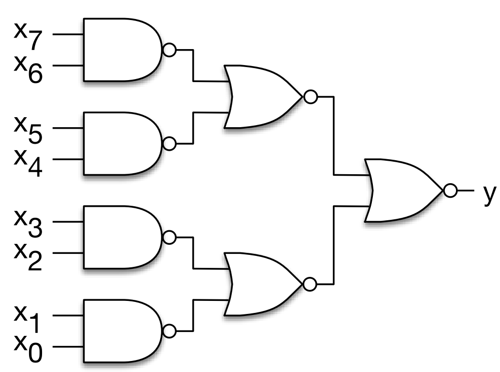
2. [7pts/7pts] Logic Gates.

For the combinational logic function:

$$y = (\bar{x_7} + \bar{x_6} + \bar{x_5} + \bar{x_4})(\bar{x_3} + \bar{x_2} + \bar{x_1} + \bar{x_0}),$$

draw a minimal gate-level diagram for y as a function of x_7, x_6, x_5, x_4, x_3, x_2, x_1, and x_0 using only inverters and 2-input NANDs and NORs.

$$\begin{aligned}
y &= (\overline{x_7} + \overline{x_6} + \overline{x_5} + \overline{x_4})(\overline{x_3} + \overline{x_2} + \overline{x_1} + \overline{x_0}) \\
&= (\overline{x_7 x_6} + \overline{x_5 x_4})(\overline{x_3 x_2} + \overline{x_1 x_0}) \\
&= \overline{\overline{(\overline{x_7 x_6} + \overline{x_5 x_4})(\overline{x_3 x_2} + \overline{x_1 x_0})}} \\
&= \overline{\overline{\overline{x_7 x_6} + \overline{x_5 x_4}} + \overline{\overline{x_3 x_2} + \overline{x_1 x_0}}} \\
&= ((x_7 \ nand \ x_6) \ nor \ (x_5 \ nand \ x_4)) \ nor \ ((x_3 \ nand \ x_2) \ nor \ (x_1 \ nand \ x_0))
\end{aligned}$$

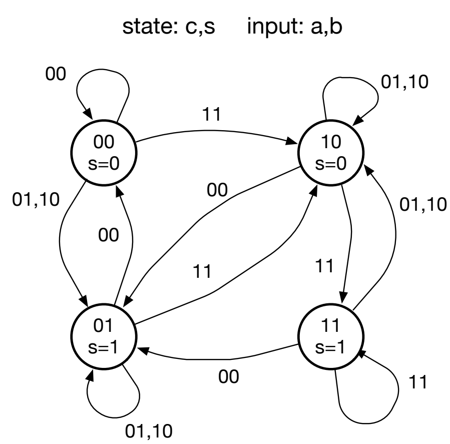


3. [8pts/12pts] FSMs.

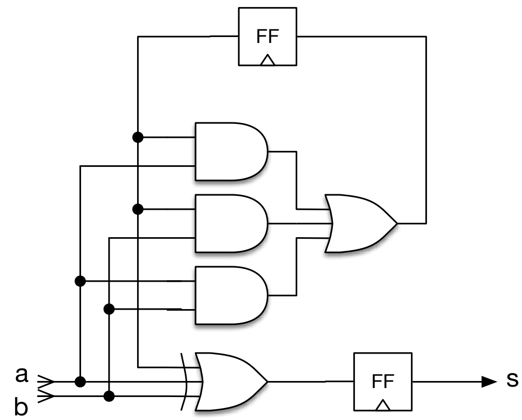
Below is the Verilog description of a bit-serial adder. The circuit adds 2 integers, A and B, generating one bit of the sum per clock cycle by taking one bit from each of the integers (least significant bit first). An add operation concludes when the rst signal is asserted on the same clock cycle as the most significant bit of the inputs.

```
module BSAdd (clk, rst, a, b, s);
input clk, rst,
input a, b;
output s;

reg s, c;
wire nc, ns;

always @ (posedge clk)
  begin
    s <= ns;
    if (rst) c <= 1b'0; else c <= nc;
  end

assign {nc, ns} = a + b + c;

endmodule
```

In the space below draw the state-transistion-diagram for a finite state machine that matches the behavior of the above circuit.



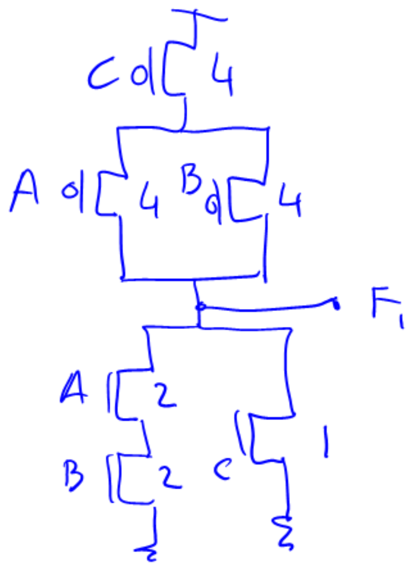
[4pts] **For 251A students only:** Draw the circuit diagram matching the Verilog description using flip-flops and simple logic gates.



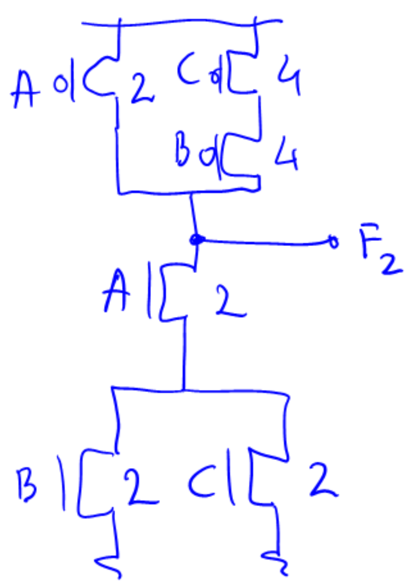
4. [6pts/10pts] CMOS logic.

Draw the single, complex gate, transistor level CMOS representation of the following functions. Size the transistors in each stage for equal worst-case pull-up and pull-down strength (i.e. $R_{eq,pu} = R_{eq,pd}$) to be the same as those of the reference inverter with equal pull-down and pull-up strength ($W_p = 2W_n$). Label the sizes in units of W_n on each schematic.

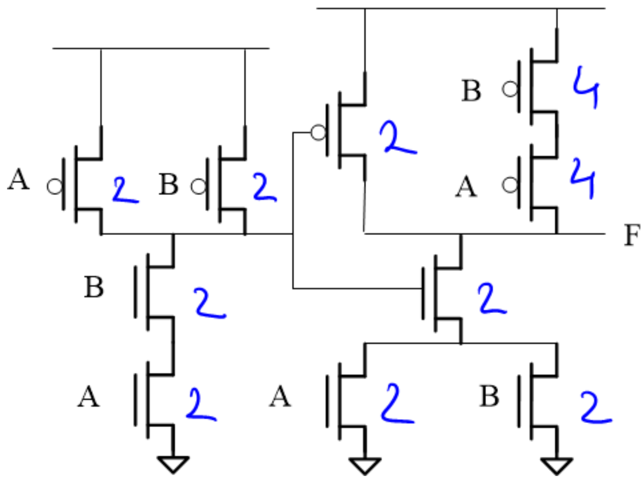
(a) [3pts] $F_1 = \overline{(AB + C)}$.



(b) [3pts] $F_2 = \bar{A} + \bar{B}\bar{C}$.



(c) [4pts] **For 251A students only:** Which 2-input Boolean logic function does the circuit below represent? Make sure to simplify the Boolean expression to the Boolean function you can recognize.



$$F = \overline{\overline{AB} \cdot (A+B)} = AB + \overline{A+B} = AB + \overline{A}\,\overline{B}$$

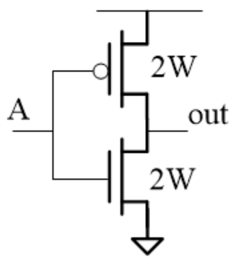
$$= A \text{ XNOR } B$$

$$= \overline{A \oplus B}$$

5. [9pts/9pts] Gate Sizing and Logical Effort.

Calculate the Logical Effort (LE) for each input (worst-case pull-down and pull-up path - e.g. $LE_{A,pup}$, $LE_{A,pdn}$) of the gates below. Assume that in this technology PMOS has twice worse mobility than NMOS (i.e. for $W_p = W_n$, $R_p = 2R_n$).

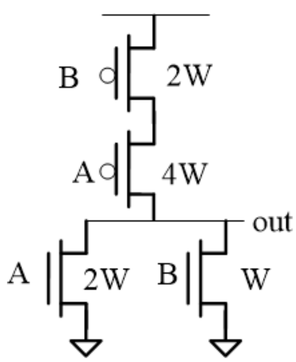
(a) [4pts]



$$LE_{PD} = \frac{\frac{1}{2W} \cdot 4W}{\frac{1}{W} \cdot 3W} = \frac{2}{3}$$

$$LE_{PU} = \frac{\frac{2}{2W} \cdot 4W}{\frac{2}{2W} \cdot 3W} = \frac{4}{3}$$

(b) [5pts]



$$LE_{A\,PD} = \frac{\frac{1}{2W} \cdot 6W}{\frac{1}{W} \cdot 3W} = 1$$

$$LE_{A\,PU} = \frac{\left(\frac{2}{2W} + \frac{2}{4W}\right) \cdot 6W}{\frac{2}{2W} \cdot 3W} = 3$$

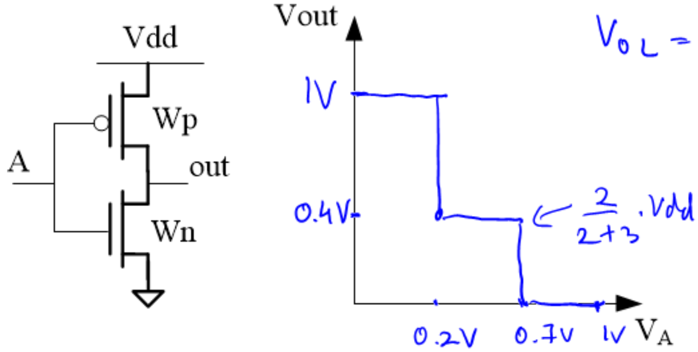
$$LE_{B\,PD} = \frac{\frac{1}{W} \cdot 3W}{\frac{1}{W} \cdot 3W} = 1$$

$$LE_{B\,PU} = \frac{\left(\frac{2}{2W} + \frac{2}{4W}\right) \cdot 3W}{\frac{2}{2W} \cdot 3W} = \frac{3}{2}$$

6. [7pts/11pts] Voltage Transfer Characteristics (VTCs).

The technology has the following parameters: $V_{th,N} = 0.2V$ and $|V_{th,P}| = 0.3V$, $R_n = 2k\Omega * \mu m$, $R_p = 3k\Omega * \mu m$ at $V_{dd} = 1V$. Draw the voltage transfer characteristic (V_{out} vs V_A) of the gates below with $W_p = W_n = 1\mu m$.

(a) [4pts] Draw the VTC and determine V_{OL}, V_{IL}, V_{OH}, V_{IH} and noise margins NM_H and NM_L.



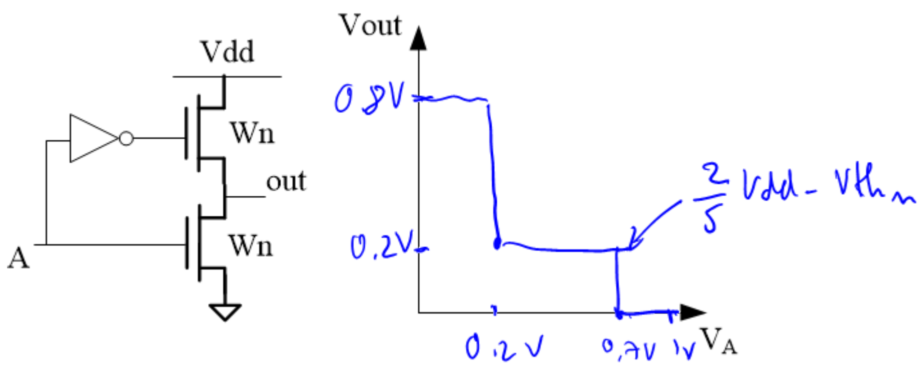
$V_{OH} = 1V$ $V_{IH} = 0.7V$

$V_{OL} = 0V$ $V_{IL} = 0.2V$

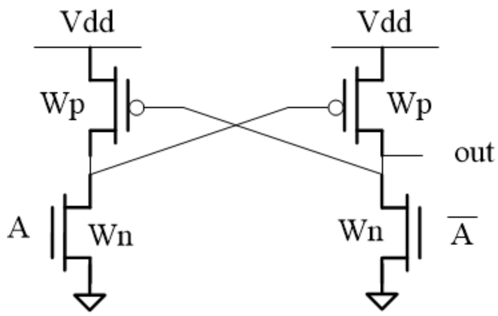
$NM_H = 0.3V$

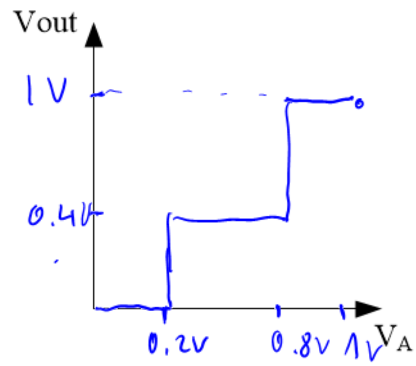
$NM_L = 0.2V$

(b) [3pts]



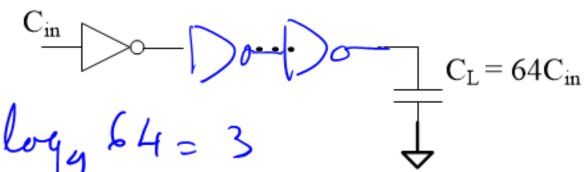
(c) [4pts] **For 251A students only:** Assume that $V_{\bar{A}} = V_{dd} - V_A$.





7. [10pts/10pts] Gates and Wires.

(a) [4pts] Calculate the optimal number of inserted inverter stages and the delay normalized to the intrinsic inverter delay t_{p0} for the following problem (assume γ = 1):



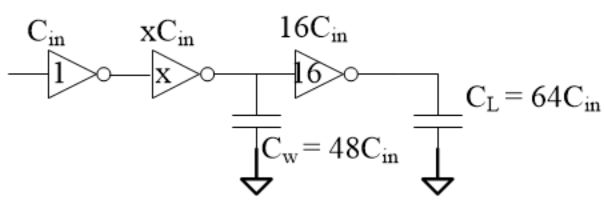
$N_{opt} = \log_4 64 = 3$

$N_{inserted} = 2$

$EF = \sqrt[3]{64} = 4$

$D = 3(1+4) = 15$

(b) [6pts] In the circuit below calculate the optimal size of the middle inverter (x) for minimum total delay:



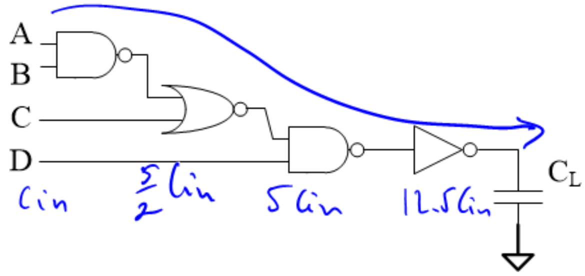
$$D = 1 + x + 1 + \frac{(16+48)C_{in}}{x\,C_{in}} + 1 + \frac{64\,C_{in}}{16\,C_{in}}$$

$$D = 7 + x + \frac{64}{x}$$

$$\frac{\partial D}{\partial x} = 0 = 1 - \frac{64}{x^2} \Rightarrow x = \sqrt{64} = 8$$

8. [10pts/15pts] Sizing the Logic Path.

For the circuit drawn below determine:



(a) [2pts] Mark the critical path in the circuit.

(b) [3pts] Calculate the path logical effort for the critical path in this circuit.

$$\Pi LE = \frac{4}{3}\cdot\frac{5}{3}\cdot\frac{4}{3} = \frac{80}{27}$$

(c) [5pts] Size the gates for minimum delay ignoring wires and mark the value of the input capacitance of each gate. The first gate in the critical path has input capacitance C_{in}, and the load capacitance at the output is $C_L = \frac{125}{3}C_{in}$.

$$EF = \sqrt[4]{\Pi LE \cdot FO} = \sqrt[4]{\frac{80}{27}\cdot\frac{125}{3}} = \frac{2\cdot 5}{3} = \frac{10}{3}$$

$$\frac{\frac{125}{3}}{\frac{10}{3}} = 12.5 \qquad \frac{\frac{25}{2}}{\frac{10}{3}}\cdot\frac{4}{3} = 5 \qquad \frac{\frac{5}{1}}{\frac{10}{3}}\cdot\frac{5}{3} = \frac{5}{2}$$

(d) [5pts] **For 251A students only:** Using the sizes from your previous answer, a wire capacitance of $C_{wire} = \frac{5}{2}C_{in}$ is inserted between each gate. Assuming $\gamma = 1$, calculate the delay through the critical path normalized to the intrinsic inverter delay t_{p0}?

$$D = 3 \cdot 2 + 1 + 4 \cdot \frac{10}{3} + \frac{4}{3} \cdot \frac{\frac{5}{2}}{1} + \frac{5}{3} \cdot \frac{\frac{5}{2}}{\frac{5}{2}} + \frac{4}{3} \cdot \frac{\frac{5}{2}}{5} =$$

$$= 7 + \frac{40}{3} + \frac{5}{3} + \frac{4}{2} \cdot 3 = 11 + \frac{45}{3} = 26$$