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DEPARTMENT OF BIOENGINEERING   BERKELEY, CALIFORNIA
94720-1762

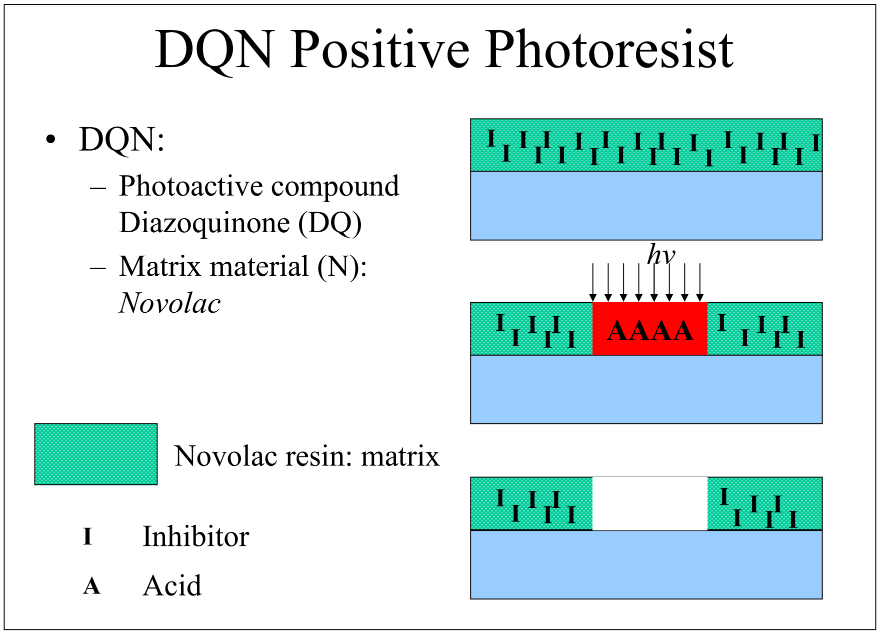
BioE 121

Midterm #1 Solutions

Problem #1. (20 points) Photolithography

a. (5 points) Describe basic photochemical mechanism of a positive resist (DQN)
b. (10 points) Describe the photochemical mechanism of reverse image process of a positive resist.
c. (5 points) Compare optical and e-beam lithography methods (resolutions limit, process time, cost, etc)

a)



DQN Positive Photoresist

- DQN:
  - Photoactive compound Diazoquinone (DQ)
  - Matrix material (N): *Novolac*

🟩 Novolac resin: matrix

I Inhibitor

A Acid

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b)

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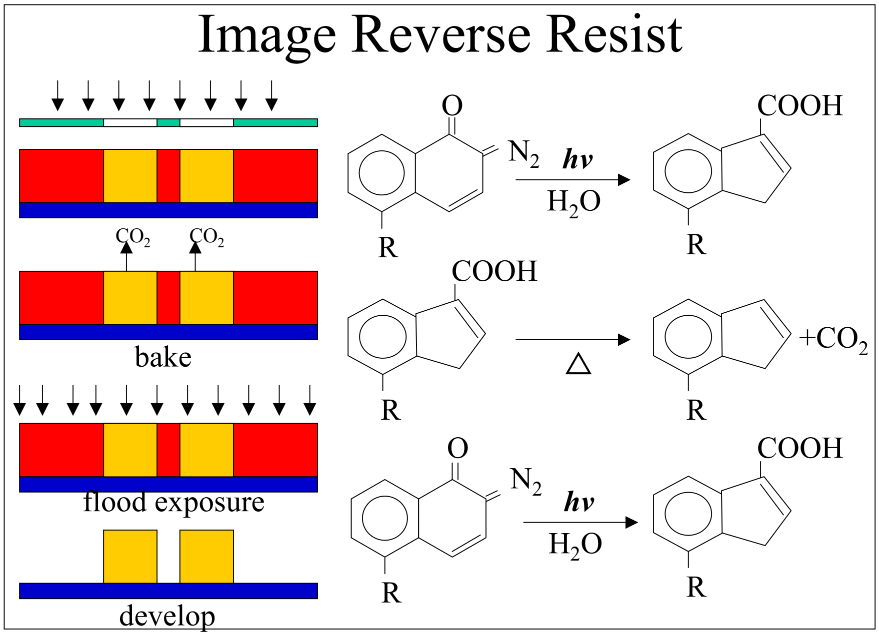

Image Reverse Resist

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e-beam Lithography:

Advantage:
Very small beam spot (< 1nm), can define very small features

Disadvantages:
Low throughput – a serial writing process versusthe parrallel writing process of optical lithography.
Proximity effect- Backscattered electrons from substrate material may affect critical feature size.

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Problem #2. (20 points) Sacrificial Layer Process

a. (10 points). Figure 1 show an encapsulated cantilever in the air. Show the process steps to accomplish this device by cross sectional fabrication steps

b. (10 points). Describe deposition and etching methods for each step

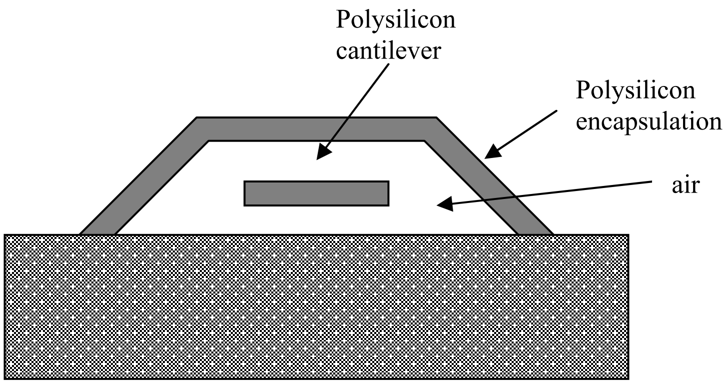

Figure 1

i) - CVD Deposition of Phosphosilicate glass (PSG)
- CVD Deposition and Patterning of Polysilicon

ii) CVD Deposition of Phosphosilicate glass (PSG)

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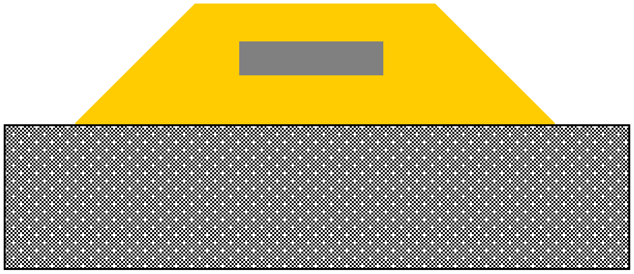
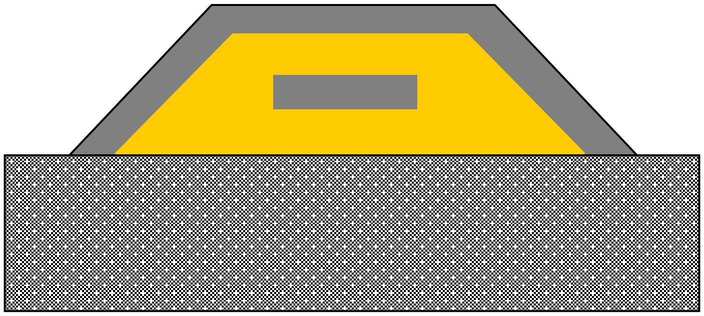
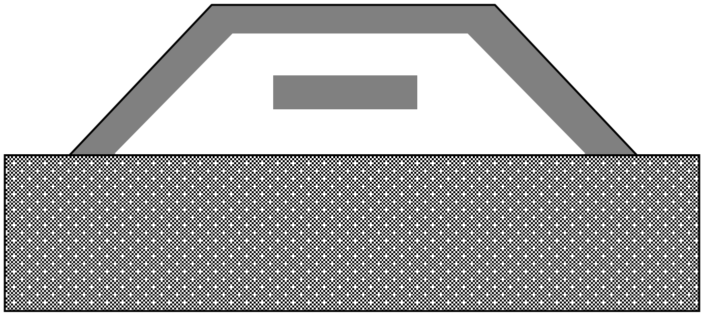
iii) Ion beam etching (Ion Milling) of PSG



iv) CVD Deposition of Polysilicon



v) Release the structure by HF etch



Note: This proposed fabrication process is the easiest method to get the desired topology, although, ion beam etching is not a common used method in micro fabrication technology. One other method, is using two different wafers and bond them together to get the desired topology, however this method cost much more than the proposed process flow.

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Problem #3. (20 points) Fabrication Process
In your old laboratory, you have only simple plasma-etching system and chemicals (KOH, Water, Isopropyl alcohol, HNO_3, HF, and $HC_2H_3O_2$). Select which you would use in the following applications. Be sure to justify your answer with an estimated etching rate. If you need to use the plasma-etching system, make sure to indicate what kind of gas you need to etch properly.

a. (3 points) Thin film etching of Si_3N_4
b. (3 points) Sacrificial oxide (PSG) layer etching under 700 nm polysilicon layer
c. (3 points) Anisotropic patterning of SiO_2.
d. (3 points) Selective etching of doped Si membrane
e. (3 points) Explain the mechanism of deep RIE
f. (5points) You need to find a process step that requires to pattern 10 microns width of a metal thin film on 10 nm thicknesses of SiO_2. Your chip design requires to maintain 10 nm of SiO_2 without any damage. However, your dry etching system for the metal is also etching SiO_2. Unfortunately, dry etching system that you have for metal does not have a selective etching rate for metal over SiO_2, it is hard to stop on 10 nm thickness of SiO_2. What is a simple and effective method of micropatterning the metal layer on SiO_2 without damaging SiO_2 layer? Explain your process steps in details.

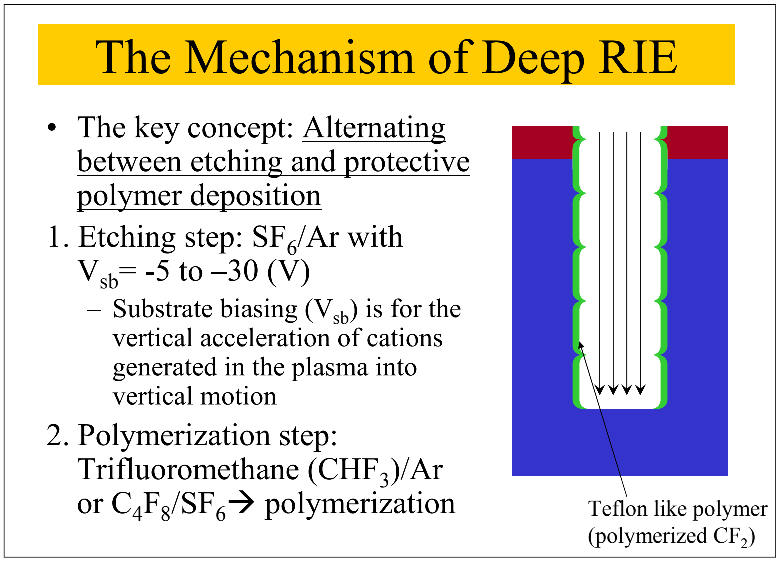
a) Non of the given chemicals will etch Si_3N_4 . Use plasma etching (SF_6 + He) which has etch rate of ~ 0.6 µm/min

b) Use HF : etch rate ~ 0.165 µm/min

c) Plasma Etch with $CF_4 + O_2$: etch rate ~ 0.06 µm/min

d) Use KOH to selectively etch undoped Si : etch rate ~ 1.4 µm/min

e) DRIE (Deep Reactive Ion Etching) alternates between isotropic Reactive Ion Etching (RIE) and polymer deposition. An inducing coupled plasma is source of deposition. The polymer protects the side wall as the bottom of the cavity is etched further. With this method high aspect ration is attained.



The Mechanism of Deep RIE

- The key concept: <u>Alternating between etching and protective polymer deposition</u>

1. Etching step: SF_6/Ar with V_{sb}= -5 to –30 (V)
   – Substrate biasing (V_{sb}) is for the vertical acceleration of cations generated in the plasma into vertical motion
2. Polymerization step: Trifluoromethane (CHF_3)/Ar or $C_4F_8/SF_6 \rightarrow$ polymerization

Teflon like polymer (polymerized CF_2)

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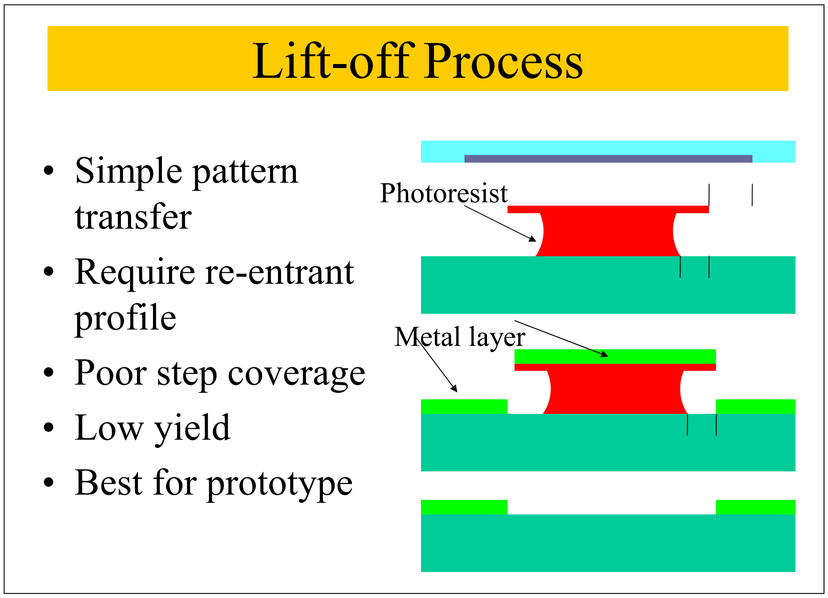
f)



Lift-off Process

- Simple pattern transfer
- Require re-entrant profile
- Poor step coverage
- Low yield
- Best for prototype

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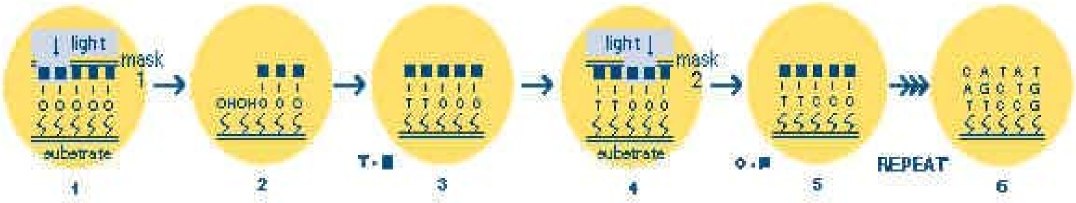
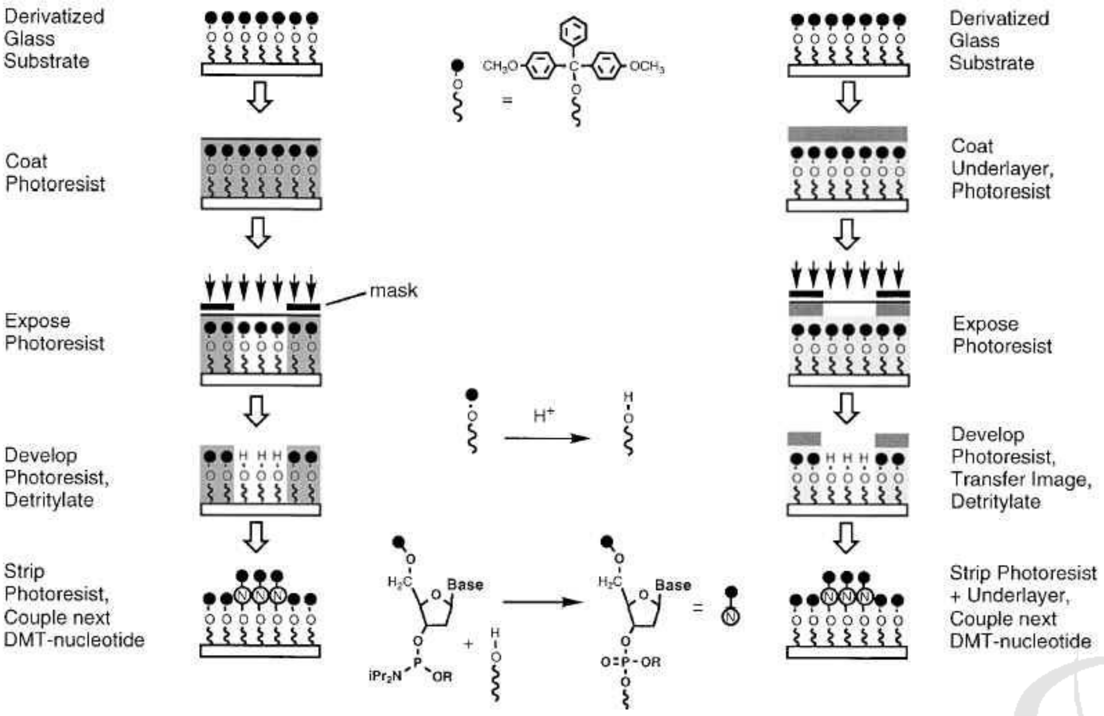
Problem #4. (20 points) Oligonucleotide Arrays

a. (5 points) Describe the fabrication steps of ologinucleotide arrays of following base pairs: TACG, CATA, ATTA, GAGG, and TATA on a substrate.
b. (5 points) Describe the detection methods of current ologinucleotide probes and discuss the limitation.
c. (5 points) Compare direct and indirect methods of detecting DNA sequencing.
d. (5 points) Describe a method of measuring a bonding force between base pairs of DNA using AFM tip.

a)





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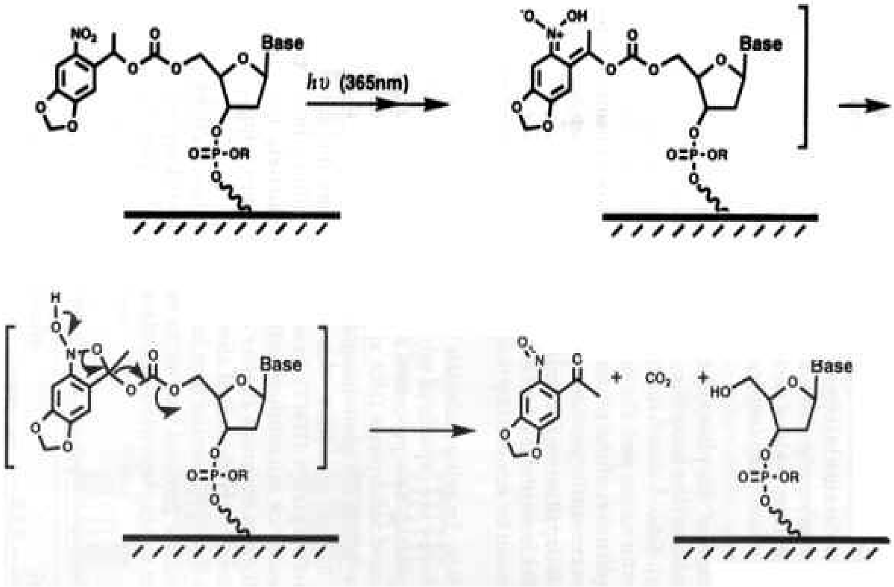
b) Fluorescently-tagged probes, when hybridized with the correct complementary sample DNA bases, will emit light when it is excited with laser (usually of shorter wavelength). Many limitations: expensive, elaborate optical equipment, only work with short oligonucleotide probes (20-25 base pairs).

c) Direct method: nanoprobe – directly sensing individual bases on a string, researchers are working in this area using nanopores.

Indirect methods: Oligonucleotide probe arrays, northern blot, southern blot, PCR-dot blot: slow, expensive, but well-established and reliable methods

d) Photolysis:



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Problem #5. (20 points) Surface & Bulk Micromachining Process: Self Focusing Acoustic Transducer (SFAT) for DNA or Protein Array

a. (10 points). Figure 2 show the SFAT. The SFAT can be used as a liquid ejector and it is fabricated by silicon micromachining. Show the process steps to accomplish this device by cross sectional fabrication steps

b. (10 points). Describe deposition and etching methods for each step

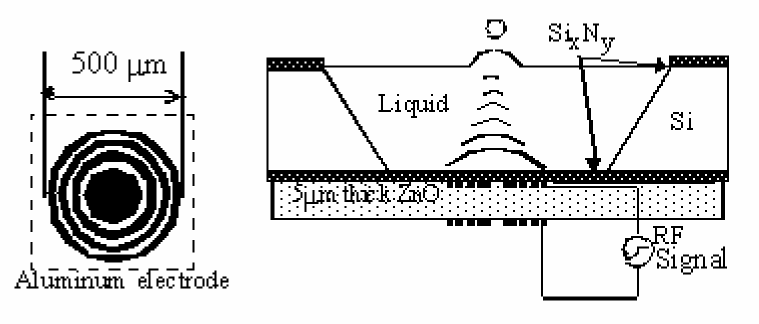

Figure 2. Cross-sectional view of the liquid ejector microfabricated on a silicon wafer.

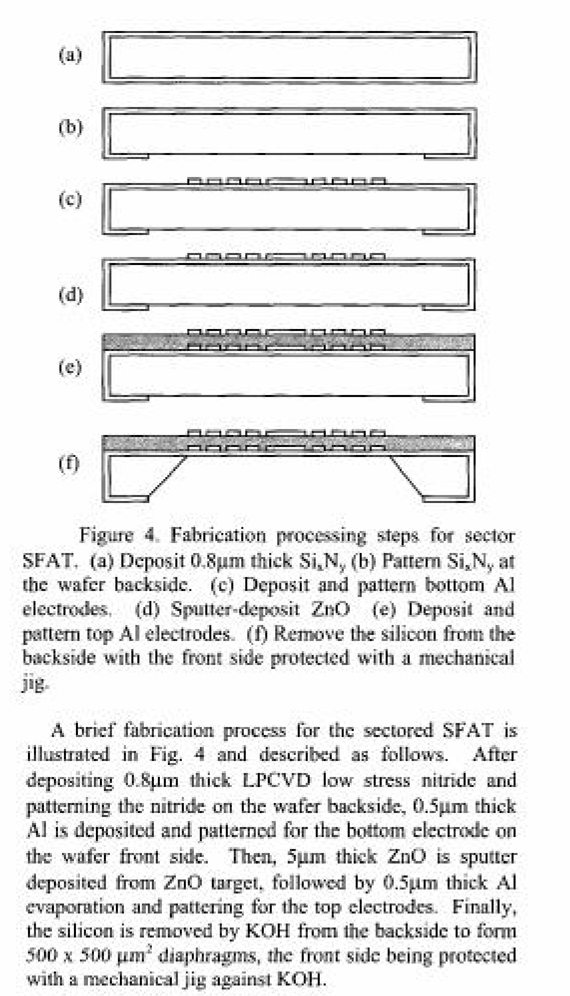

Figure 4. Fabrication processing steps for sector SFAT. (a) Deposit 0.8µm thick Si_xN_y (b) Pattern Si_xN_y at the wafer backside. (c) Deposit and pattern bottom Al electrodes. (d) Sputter-deposit ZnO (e) Deposit and pattern top Al electrodes. (f) Remove the silicon from the backside with the front side protected with a mechanical jig.

A brief fabrication process for the sectored SFAT is illustrated in Fig. 4 and described as follows. After depositing 0.8µm thick LPCVD low stress nitride and patterning the nitride on the wafer backside, 0.5µm thick Al is deposited and patterned for the bottom electrode on the wafer front side. Then, 5µm thick ZnO is sputter deposited from ZnO target, followed by 0.5µm thick Al evaporation and pattering for the top electrodes. Finally, the silicon is removed by KOH from the backside to form *500 x 500 µm²* diaphragms, the front side being protected with a mechanical jig against KOH.

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