EE143 Microfabrication Technology
Spring 2012
Prof. J. Bokor

Midterm Exam 2

Name: Solutions

Signature: ____________________

SID: ____________________

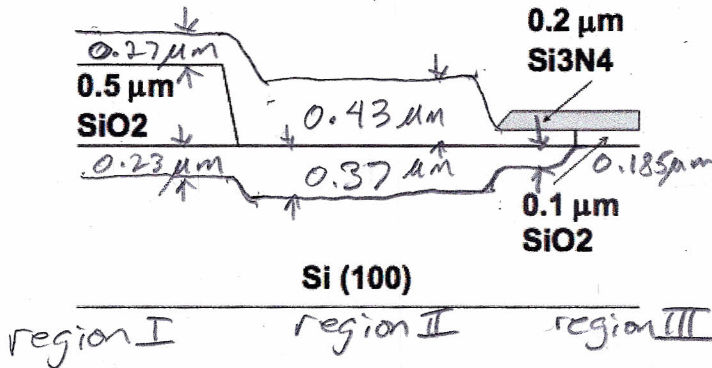
CLOSED BOOK. ONE 8 1/2" X 11" SHEET OF NOTES, AND SCIENTIFIC POCKET CALCULATOR PERMITTED. MAKE SURE THE EXAM PAPER HAS 10 PAGES. DO ALL WORK ON THE EXAM PAGES. USE THE BACK OF PAGES IF NECESSARY.

TIME ALLOTTED: 80 MINUTES

Fundamental constants you might need:

Boltzmann's constant, $k = 1.38 \times 10^{-23}$ J/K
Permittivity of free space, $\varepsilon_o = 8.85 \times 10^{-12}$ F/m
Permeability of free space, $\mu_o = 1.26 \times 10^{-6}$ H/m
Speed of light in vacuum, $c = 2.998 \times 10^{8}$ m/s
Electron charge, $e = 1.6 \times 10^{-19}$ C
Free electron mass, $m_o = 9.1 \times 10^{-31}$ kg
Electron volt, 1 eV = 1.6×10^{-19} J
Thermal voltage, $kT/q = 0.0258$ V (at 300K)
Relative dielectric constant of silicon, $K_s = 11.8$
Relative dielectric constant of silicon dioxide, $K_o = 3.9$
Effective masses in silicon at 300K. Electrons: $m_n^* = 1.18\ m_o$; Holes: $m_p^* = 0.81\ m_o$
Silicon band gap at 300K, $E_g = 1.12$ eV
Silicon intrinsic carrier concentration at 300K, $n_i = 10^{10}$ cm^{-3}
Avogadro's number, $N_A = 6.02 \times 10^{23}$

1. **Thermal oxidation (25 points)**
   a. The following structure is subjected to a steam oxidation step at 1000°C for 3 hours. Sketch a roughly proportional cross-section after this oxidation step in the same figure. Label all regions and important thicknesses. Use the attached oxidation chart to generate numerical values of the different oxide thickness. (15 points)



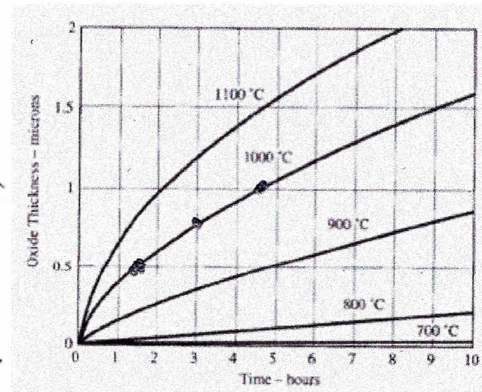


Figure 6-20 Calculated oxidation rates for (100) silicon in H_2O based on the Deal-Grove model. Parameter values taken from Table 6-2.

Region I

0.5 μm initial oxide thickness corresponds to 1.5 hrs at 1000C. Total oxidation time is then 4.5 hrs which gives 1 μm total thickness. Additional oxide thickness is 0.5 μm. Si consumption is $0.46 \times 0.5\,\mu m = 0.23\,\mu m$

Region II

3 hrs at 1000C gives 0.8 μm. Si consumed is $0.46 \times 0.8\,\mu m = 0.37\,\mu m$

Region III

Region under the Si_3N_4 in the gap. Oxidation proceeds until oxide reaches the Si_3N_4, then stops. So total oxide thickness is X, where

$$(1-0.46)X = 0.1\,\mu m \Rightarrow X = \frac{0.1}{0.54}\,\mu m = 0.185\,\mu m$$

b. In general (not referring to the part a) will the following increase (⇧), decrease (⇩), or not affect (-) the silicon thermal oxidation rate? [4 pts]

	result
decreasing the furnace temperature	↓
using silicon on insulator (SOI) substrate with a thin (20 nm) top Si layer (crystalline)	–
using wet oxidation instead of dry oxidation	↑
adding 2% by volume HCl to the dry gaseous input	↑
Switching from a (100) to a (111) oriented silicon wafer	↑
using a poly-Si substrate	↑
doping the substrate heavily with phosphorous	↑
relocating your non-pressurized furnace to the top of Mt. McKinley	↓

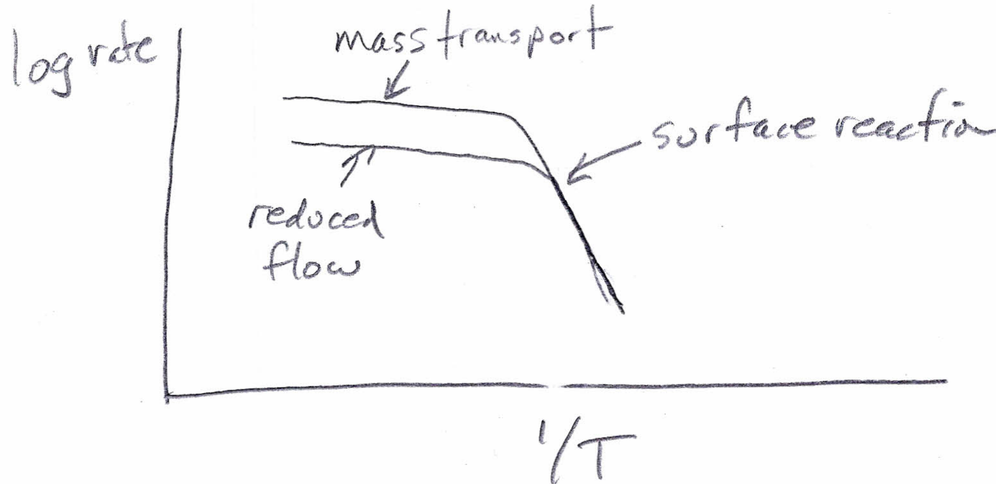
c. List the three main kinetic steps of the oxidation process. [3 pts]

1. Gas diffusion through gas stagnant layer
2. Solid state diffusion
3. SiO_2 formation

d. For short oxidation times on a bare wafer, which of the above step(s) do you think will be the rate limiting step(s)? Briefly explain. [3 pts]

SiO_2 formation. For short times oxide is thin so solid state diffusion not important. For short times, gas diffusion is also not important.

2. **Deposition (25 points)**
   a. Qualitatively plot the deposition rate as a function of 1/temperature for CVD. Label each regime on the curve in terms of the rate limiting step that applies in that regime. (10 points)



   b. Suppose we maintain all CVD conditions the same except the gas flow velocity is reduced. Sketch a new deposition rate curve versus 1/T in the above figure. [No credit will be given without a brief explanation] (7 points)

      mass transport reduced. surface reaction rate same.

   c. A postdeposition anneal called a densification step is often used to reduce the etch rate of CVD SiO_2. This step is typically run at 900-1000 C. The step is not normally done for PECVD films, although they would benefit from the anneal. Explain briefly why the process is not done for these films. (3 points)

      PECVD is used for low temperature steps on substrates that cannot tolerate high temperatures

   d. List two major advantages of using chemical vapor deposition versus physical vapor deposition for thin films. (2 points)

      - Better step coverage (more conformal)
      - Better uniformity

e. List three major advantages of using sputter deposition versus evaporation deposition for thin films. (3 points)

- better composition control for alloy films
- better uniformity
- better step coverage
- ability to sputter etch clean substrate befor deposition

3. **Doping (25 points)**

An ion implantation step (dose=10^{14} cm-2, R_p=0.0226μm, ΔR_p=0.0102μm) implants Arsenic (As) into a p-type semiconductor material with uniformly doped boron (B) background concentration of 10^{16} cm^{-3}. The total thickness of this Si wafer is 300 μm.

a. Find the peak As concentration, N_p (5 pts)

$$N_p = \frac{Q}{\Delta R_p \sqrt{2\pi}} = \frac{10^{14}}{0.0102 \times 10^{-4} \times \sqrt{2\pi}}$$

$$= \underline{3.9 \times 10^{19}} \ cm^{-3}$$

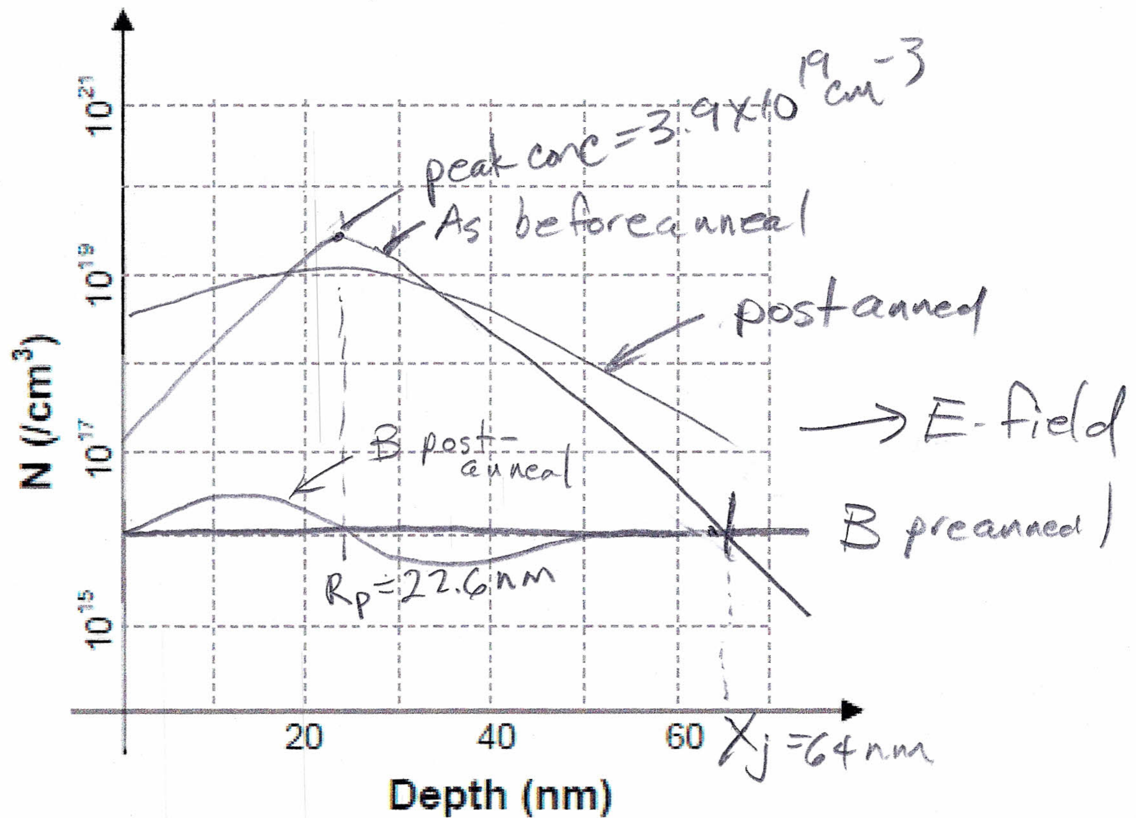
b. Find the junction depth(s) right after the implantation (5 pts)

$$X_j = R_p + \Delta R_p \sqrt{2 \ln(N_p/N_B)}$$

$$= \underline{64 \ nm}$$

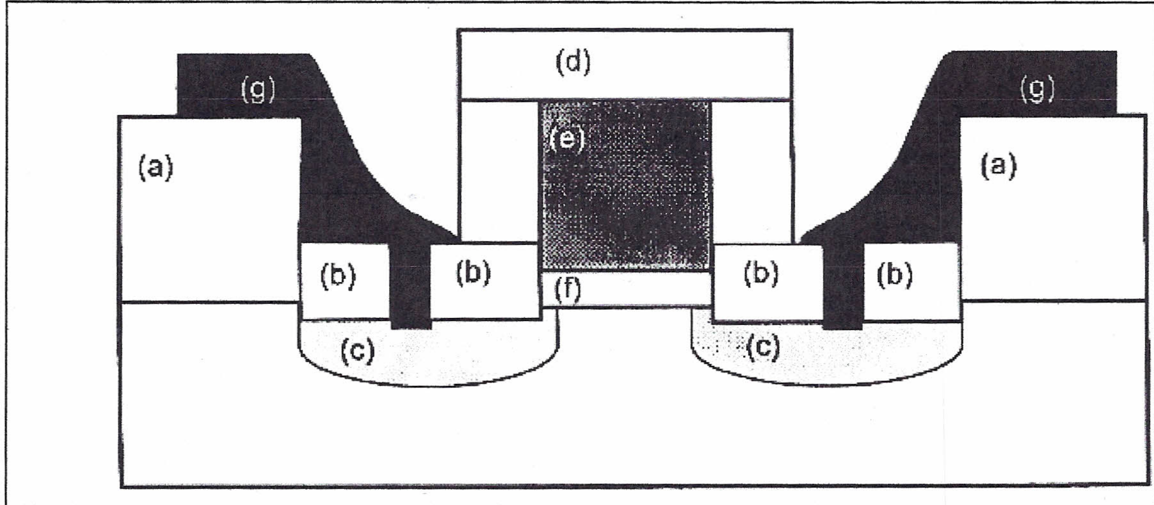
c. Draw the As and B concentration profiles. Clearly indicate and label the projected range, peak concentration, and the junction location. Assume an ideal Gaussian profile. (8 pts)

d. Sketch the As and B profiles of the sample after thermal annealing, ignoring TED but including the electric field enhanced diffusion. Label the direction of the e-field as well. (7pts)



4. EE 143 Lab (7 points)

Label the lettered parts of the EE143 lab MOSFET cross section schematic below (not scaled). Select from the list of possible options given. A given option could be used more than once.



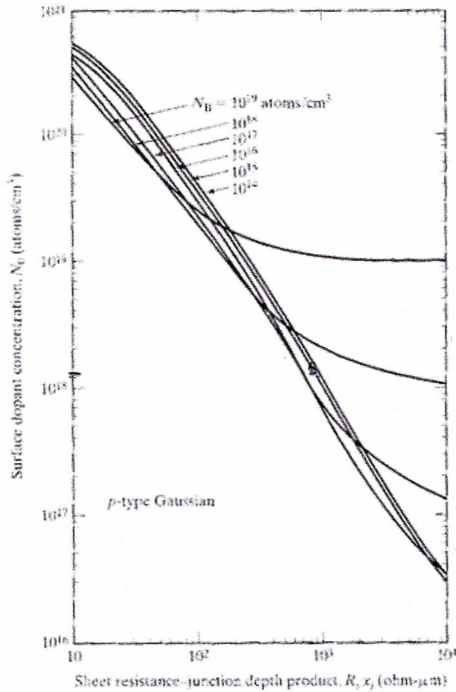
(a) FOX
(b) IOX
(c) n+ Si
(d) IOX
(e) n+ polySi
(f) GOX
(g) Al

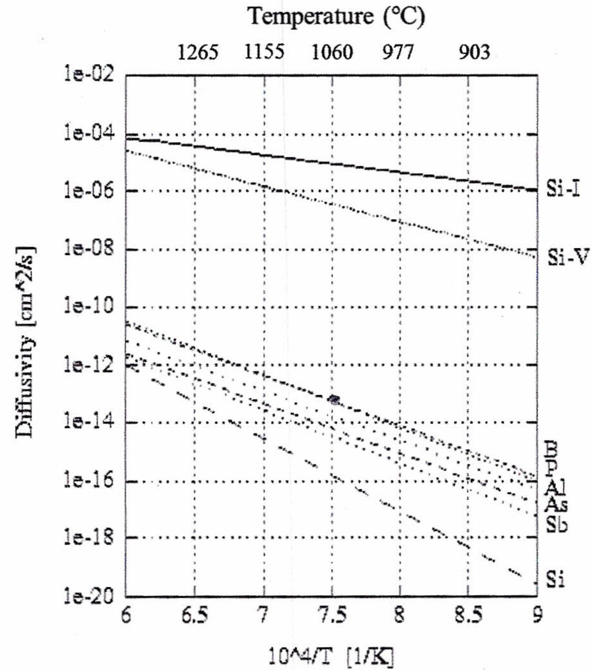
<u>Options</u>

n+ Si
p+ Si
intrinsic Si
n+ polySi
p+ polySi
intrinsic polySi
field oxide (FOX)
gate oxide (GOX)
intermediate oxide (IOX)
silicon nitride
silicon oxy-nitride
photoresist (PR)
Au
Spin-on-glass (SOG)
Aluminum (Al)
Phosphosilicate glass (PSG)

5. **Contacts and Sheet Resistance (18 points)**

a. We start with a substrate with a phosphorous background concentration of 1 x $10^{16}/cm^3$. After a solid-source boron pre-deposition for 30 minutes at 900°C, and 2.25 hour drive-in anneal at 1060°C, the wafer has a surface concentration of 1.1 x $10^{18}/cm^3$. Using the plots below, calculate the approximate sheet resistance of the wafer. (9 points)





$$C_B = C_s \exp[-x_j^2/(4Dt)]$$

At 1060 C for B, $D \cong 10^{-13}\ cm^2/s$

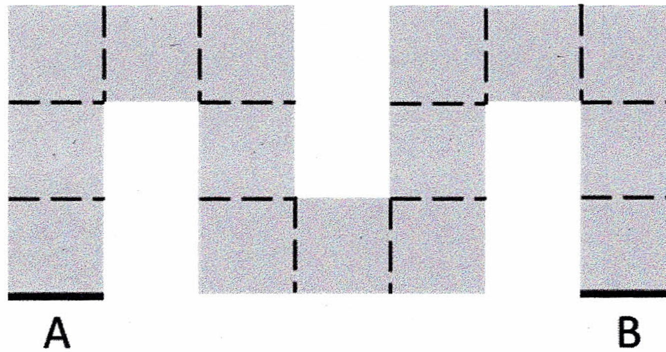
Solve for $x_j = \sqrt{4Dt \ln(C_s/C_B)} = 1.23\ \mu m$

Use Irvin curve, $C_s = 1.1 \times 10^{18}$, $C_B = 1 \times 10^{16}$,

read off $R_s x_j \cong 800\ \Omega\text{-}\mu m$

So $R_s = 800/1.23 = \underline{648\ \Omega/\square}$

b. The figure below is of a 200nm-thick gold interconnect. If the resistivity of gold is 2.44×10^{-8} Ω*m, what is the resistance between points A and B? (9 points)



Sheet resistance $R_s = \rho / t = 0.122\ \Omega/\square$

9 regular squares

6 corner squares = $6 \times 0.56 = 3.36$ equivalent

12.36 equivalent squares $\times$ 0.122

$= 1.5\ \Omega$