University of California at Berkeley
College of Engineering
Dept. of Electrical Engineering and Computer Sciences

EE 105 Midterm I

Fall 2005 Prof. Borivoje Nikolić October 13, 2005

Your Name: _____

Student ID Number: _____

Guidelines

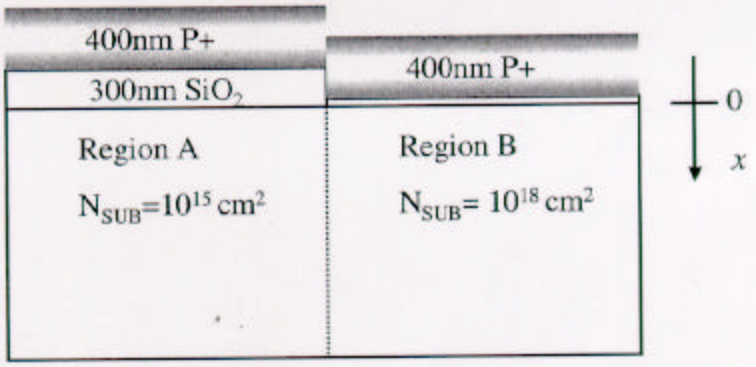
Closed book and notes; there are some useful formulas in the end of the exam.
You may use a calculator.
You can unstaple the pages with formulas, but do not unstaple the exam.
Show all your work and reasoning on the exam in order to receive full or partial credit.
Time: 80 minutes = 1 hour, 20 minutes.

Score

Problem	***Points*** Possible	Score
1	~~14~~ 20	
2	20	
3	16	
Total	~~56~~ 60	

1. Integrated charge-storage element [14 points] 20

The following figure shows the cross-section of a PMOS capacitor structure. P+ poly-silicon gate covers two regions: region A with gate oxide thickness of 300nm and region B with gate oxide thickness of 3nm respectively. The effective areas of the capacitor over the thick and thin oxide are 10,000μm^2 and 100μm^2 respectively. Please use the following parameters: $\phi_{p+} = -550$mV, $\varepsilon_{Si} = 11.7$, $\varepsilon_{SiO2} = 3.9$, $\varepsilon_0 = 8.854\times10^{-14}$F cm^{-1}, $n_i = 10^{10}$cm^{-3}.



(a) [4 points] What are the flat-band voltages (V_{FB}'s) of regions A and B?

$V_{FBA} = -(\phi_{p+} - \phi_n) = -(-550 - 25\ln(\frac{10^{15}}{10^{10}}))mV = 838mV$

$V_{FBB} = -(-550 - 25\ln(\frac{10^{18}}{10^{10}}))mV = 1010mV$

$W_{FBA} = 0.838\,V$

$W_{FBB} = 1.01\,V$

(b) [4 points] What are the threshold voltages (V_T's) of regions A and B?

$$V_T = V_{FB} - 2\phi_n - \frac{1}{C_{ox}}\sqrt{2q\varepsilon_s N_a (2\phi_n)}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}, \quad \varepsilon_{ox} = \varepsilon_{SiO_2}\cdot\varepsilon_0, \quad \varepsilon_s = \varepsilon_{Si}\cdot\varepsilon_0$$

$$\phi_n = 0.025\ln\left(\frac{N_a}{n_i}\right)$$

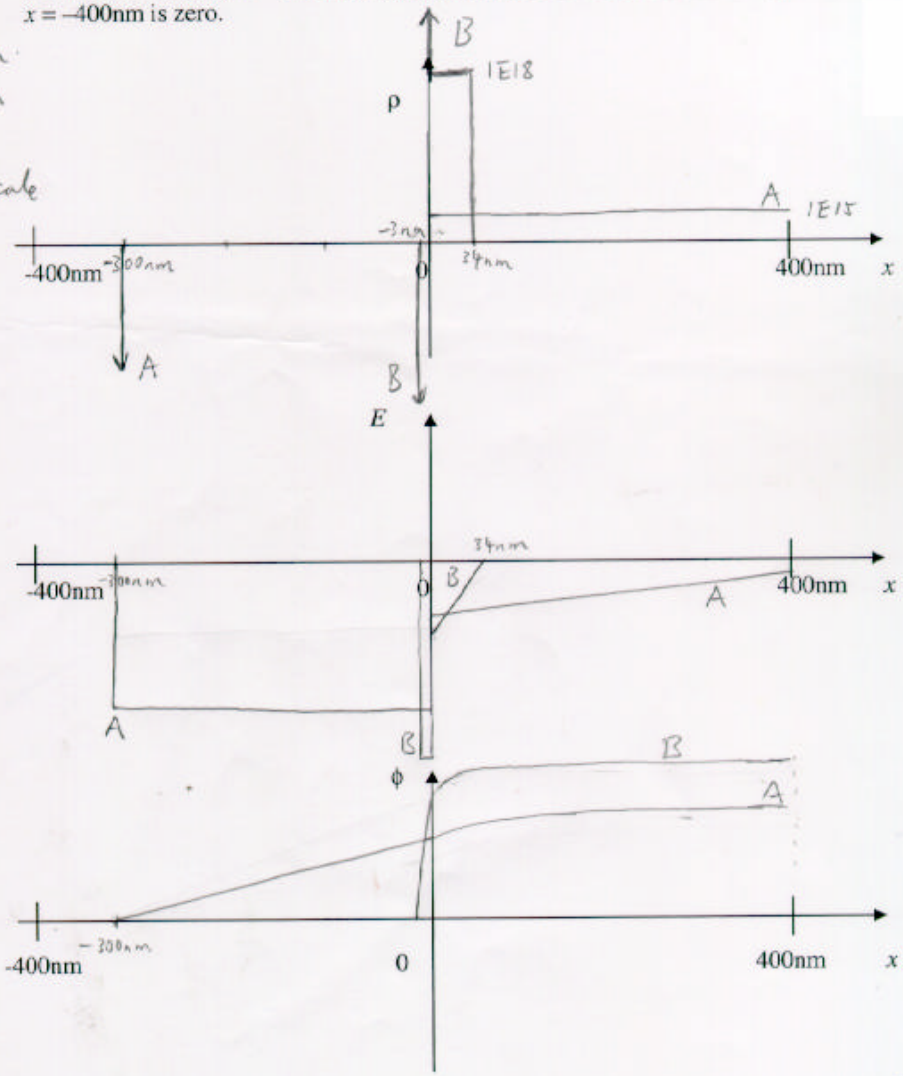
$V_{TA} = -0.938\ V$

$V_{TB} = -0.391\ V$

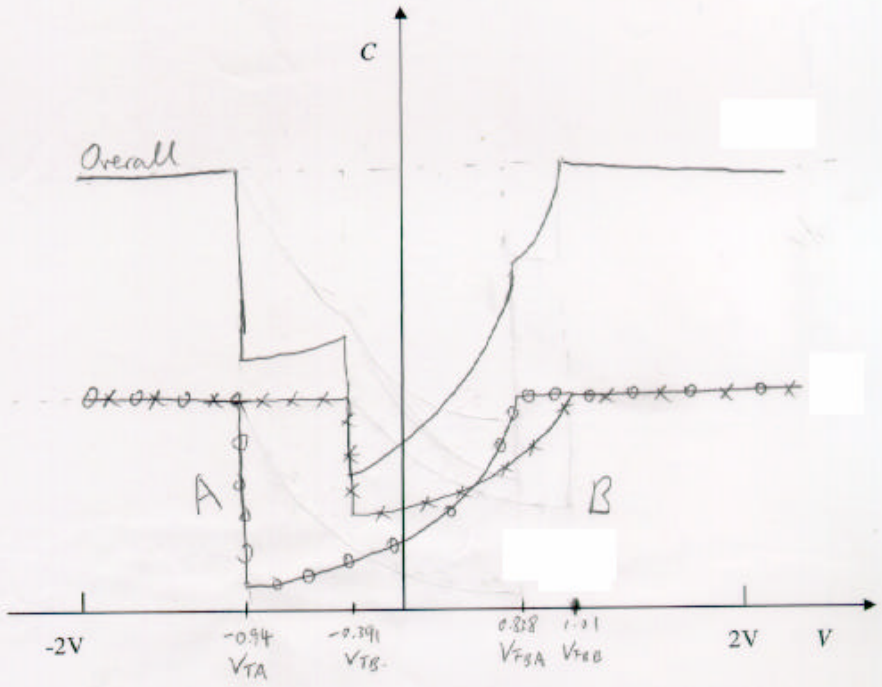
(c) [6 points] Sketch the charge, E-field and potential distribution from $x = -400$nm to $x = 400$nm when V_G = -0.5V for regions A and B. Assume that the potential at $x = -400$nm is zero.

A – depletion
B – inversion

A, B not in scale



(d) [6 points] Sketch the CV of the whole capacitor structure. Please label the relevant points on the *C*- and *V*-axii.



2. Semiconductors, pn Junctions and MOS devices [20 pts]

A few useful constants: The permittivity of silicon is $\varepsilon_s = 1.035 \times 10^{-12}$ F/cm and the permittivity of SiO_2 is $\varepsilon_{ox} = 3.45 \times 10^{-13}$ F/cm. You can assume mobilities of $\mu_n = 1500$ $cm^2/(Vs)$ and $\mu_p = 500$ $cm^2/(Vs)$. The saturation electric field for electrons is $E_{sat} = 1.25 \times 10^4$ V/cm and their saturation velocity is $v_{sat} = 10^7$ cm/s. Unit charge: $q = 1.6 \times 10^{-19}$ C, $n_i = 10^{10} cm^{-3}$.

(a) [4 points] In a silicon resistor made from N-doped silicon doped to 10^{18} per cubic cm, with a length of 10μm, a width of 1μm, and a thickness of 0.1μm, what is the maximum current which can flow?

$$I = AJ = A q n v_{sat}$$
$$= (0.1 \times 1) \times 10^{-8} \times 1.6 \times 10^{-19} \times 10^{18} \times 10^7$$
$$= 0.0016 A = 1.6 mA$$

$I_{max} =$ 1.6 mA

(b) [4 points] For a silicon PN junction at room temperature which has one side P doped to a concentration of 10^{18} per cm^3 and the other side N doped to a concentration of 10^{16} per cm3, find the depletion depth into both the P side and into the N side.

$$X_{do} = X_{dn} + X_{dp}$$
$$\because N_A X_{dp} = N_D X_{dn}$$
$$\therefore X_{do} = X_{dn} + \frac{N_D}{N_A} X_{dn} = X_{dn}\left(1 + \frac{N_D}{N_A}\right)$$
$$\text{Use } X_{do} = \sqrt{\frac{2\varepsilon_s \phi_{bi}}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)} = 325 nm$$

$X_{p0} =$ 3.2nm

$X_{n0} =$ 321.8nm

(c) [4 points] What is the qualitative relationship between the width of the depletion region and the conductivity for the N side of the junction in part (b) . Briefly explain.

$$X_{dn} \propto \frac{1}{\sqrt{N_A}}, \quad \sigma = q n \mu = q N_A \mu \propto N_A$$
$$\therefore X_{dn} \propto \frac{1}{\sqrt{\sigma}}$$

With an increase in conductivity, depletion width increases / decreases. (circle one)

(d) [4 points] Consider two MOSFETs with identical dimensions, but with differently doped substrates; MOSFET A has the substrate doped with $N_A = 10^{15}$ cm^{-3}, and MOSFET B has doping of $N_A = 10^{16}$ cm^{-3}. Assume equivalent bias for both transistors, where both transistors are in saturation. In which case will the same change in V_{DS} voltage (ΔV_{DS}) cause a larger *relative* change in the capacitance between the drain and the substrate $\Delta C_j/C_j$. Explain your answer.

$$C_j = \frac{C_{j0}}{\sqrt{1-\frac{V_D}{\phi_{bi}}}} \quad \therefore \quad \frac{dC_j}{dV_D} = \left[\frac{C_{j0}}{\sqrt{1-\frac{V_D}{\phi_{bi}}}}\right]' = C_{j0}\left(-\frac{1}{2}\right)\left(1-\frac{V_D}{\phi_{bi}}\right)^{-\frac{3}{2}}$$

$$\Rightarrow \quad \frac{dC_j}{C_{j0}} = \underbrace{\frac{1}{2}\frac{1}{\phi_{bi}}}_{A}\underbrace{\left(1-\frac{V_D}{\phi_{bi}}\right)^{-\frac{3}{2}}}_{B} dV_D$$

$\because N_A \uparrow \Rightarrow \phi_{bi} \uparrow \Rightarrow A \downarrow, \; B \downarrow$

$\therefore N_A \uparrow, \; \frac{dC_j}{C_{j0}} \downarrow$

(MOSFET A) / MOSFET B (circle one)

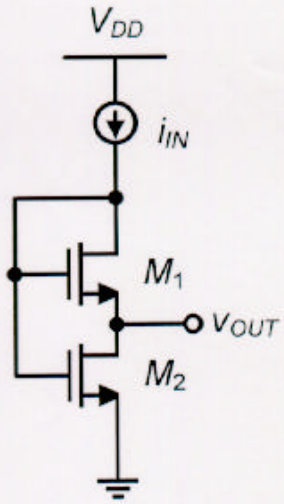
(e) [4 points] Which one of the two MOSFETs from (d) would have a larger relative change in effective channel length, $\Delta L/L$, under the same change in V_{DS} voltage (ΔV_{DS}). Explain your answer.

$\because C = \frac{\varepsilon}{x}$

from d), $N_A \uparrow \Rightarrow \frac{\Delta C}{C} \downarrow \Rightarrow \frac{\Delta x}{x} \downarrow \Rightarrow \frac{\Delta L}{L} \downarrow$

(MOSFET A) / MOSFET B (circle one)

3. MOSFET circuit [16 points]



Given:
$L_1 = L_2 = 0.5\ \mu m$
$W_1 = W_2 = 5\ \mu m$
$\mu_n C_{ox} = 100\ \mu A/V^2$
$V_{Tn} = 0.5\ V$
$\lambda_n = 0\ V^{-1}$
$\gamma = 0$

(a) [4 points] In which modes of operation are operating M1 and M2 for $i_{IN} > 0$? Explain your answer.

M1 – saturation $(V_{GD1} = 0 < V_{Tn})$

M2 – linear $(V_{GD2} = V_{GS1} > V_{Tn})$

(b) [8 points.] Find the relationship $v_{OUT} = v_{OUT}(i_{IN})$. You do not need to substitute the numerical values.

M1: $i_{IN} = \left(\frac{W}{L}\right)\frac{\mu C_{ox}}{2}\left(V_{GS1} - V_{Tn}\right)^2$

$= \frac{K}{2}\left(V_{IN} - V_{out} - V_{Tn}\right)^2$ — (1) $K = \mu C_{ox}\frac{W}{L}$

M2: $i_{IN} = \left(\frac{W}{L}\right)\mu C_{ox}\left(\left(V_{GS2} - V_{Tn}\right)V_{DS2} - \frac{V_{DS2}^2}{2}\right)$

$= K\left(\left(V_{in} - V_{Tn}\right)V_{out} - \frac{V_{out}^2}{2}\right)$ — (2)

From (1), $V_{IN} = \sqrt{\frac{2i_{IN}}{K}} + V_{out} + V_{Tn}$ — (3)

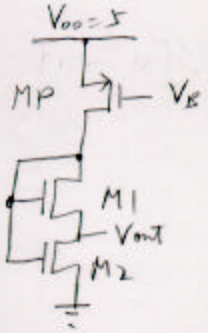
From (2), $V_{IN} = \left[\frac{i_{IN}}{K} + \frac{V_{out}^2}{2}\right]/V_{out} + V_{Tn}$ — (4)

(3), (4) $\Rightarrow$ $\sqrt{\frac{2i_{IN}}{K}} + V_{out} = \frac{i_{IN}}{KV_{out}} + \frac{V_{out}}{2}$

$\therefore V_{out}^2 + 2\sqrt{\frac{2i_{IN}}{K}}V_{out} - \frac{2i_{IN}}{K} = 0$

$\therefore V_{out} = (2-\sqrt{2})\sqrt{\frac{i_{IN}}{K}}$ //

(c) [4 points] If the current source i_{IN} is implemented as simple DC-biased PMOS transistor (W/L = 10, $\mu_p C_{ox}$ = 100 μA/V^2, V_{Tp} = - 0.5 V, λ_p = 0 V^{-1} γ = 0), find the maximum and minimum values of v_{OUT}, under which the circuit operates correctly, with the supply voltage of V_{DD} = 5V.



From b)

$i_{IN} \to 0$, $V_{out} \to 0$ (M1, M2 barely ON)

$V_{out,min} = 0\,V$ //

When $V_B \downarrow \Rightarrow i_{IN} \uparrow \Rightarrow V_{O1} \uparrow$,

MP is still in saturation as long as

$V_B \geq -|V_{Tp}| + V_{O1}$

When V_{out} is max, $V_B = V_{O1} - |V_{Tp}| = V_{IN} - |V_{Tp}|$

MP: $i_{IN} = \frac{K}{2}(V_{DD} - V_B - |V_{Tp}|)^2 = \frac{K}{2}(V_{OD} - V_{IN})^2$

$V_{out} = (2-\sqrt{2})\sqrt{\frac{i_{IN}}{K}}$

$= (\sqrt{2}-1)(V_{DD} - V_{IN}) = (\sqrt{2}-1)V_{OV}$

On the other hand, $V_{out} = V_{DD} - 2V_{OV} - V_{Tn}$

$\therefore V_{OV} = \frac{V_{out} - V_{DD} + V_{Tn}}{-2}$

$\therefore V_{out} = \frac{(1-\sqrt{2})}{2}[V_{out} - V_{DD} + V_{Tn}]$

$\therefore V_{out} = \frac{(\sqrt{2}-1)(V_{DD} - V_{Tn})}{(\sqrt{2}+1)}$

$= \left(\frac{\sqrt{2}-1}{\sqrt{2}+1}\right) 4.5$

$= 0.772\,V$ //

$V_{OUTmax} = 0.772\,V$

$V_{OUTmin} = 0\,V$