EE143 Microfabrication Technology
Spring 2011
Prof. J. Bokor

Final Exam

Name: Solutions

Signature: _____

SID: _____

CLOSED BOOK. THREE 8 1/2" X 11" SHEET OF NOTES, AND SCIENTIFIC POCKET CALCULATOR PERMITTED. MAKE SURE THE EXAM PAPER HAS 15 PAGES. DO ALL WORK ON THE EXAM PAGES. USE THE BACK OF PAGES IF NECESSARY.

TIME ALLOTTED: 180 MINUTES

Question	Score
1 (30 pts)	
2 (35 pts)	
3 (45 pts)	
4 (30 pts)	
5 (60 pts)	
Total (200 pts)	

Fundamental constants you might need:

Boltzmann's constant, $k = 1.38 \times 10^{-23}$ J/K

Permittivity of free space, $\varepsilon_o = 8.85 \times 10^{-12}$ F/m

Permeability of free space, $\mu_o = 1.26 \times 10^{-6}$ H/m

Speed of light in vacuum, $c = 2.998 \times 10^{8}$ m/s

Electron charge, $e = 1.6 \times 10^{-19}$ C

Free electron mass, $m_o = 9.1 \times 10^{-31}$ kg

Electron volt, 1 eV = 1.6×10^{-19} J

Thermal voltage, kT/q = 0.0258 V (at 300K)

Relative dielectric constant of silicon, $K_s = 11.8$

Relative dielectric constant of silicon dioxide, $K_o = 3.9$

Effective masses in silicon at 300K. Electrons: $m_n^* = 1.18\ m_o$; Holes: $m_p^* = 0.81\ m_o$

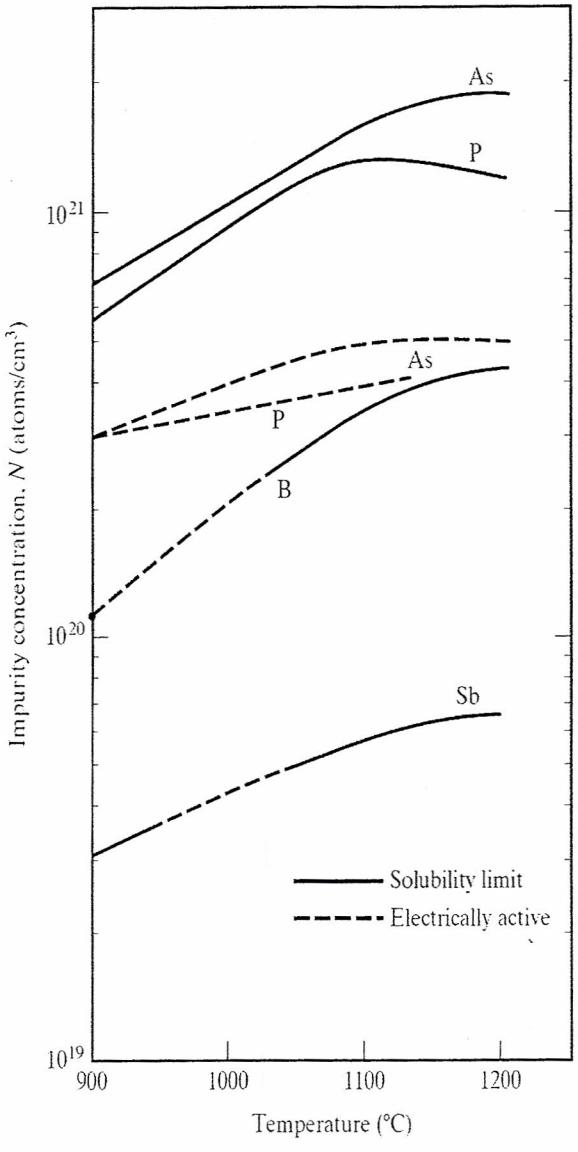
Silicon band gap at 300K, $E_g = 1.12$ eV

Intrinsic carrier concentration in Si (at 300K), $n_i = 10^{10}$ cm^{-3}

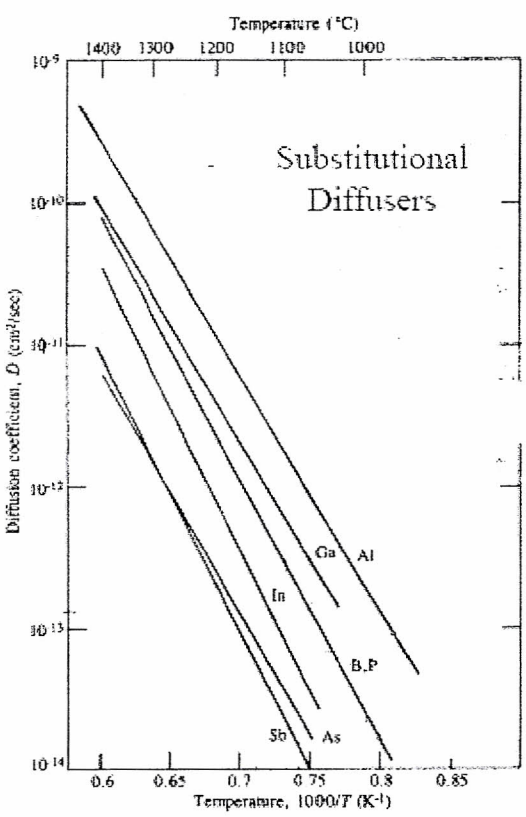
Ideal gas constant, R = 8.315 J mol^{-1} K^{-1} ; 0.082 L atm mol^{-1} K^{-1}

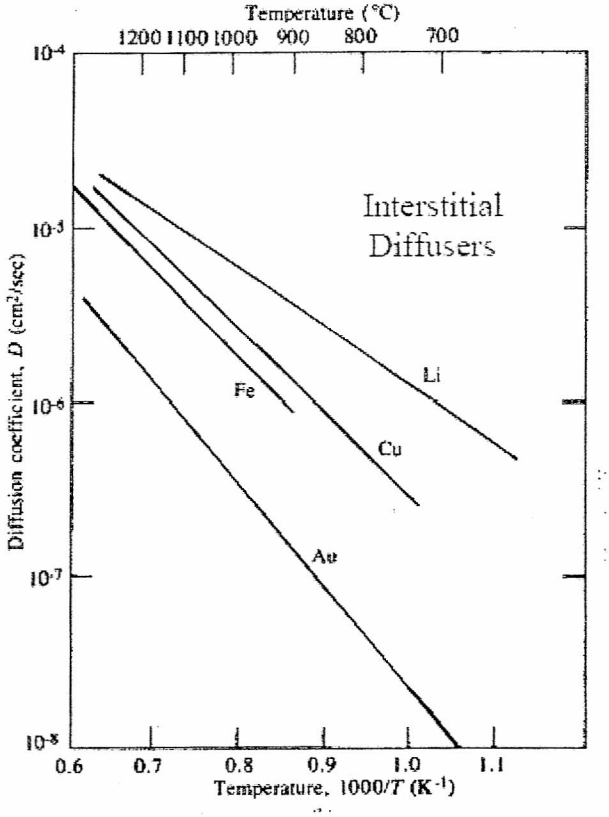
Solid Solubility Limits

Information which may be useful:

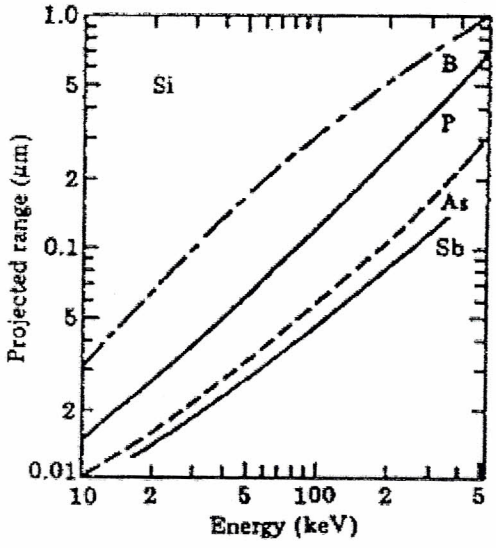


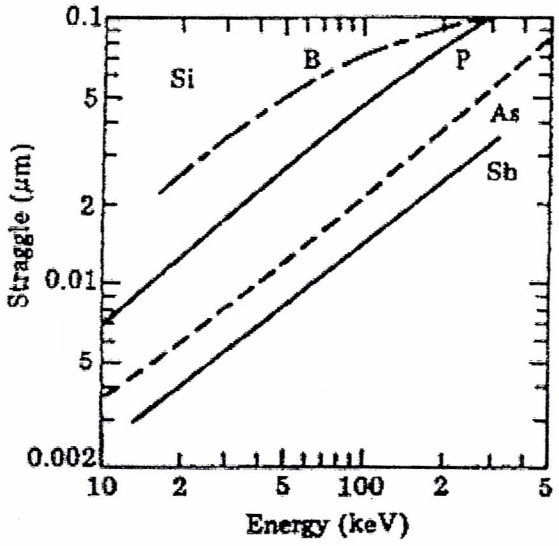
Diffusion
Information which may be useful:



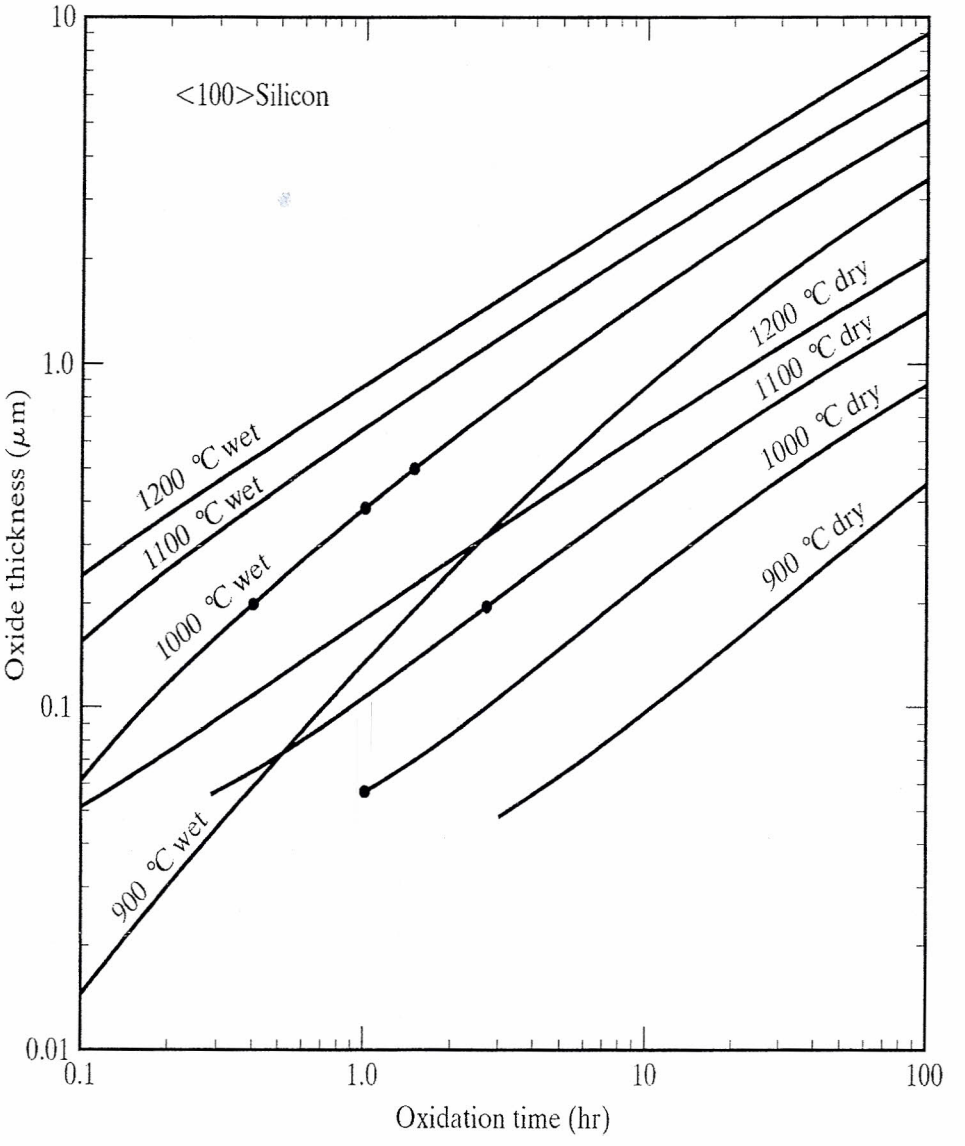


Ion Implantation
Information which may be useful:

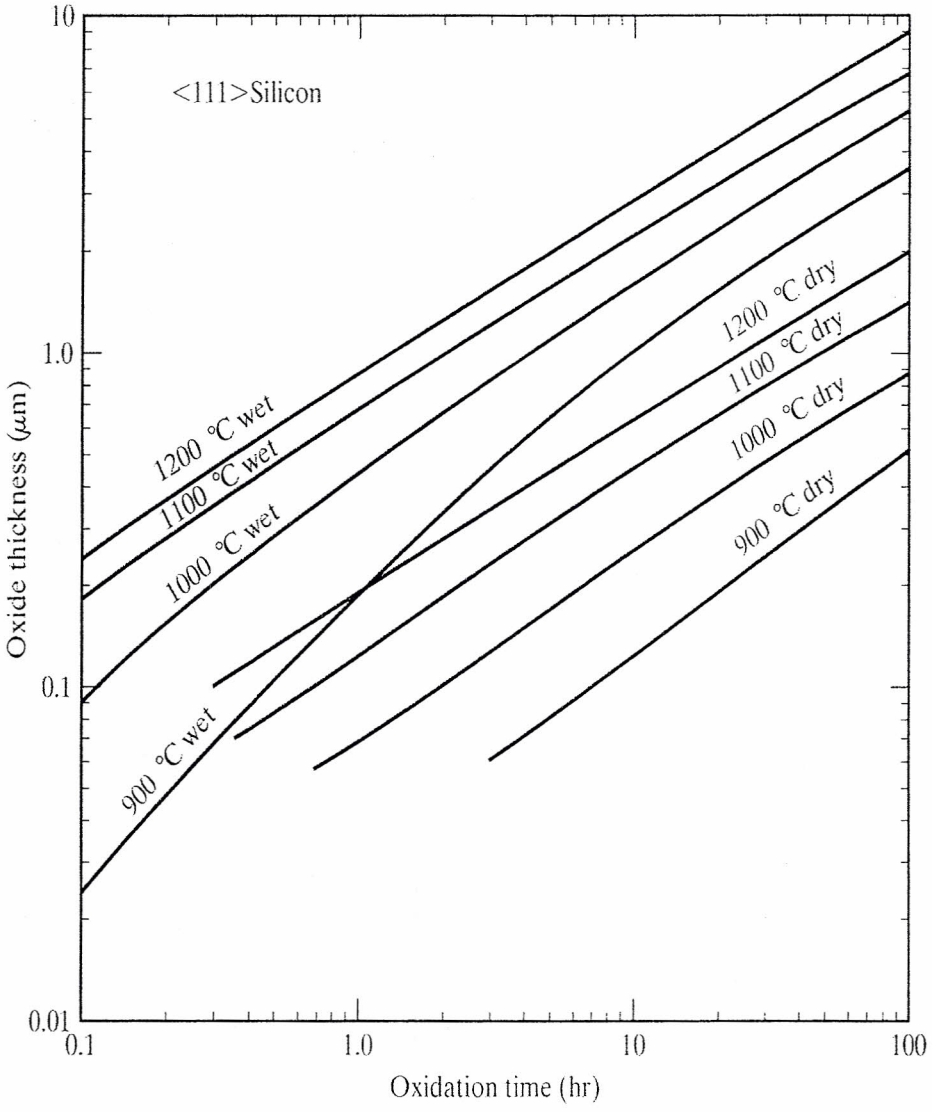




Thermal Oxidation
Information which may be useful:



Thermal Oxidation
Information which may be useful:



1) **True or False. (30points total, 2 points for each question)**

T **A)** In a p-channel MOSFET operating in the saturation region, the inversion charge density decreases from the Source toward the Drain.

F **B)** For a p-channel MOSFET pinchoff occurs when $V_D > V_{Dsat}$.

T **C)** V_T rolloff describes when MOSFET threshold voltage is reduced as channel length decreases.

T **D)** The work function of silicon depends on the doping concentration.

F **E)** At the flatband condition in an MOS capacitor, the charge density in the semiconductor is equal to the intrinsic charge density.

T **F)** In an n-channel MOSFET at threshold, the semiconductor bands bend downward towards the oxide interface.

F **G)** The threshold voltage for a n-channel MOSFET with heavily doped n-type polysilicon gate is equal to the threshold voltage for a p-channel MOSFET with heavily doped p-type polysilicon gate.

F **H)** Electrons diffuse from high concentration to lower concentration regions, while holes diffuse from low concentration to higher concentration regions.

T **I)** According to EE143 design rules, an Al to poly contact can not be directly on top of an active (thin oxide) region.

F **J)** The self-aligned source/drain implant process saves two lithography steps.

F **K)** Electromigration in metals is dominated by grain boundaries because electrons preferentially flow in the grain boundaries.

T **L)** A uniform substrate concentration profile for one dopant can be perturbed by diffusion of another dopant with a high concentration gradient.

T **M)** Anisotropic etching of silicon can be achieved using wet etching.

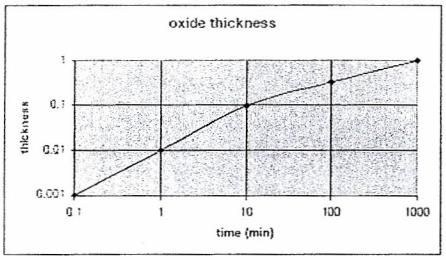
T **N)** EUV lithography requires the use of a reflection mask.

T **O)** You add acid to water to dilute the acid, but you add hydrogen peroxide to sulfuric acid to mix piranha.

2) Definitions (35 points total, 5 points for each)

Define each of the terms below in one or two sentences and illustrate the definition with a sketch. The following example illustrates the response requested.

Example: *linear rate constant* Answer: The linear rate constant in oxidation expresses the growth rate as limited by the surface reaction rate. The sketch below shows a typical growth curve for oxide; in the linear portion (short time), the slope is the linear rate constant.

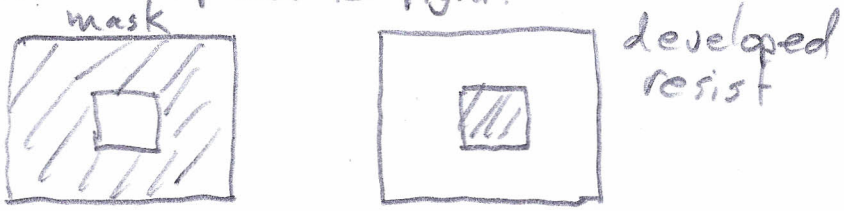


a) Optical proximity correction

Auxiliary features are added to the mask to improve feature definition

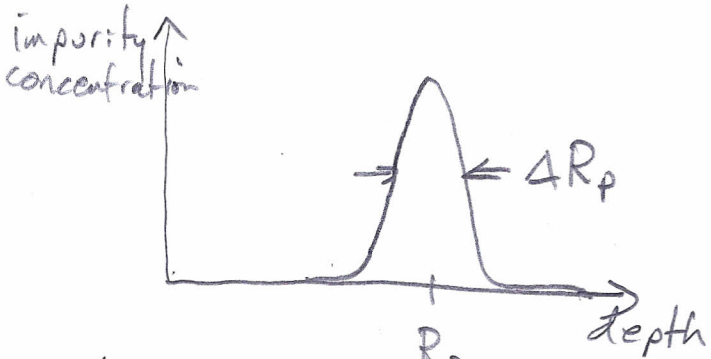
b) Negative photoresist

After development, resist remains where it was exposed to light.



c) Straggle

The random distribution of the stopping point of ions after ion implantation.



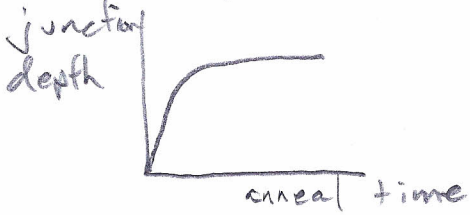
distribution of implanted impurities

Rp is the average depth of implanted ions.

ΔRp is the spread of the distribution. This is the straggle.

d) Transient enhanced diffusion

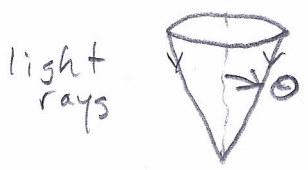
The enhancement of the impurity diffusion caused by defects (vacancies and interstitials) created by ion implantation.



The plot shows the junction depth rapidly increases with anneal time at first, due to TED. After the defects anneal out, diffusion slows down.

e) Numerical aperture

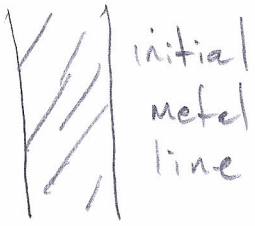
The sine of the cone angle of light produced by a focusing lens.

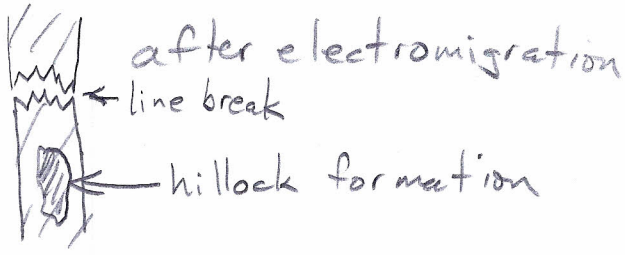


$NA = \sin\theta$

f) Electromigration

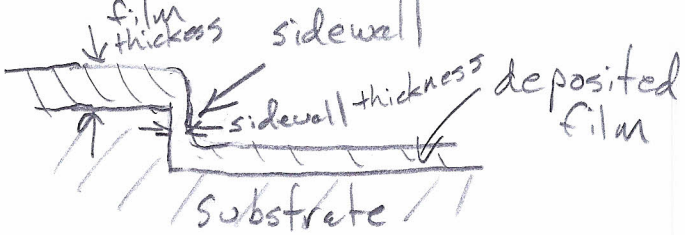
Movement of metal atoms in a wire caused by electron flow





g) Step coverage

film deposition coverage on the sidewall of a step



step coverage is the ratio of the film thickness on the sidewall to the film thickness on the flat part of the wafer

3) **CMOS (45 points total)**

a) Increasing substrate doping causes increase or decrease of MOS transistor threshold. **(5 points)**

nmos increase

pmos decrease

Explain your answers.

$$V_{TN} = \Phi_m - \chi - \frac{E_g}{2q} + |\phi_F| + \left[\sqrt{2\epsilon_s q N_B (2|\phi_F| + V_{SB})}\right]/C_{ox} - \frac{Q_i}{C_{ox}}$$

$$V_{TP} = \Phi_m - \chi - \frac{E_g}{2q} - |\phi_F| - \left[\sqrt{2\epsilon_s q N_B (2|\phi_F| - V_{BS})}\right]/C_{ox} + \frac{Q_i}{C_{ox}}$$

$|\phi_F|$ and N_B increase with increased doping for both nmos and pmos

b) A CMOS process is made with N+ poly gates for both n-channel and p-channel devices. If you switch to P+ poly gates, will it cause an increase or decrease in threshold voltage? **(5 points)**

nmos increase

pmos increase

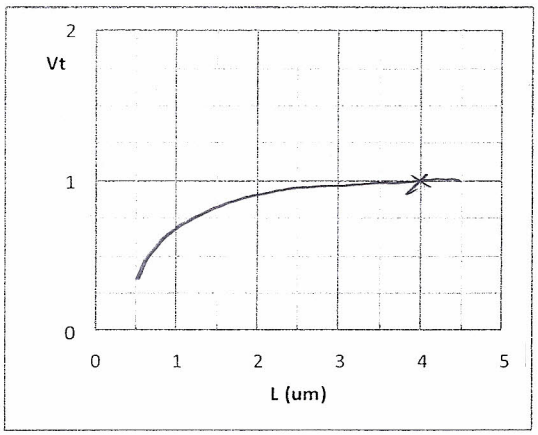
Explain your answers.

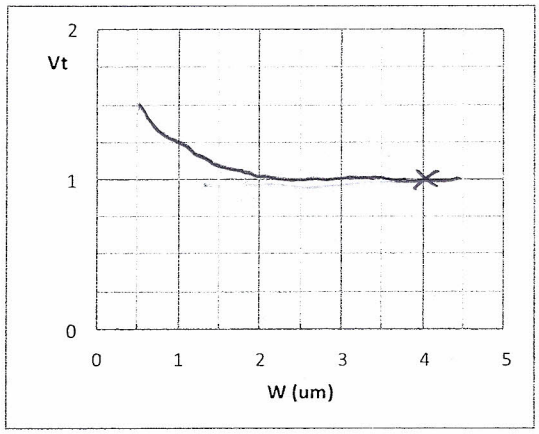
$$V_{FB} = \Phi_m - \Phi_s$$

Φ_m: gate workfunction; Φ_s: semiconductor workfunction

p^+ poly has a larger work function than n^+ poly, V_{FB} increases, so V_T increases for both nmos + pmos.

c) In a "1μm"process, a large NMOS transistor (W/L = 4μm/4 μm) is designed to have a 1V threshold. But the threshold is known to vary with W and L as they are reduced. Qualitatively complete the sketches below (i.e., get one point on the curve and show the general trend from this point.) **(10 points)**





d) If the gate oxide thickness is 50 nm, N_A = 1E15 cm^{-3}, what is the approximate threshold implant dose, and what dopant would you choose to achieve the desired 1V large device threshold voltage? Assume no fixed oxide charge or interface traps. **(25 points)**

$V_{FB} = -0.56 - |\phi_F|$

$|\phi_F| = \frac{KT}{q} \ln \frac{N_B}{n_i} = 0.026 \ln 10^5 = 0.3V$

$\therefore V_{FB} = -0.86\,V$

$V_T = V_{FB} + 2|\phi_F| + \frac{\sqrt{4\epsilon_s |\phi_F| q N_B}}{C_{ox}} - \frac{Q_i}{C_{ox}}$

$= -0.86 + 0.6 + \frac{(4 \times 1.04 \times 10^{-12} \times 1.6 \times 10^{-19} \times 10^{15} \times 0.3)^{1/2}}{6.9 \times 10^{-8}} - Q_i/C_{ox}$

$\epsilon_s = 11.8 \times \epsilon_0$
$= 1.04 \times 10^{-12}$ F/cm

$C_{ox} = \frac{3.9\epsilon_0}{50 \times 10^{-7}}$
$= 6.9 \times 10^{-8}$ F/cm²

for 1V V_T,

$1 = -0.26 + 0.2 - \frac{Q_i}{C_{ox}}$

$Q_i = qN_i$ ← implant dose

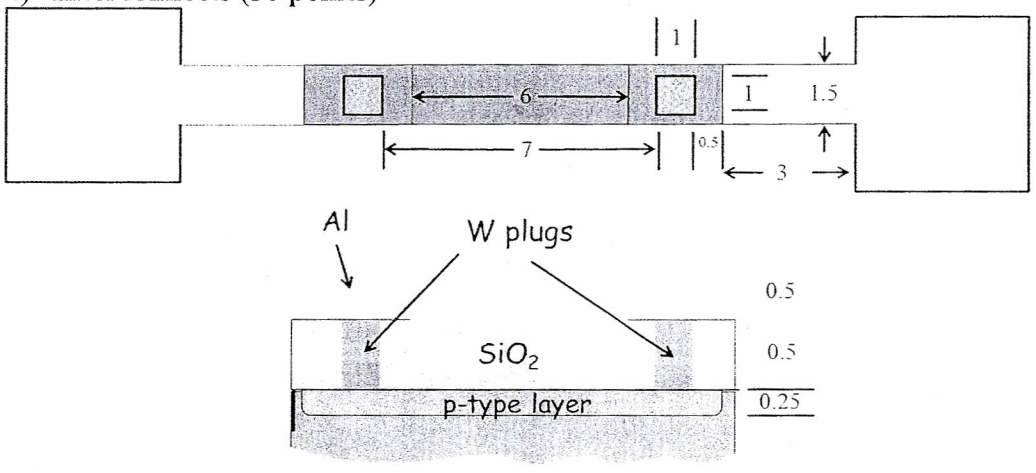
$\frac{qN_i}{C_{ox}} = (-)0.06\,V$

$N_i = 4.6 \times 10^{11}\ cm^{-2}$

need negative charge

use **Boron**

4) Interconnects (30 points)



Calculate the resistance of this structure between the two large pads on either side. All dimensions are given in μm. Assume the p-layer is uniformly doped. Neglect current crowding effect (if you don't know what that is, don't worry about it). Use the following values:

Al resistivity (μΩ-cm)	2.8
W resistivity (μΩ-cm)	5.5
W to Si specific contact resistivity (Ω-cm^2)	3.0E-6
W to Al specific contact resistivity (Ω-cm^2)	1E-8
p-layer doping (cm^{-3})	1E19
Hole mobility (cm^2/V-s)	100

On one side

Al line: $L = 3 + 0.5 = 3.5$ $W = 1.5$ $T = 0.5$

$R_{AL} = \rho \frac{L}{WT} = 0.13\ \Omega$

W plug: $L = 0.5$ $W = 1$ $T = 1$

$R_W = 0.03\ \Omega$

W-Si contact:

$R_c = \rho_c / A$ $A = \mu m^2 = 10^{-8}\ cm^2$

$R_c = 300\ \Omega$

W-Al contact

$R_c = 10^{-8}/10^{-8} = 1\ \Omega$

Si resistivity $\rho_{Si} = (p \cdot q \cdot \mu)^{-1} = \left(10^{19} \times 1.6 \times 10^{-19} \times 100\right)^{-1} = 0.0063\ \Omega\text{-cm}$

(p: hole concentration; μ: mobility)

Silicon line $L = 7\ \mu m$ $W = 1.5$ $T = 0.25$

$R_{Si} = 1.18\ k\Omega$

Total $R = 2(R_{Al} + R_W + R_{W\text{-}Si} + R_{W\text{-}Al}) + R_{Si} = \boxed{1.78\ k\Omega}$

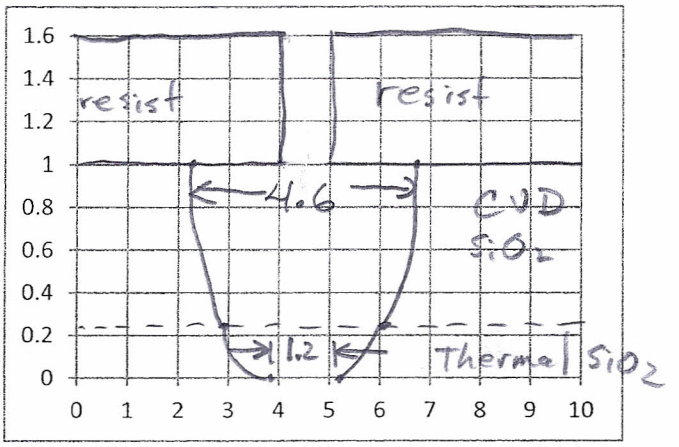
5) Process integration (60 points total, 15 points for each diagram)

For each of the 4 following process sequences, carefully and neatly sketch a cross-section through the stated feature at the end of the sequence given. Note scales on sketches. Indicate all important dimensions on your diagrams. **Neatness counts for 30% of the grade**. Note that except for parts c&d, these are all independent, so you can do (b) without doing (a), etc.

a)

i) Grow 0.25 μm thermal oxide on Si
ii) Deposit 0.75 μm CVD oxide
iii) Photomask 1μm × 1μm openings for contacts. Resist 0.6 μm thick.
iv) Wet etch 6 min BHF (etch rate 0. 1 μm /min thermal oxide, 0.3 μm /min for CVD oxide). Assume infinite selectivity to resist.

Draw cross section through the contact on the given chart. Units are in μm. A good estimate of the final oxide thickness is adequate.

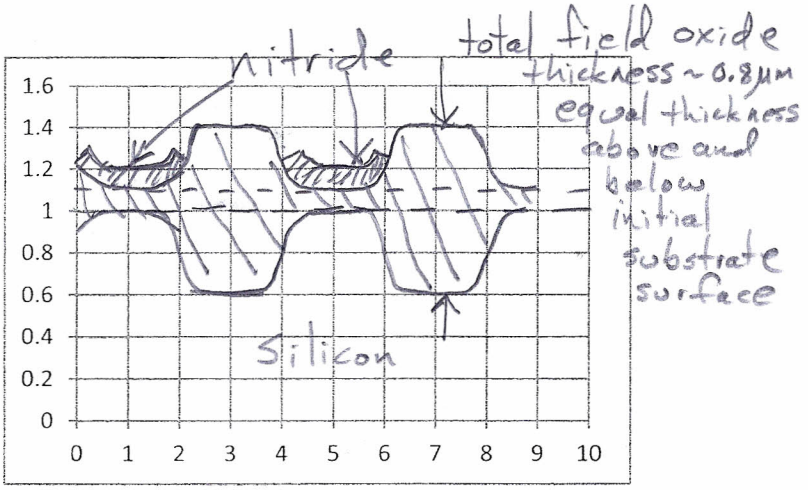


0.75/0.3 = 2.5 min to etch CVD oxide. 3.5 min overetch
3.5 × 0.3 = 1.05 μm lateral etch.
3.5 min etch of thermal oxide. 1 min overetch. 0.1 μm lateral etch

b)

i) Grow 0.1 μm thermal oxide on Si
ii) Deposit 0.1 μm Si_3N_4
iii) Photomask 2 μm lines and spaces
iv) Etch Si_3N_4 (anisotropy plasma etch, selectivity Si_3N_4 vs. oxide 4:1)
v) 20% overetch; remove resist
vi) Wet oxidation (0.75 μm oxide on bare test wafers)

Draw cross section through at least one line and space.



c)

i) Grow 0.1μm thermal oxide on Si

ii) Deposit 0.5μm Polysilicon

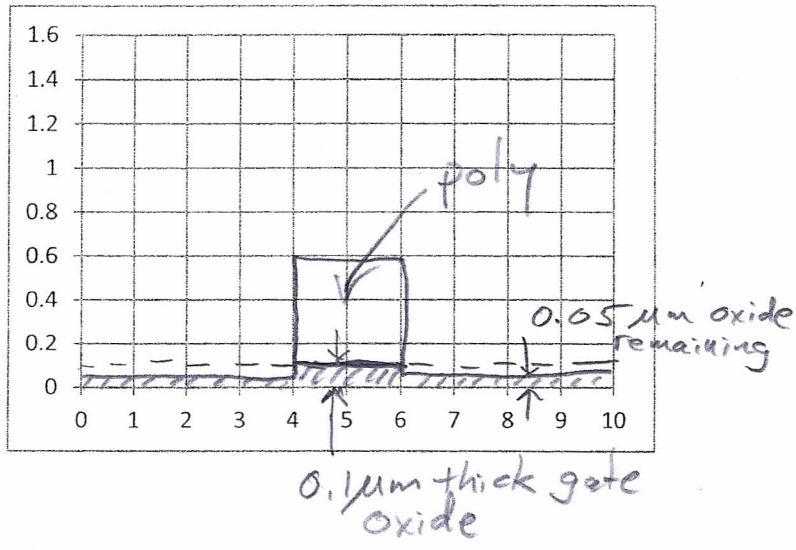
iii) Dope with Phos 900°C

iv) Photomask 2μm wide gate pattern

v) Plasma etch Poly in fully anisotropic etch with 20% overetch. Selectivities: poly vs. oxide 2:1, poly vs. resist 10:1

vi) Remove resist

Draw cross section through the gate.



d) Continuation of (c)

i) Deposit 0.5μm CVD oxide

ii) Plasma etch oxide in fully anisotropic etch. Etch rate same for CVD and thermal oxide. Etch to remove 0.5μm plus 20% overetch. Selectivities: oxide vs poly 5:1, oxide vs. Si 5:1

Draw cross section through the gate.