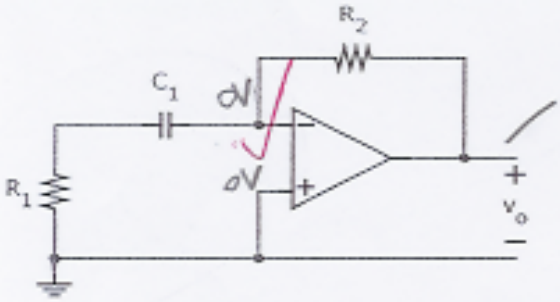
Problem 1		Points of 10
Problem 2		Points of 10
Problem 3		Points of 20
Problem 4		Points of 20
Problem 5		Points of 20
Problem 6		Points of 20
Score		%

- Closed book, closed notes
- One pocket calculator permitted (no PDAs, laptops, cell phones, or other electronic devices)
- Show derivations to get partial credit in case of numerical errors
- Cross out incorrect attempts (no partial credit for ambiguous derivations)
- Write results into boxes
- Take off hats or caps and leave backpacks and electronic devices in isle
- You may assume that all operational amplifiers are ideal
- Use only positive values (≥ 0) for all passive components (resistors, capacitors, inductors)
- Verify that an assistant receives your completed exam!

1. In the circuit below, $v_o(t = 0) = 5.2\,\text{V}$. Derive an expression for $v_o(t)$, $t > 0$. Use $R_1 = 25\,\text{k}\Omega$, $R_2 = 75\,\text{k}\Omega$ and $C_1 = 8.8\,\mu\text{F}$.

$v_o(t)$ (algebraic result) $(5.2\text{V})\,e^{-\frac{+}{(R_1+R_2)C_1}}$ 5 pts 0

$v_o(t = 175\,\text{ms})$ 4.26V 2 pts 1



$(I_{R2} \cdot R_2)$

$V_o = IR_2 = I_C R_2$ $\quad I_C = \frac{5.2}{R_2} e^{-\frac{+}{(R_1+R_2)C_1}}$

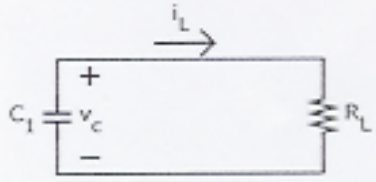
$I_C(0) = \frac{5.2}{R_2}$ $\quad V_o = \frac{R_2 \cdot 5.2}{R_2} e^{-\frac{+}{(R_1+R_2)C_1}}$

$= 5.2\, e^{-\frac{+}{(R_1+R_2)C_1}}$

$V_o(.175) = 4.26\text{V}$

2. Capacitor $C_1 = 688\,\text{mF}$ is used to power a model airplane modeled by resistor $R_L = 387\,\Omega$. Initially the capacitor is charged to $v_c = 7\,\text{V}$. Calculate the fraction r of the initial energy remaining on the capacitor and the voltage v_c across the capacitor after i_L has decreased to 75 percent of its initial value. After what time T is this condition reached?

$r =$	.5625	3 pts. 2
$v_c =$	5.25 V	3 pts. 3
$T =$	76.6 s	4 pts. 4



$E = \frac{1}{2}CV^2$

$V = IR$

$E_i = \frac{1}{2}CI^2R^2$

$E_f = \frac{1}{2}C(.7I)^2R^2$

$E_f = .5625\,E_i$

(a) $r = .5625$

(b) $V_c = .75\,IR = .75\,V_0 = 7(.75) = 5.25$

(c) $V_c = 7e^{-t/R_LC}$

$-\ln\frac{5.25}{7} \cdot R_L \cdot C = t = 76.5975\ \text{s}$

3. You have been hired by SnapOMatic, a fledgling startup making ultra-low power cameras. Your job is to redesign their image compression chip to use less energy.

The current solution consists of $N = 8 \times 10^6$ gates. Each gate drives an average capacitance $C_{in} = 2.4$ fF. The image compression algorithm takes $M = 3 \times 10^6$ clock cycles (operations) per image. The activity factor, i.e. percentage of gate outputs changing in each clock cycle is $\eta = 24\%$. The maximum operating frequency f_s depends on the supply voltage V_{dd} and is

$$f_{s,max} = 400 \frac{\text{MHz}}{\text{V}^2} \times V_{dd}^2.$$

a) Calculate the time T_1 and energy E_1 required to compress one image if the processor is operating at its maximum frequency for $V_{dd} = 1$ V.

$T_1 =$ 7.5 ms 3 pts. ✓
$E_1 =$ 6.91 mJ 5 pts. ✓

b) The marketing department found a great opportunity for a chip that consumes only $E_x = 690.8\ \mu$J per compressed image. Calculate the operating frequency f_x and supply voltage $V_{dd,x}$ for the existing chip such that the energy per compressed image is E_x.

$f_x =$ 39.98 MHz 3 pts. ✓
$V_{dd,x} =$ .316 V 7 pts. ✓

c) Your friend who took CS61p learned about a parallelized image compression algorithm that has no overhead. What is the number of processors P needed to achieve image compression in 351 μs and only 6.9 mJ energy per compressed image? At what frequency $f_{s,p}$ are they operating?

$P =$ 22 2 pts. ✓
$f_{s,p} =$ 400 MHz 2 pts. ✓

a) $f = 400$ MHz
$M = 3 \times 10^6$

$T = 3 \times 10^6 \cdot \frac{1}{400 \times 10^6} =$ 7.5 ms

$E = \frac{1}{2} C V^2 \cdot \eta \cdot M \cdot N = (.5)(2.4 \times 10^{-15})(1^2)(.24)(3 \times 10^6)(8 \times 10^6)$

$= .0069$ J

b) $690.8 \times 10^{-6} = \frac{1}{2} C V_x^2 \cdot \eta \cdot M \cdot N$

$V_x^2 = \frac{690.8 \times 10^{-6}}{.5 \cdot 2.4 \times 10^{-15} (.24)(3 \times 10^6)(8 \times 10^6)} = .0999$

$V_x = \sqrt{.0999} =$ .316 V

$f = 400 \times 10^6 \cdot V_x^2 =$ 39.98 MHz $= 39.98 \times 10^7$ Hz

C on back

$E = 6.9\ mJ = \frac{1}{2} C V^2 \cdot \eta \cdot \frac{M}{\rho} \cdot N \cdot \rho$

$V^2 = \frac{6.9 \times 10^{-3}}{(.5)(2.4 \times 10^{-5})(.24)(3 \times 10^6)(1 \times 10^9)} = 1$

$V = 1V$

$F_{max} = 400 \times 10^6 \times 1^2 = 400 \times 10^6$

$T_{(one\ image)} = \frac{1}{400 \times 10^6} \cdot 3 \times 10^6 = .0075\ s$

desired time = 351 ms

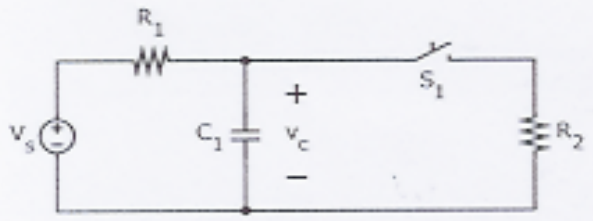
$P = \frac{.0075}{351 \times 10^{-6}} = 21.37$

Need 22 processors

4. In the circuit below, switch S_1 closes when v_c increases above $0.7 \times V_s$. It then remains closed until v_c has dropped to $0.3 \times V_s$, at which point it opens and stays open until $v_c > 0.7 \times V_s$. Find the value of C_1 such that the switch opens every $6.2\ \mu s$ in steady state.

Use $R_1 = 7.9\ k\Omega$, $R_2 = 2.8\ k\Omega$ and $V_s = 3.2\ V$.

$C =$ .68 nF 30 pts 11 × ~ 6



Charge =

$V_c = V_s(1 - .7e^{-t/R_1C_1})$

$-\ln\frac{.3}{.7} \cdot R_1 \cdot C_1 = t_1$

$t_1 + t_2 = 6.2\ \mu s$

-4 τ_2 ($V_2(\infty)$)

discharge

$V_c = .7e^{-t/R_2C_1}$

$-\ln\left(\frac{.3}{.7}\right) \cdot R_2 \cdot C_1 = t_2$

$C_1 \ln\left(\frac{.7}{.3}\right)(R_1 + R_2) = 6.2 \times 10^{-6}\ s = t_1 + t_2$

$= 6.84 \times 10^{-10}\ F$

$C_1 = .68\ nF$

5. In this problem we design a "step down converter" (Buck converter) to efficiently convert the input voltage $V_s = 60\,\text{V}$ to a lower value $v_o = 20\,\text{V}$. Such circuits are employed in the familiar "power bricks" used to power laptops and gadgets from the grid. In the diagram below the switch is controlled by a periodic waveform. It is closed for a period T_1, followed by a period $T_2 = T - T_1$ during which it is open, with $T = T_1 + T_2 = 2.4\,\mu\text{s}$. The diode D_1 acts like a "valve": current passes for $v_d \geq 0\,\text{V}$; for $v_d < 0\,\text{V}$ the diode behaves like an open circuit.

Assume that the circuit operates in "steady state", i.e. the voltage and current waveforms in the circuit repeat with period T. To simplify the analysis, assume that the output voltage v_o is constant and equal to the design value specified above. This leads to minimal errors when the ripple is small. In practice we would verify the circuit with SPICE to check if all assumptions are valid and we have not made design errors.

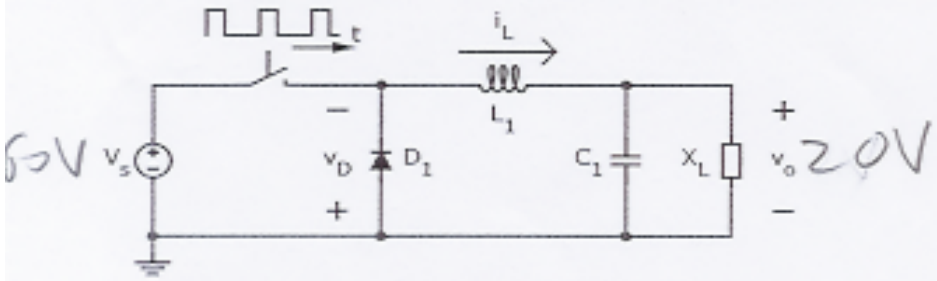
a) Find T_1 and T_2.

$T_1 =$ .8 µs (5 pts. 12)

$T_2 =$ 1.6 µs (5 pts. 13)

b) Find the minimum value of L_1 that results in $\Delta i_L = 34\,\text{mA}$.

$L_1 =$ 941 µH (10 pts. 14)



T_{ON}:

$$i_L = \frac{V_S - V_o}{L} \cdot t = \frac{40\,t_{on}}{L}$$

T_{OFF}:

$$i_L = \frac{20}{L}\,t_{off}$$

$$\frac{60-20}{L}\,t_{on} = \frac{20}{L}\,t_{off}$$

$$\frac{t_{on}}{t_{on}+t_{off}} = \frac{20}{60}$$

$$\frac{t_{on}}{2.4\,\mu s} = \frac{1}{3} \qquad t_{on} = 8\times10^{-7}\,s$$

$$t_{off} = 2.4\times10^{-6} - t_{on} = 1.6\times10^{-6}$$

$$\Delta i_L = \frac{40\,t_{on}}{L} = .034$$

$$L = \frac{40\cdot t_{on}}{.034} = 9.41\times10^{-4} = 941\,\mu H$$

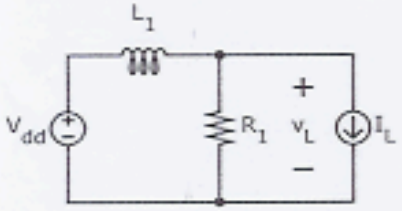
6. The supply current flowing into digital circuits consists of large spikes with magnitude $I_{L,max}$ at the beginning of each clock cycle of duration $T = 1/f_s$. The circuit below shows a simplified model of this behavior, consisting of current source I_L that models the current spikes, and resistor R_1 that models the constant part of the supply current flowing into the circuit. Also included in the model are the power supply V_{dd} and the wiring inductance L_1.

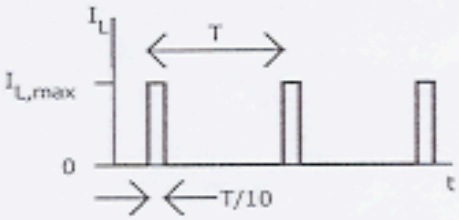
Parameter: $V_{dd} = 1.2\,\text{V}$, $L_1 = 3.8\,\text{nH}$, $R_1 = 9.8\,\Omega$, $I_{L,max} = 3.9\,\text{A}$, $f_s = 3\,\text{GHz}$.

a) Calculate the minimum value of v_L in steady state.

$v_{L,min} =$ $-3.219\,\text{V}$ 5pts ok

b) (15 points) For the digital circuit to operate properly, it is necessary that $v_{L,min} > 0.9\,V_{dd}$ at all times. Propose a circuit modification that accomplishes this goal. You are only allowed to add circuit components (only capacitors and inductors are available). Use the minimum number of components required to meet the specification and use the minimum required value for all components. Specify all component values. Suggestion: to simplify the analysis, you may assume that $v_L = V_{dd}$ at the start of each clock cycle. In practical situations, the error from this approximation is usually negligible. Of course you would verify this using e.g. a circuit simulator.





(a) at steady state $I_{R_1} = \frac{V_{dd}}{R_1} = I_{L_1} = \frac{1.2}{9800} = .122\,\text{mA}$

at spike, $I_{L1} = .122\,\text{mA}$ $I_{R_1} = .122\,\text{mA} - I_{Lmax}$

$= -3.9\,\text{A}$

$V_{Lmin} = -3.9 \cdot R_1 = -3.8218\,\text{V}$ 10

$R_1 = 9.8\,\Omega$

(b)

Add capacitor to stabilize voltage across circuit.

$\Delta V_C = \frac{\Delta Q}{C_1} = \frac{i\,t}{C_1} = .1V_{dd}$ $C_1 = \frac{I_{Lmax}\left(\frac{T}{10}\right)}{.1V_{dd}} = 1.08\,\text{nF}$ ✓

↑ change voltage by .1 of its initial value

$V_{new} = V_0 - \Delta V_C = 1V_{dd} - .1V_{dd} = .9V_{dd}$