University of California at Berkeley
College of Engineering
Dept. of Electrical Engineering and Computer Sciences

EECS 40 Midterm II

Fall 1998 | Prof. Roger T. Howe | November 19, 1998

Name: _____

Student ID: _____

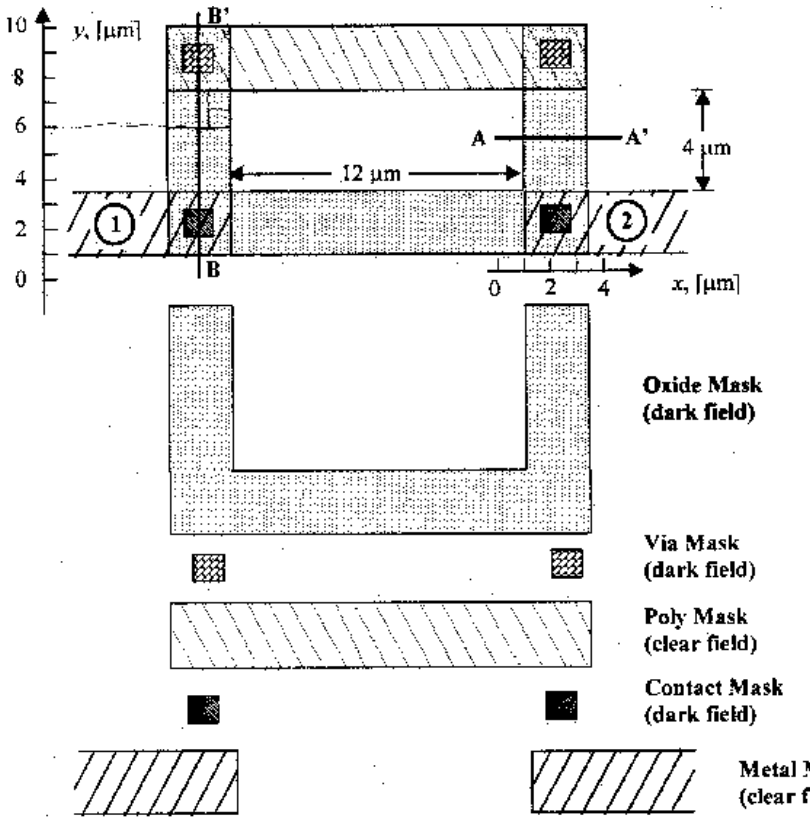
Guidelines

1. Closed Book and notes; one 8.5" x 11" page (both sides) of your own notes is allowed.
2. You may use a Calculator
3. Do not unstaple the exam.
4. Show all your work and reasoning on the exam in order to receive full or partial credit.

Score

Problem	Possible Points	Score
1	24	
2	18	
3	8	
Total	50	

1. Integrated Circuit Structure [24 points]



Process Sequence:

1. Starting Material: boron-doped silicon, concentration 5 x 10^{16} cm^{-3}
2. Deposit 250 nm of silicon dioxide and pattern using the **oxide mask** (dark field)
3. Implant phosphorus and anneal (depth 500 nm and concentration 1.25 x 10^{17} cm^{-3}
4. Deposit 250 nm of slicon dioxide and then etch 250 nm of oxide using the **via mask** (dark field).
5. Deposit 250 nm of aresenic-doped polysiliconsilicon and pattern using the **polymask** (clear field). The arsenic concentration is 5 x 10^{18} cm^{-3}
6. Deposit 250 nm of silicon dioxide and then etch 500 nm of oxide using the **contact mask** (dark field).
7. Depoist 500 nm of aluminum and pattern using the **metal mask** (clear field).

Given :	single cyrstal silicon:	mu_n = 1000 cm^2/(Vs)	mu_p = 400 cm^2/(Vs)
	polysilicon:	mu_n = 100 cm^2/(Vs)	mu_p = 50 cm^2/(Vs)

(a) [8 pts.] Sketch the cross section **A-A'** on the graph below. Identify all layers clearly.

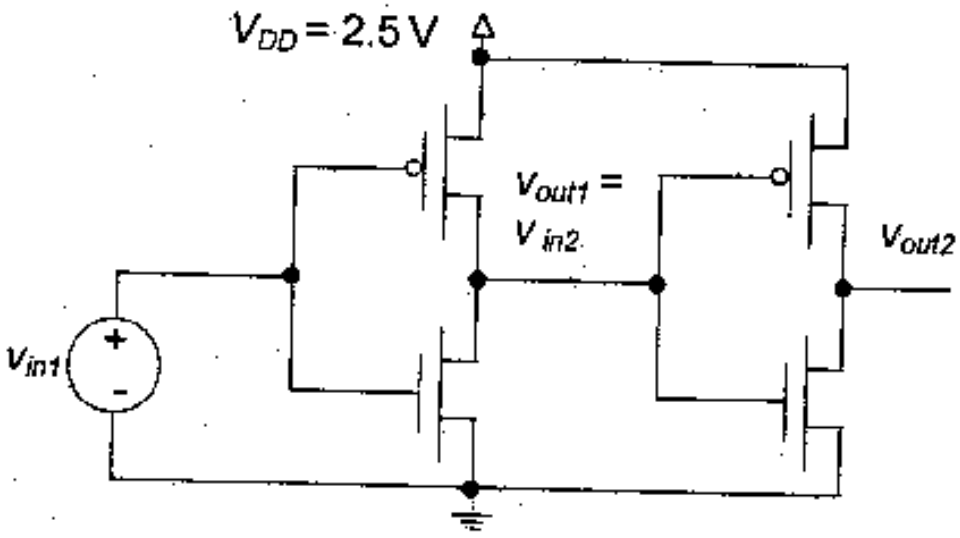
(b) [8 pts.] Sketch the cross section **B-B'** on the graph below. Indentify all layers clearly.

(c) [2 pts] What is the sheet resistance $R_{square,\ poly}$ of the polysilicon layer in ohms/square? Given : the magnitude of the hole or electron charge is 1.6 x 10^-19 C.

(d) [2 pts.] What is the sheet resistance $R_{square,\ implant}$ of the phosphorus-implanted layer [ohm/square]?

(e) [4pts] What is the numerical value of the resistance between terminals 1 and 2? You can neglect the "end squares" at connections between the conducting layers. If you have ano answers for parts (c) and (d), you can use $R_{square,\ poly}$ of = 250 ohms/square for the polysilicon layer and that $R_{square,\ implant}$ = 150 ohms/square for the phosphorus implanted layare for this part.

2. CMOS inverter pair [18 points]



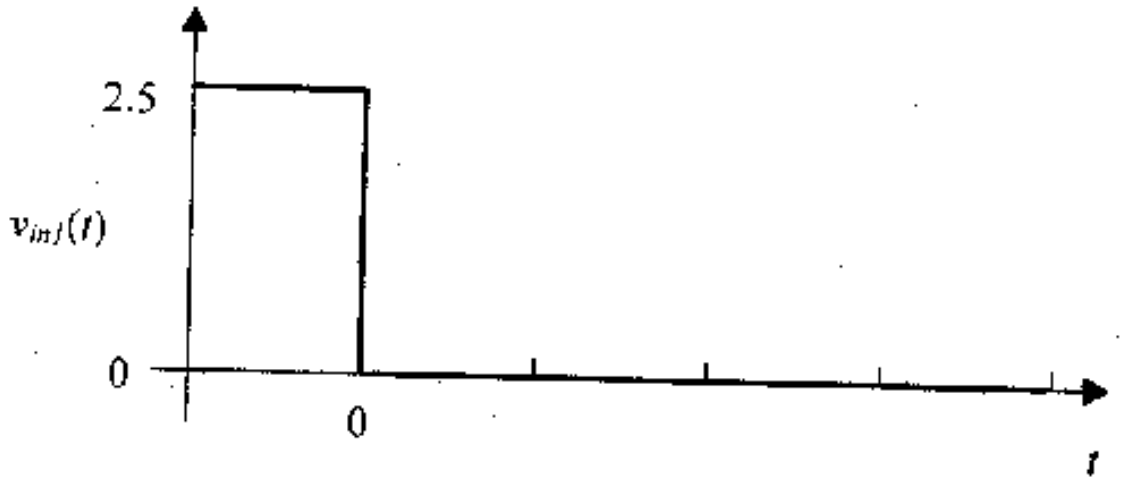
Gate capacitance:
$C_{ox} = 2$ fF/μm^2

PMOS:
Width = $W_p = 3$ μm
Length = $L_p = 0.5$ μm
"on" resistance = $R_p = 200\ \Omega$

NMOS:
Width = $W_n = 2$ μm
Length = $L_n = 0.5$ μm
"on" resistance = $R_n = 150\ \Omega$

(a) [4pts.] This inverter pair ahs been "at rest" for some time with its input "high." The wave for for $v_{in1}(t)$ is sketched

below. Draw teh switch-model circuit for finding the output voltage $v_{out1}(t)$ of inverter 1 for t > 0. Provide some numerical values for the circuit elements. You can neglect the drain-bulk capacitances and any wire capacitance.



(b) [4 pts.] Determine the wave form $v_{out1}(t)(t)$ for t>0.

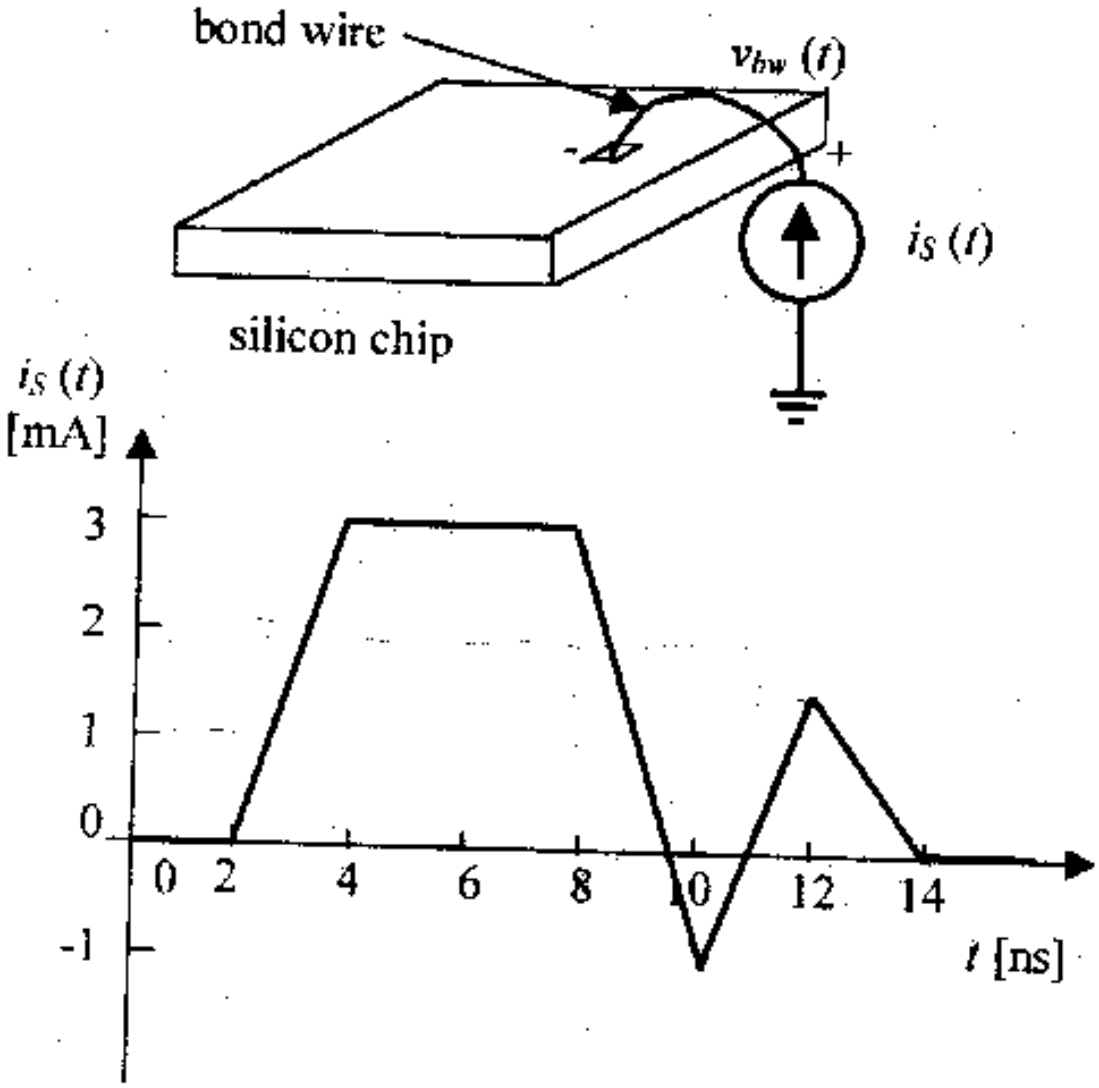
(c) [4pts.] Due to contamination of the gate oxide furnace, you discover that the gate oxide is not a perfect insulator, but instead is modeled by a resistance R_G = 1 kOhm in parallel with the gate-source capacitance (C_{Gn} for the NMOS, C_{Gp} for the PMOS). Repeat part (a) using these "leaky" NMOS and PMOS transistors for both inverters.

(d) [3pts] What is the value of $v_{out1}(t)(t<0)$ for the circuit in part (c), assuming the input wave form $v_{in1}(t)$ that is given in

part (a). Note that the inverter has had a "high" input for a long time before its input transitions at t = 0.

(e) [3pts.] What is the value of $v_{out1}(t)$(t approaches infiniti) for the circuit in part (c), assuming the input waveform $v_{in1}(t)1$ (t) that is given in part (a). Hint: consider superposition.

3. Bond wire inductance [8 points]



(a) [5pts] The bond wire can be modeled by a 1 nH inductor. Given the wave form for the supply current $\boldsymbol{i}_s(t)$, plot the voltage drop across the bondwire $\boldsymbol{v}_{bw}(t)$ on the graph below.

(b) [3pts] A particular circuit can tolerat at most | $\boldsymbol{v}_{bw}(t)$ | = 250 micro - V for a critical application. How many bondwires are needed to meet this requirement, given the $\boldsymbol{i}_s(t)$ waevform? Hint: consider whether series or parallel bond wires will help.
