# EE 122, Spring 1997 <br> Midterm \#2 <br> Professor Edell 

## Problem \#1

## Multiple Choice \& Why (25 possible points)

In this problem you are to select which of the multiple choices are most correct or most appropriate. Please circle the appropriate roman numeral to indicate your selection. Then you are to explain why your selection is most correct/appropriate. Approximately $1 / 5$ credit is given for the "choice" and $4 / 5$ for the explanation.
A) (5 points) A BCH code with a minimum distance between codewords of 7 may be used to
i. detect up to 7 errors (per block).
ii. correct up to 4 errors (per block).
iii. correct up to 3 errors (per block).
iv. correct up to 2 errors and detect up to 5 errors (per block).
v. none of the above.

Explain why:

## B) ( 5 points) ATM cells are 53 bytes long because

i. the 48 byte payload is just large enough for an IP+TCP header.
ii. the ATM designers patented a fast divide-by- 53 algorithm.
iii. small cells mean low latency for low data rate CBR applications.
iv. 53 byte cells, together with 11 bytes of overhead, fit nicely (i.e. with little additional overhead) into a DS-1 frame.
v. none of the above.

Explain why:
C) ( 5 points) TCP uses a combination of GBN \& SRP. Therefore, TCP is rather complicated. It is
possible to design a simpler transport layer (i.e. end-to-end on top of IP that uses ABP?
i. True.
ii. False.

Explain why:
D) (5 points) Statistically multiplexing 24 constant bit-rate channels will result in a statistical multiplexing gain of approximately
i. 2.4
ii. 1.2
iii. 1.0
iv. 0.75
v. None of the above.

Explain why:
E) ( 5 points) There are several reasons why virtual circuit switching is used in ATM. Which of the following is *not* a reason?
i. VCI fields are smaller than nodes names -> less overhead in small cells.
ii. admission control -> allows for QoS
iii. out-of-band signalling -> better security, reduces fraud.
iv. VC switching is faster than datagram switching.

Explain why:

## Problem \#2

## Framing (20 possible points)

In class, we have discussed five different approaches used to locate the beginning of a data link layer frame (Ethernet, FDDI, HDLC, ATM over DS-3, ATM over SONET). You are to describe how three of these approaches work. Choose the three approaches with which you feel most comfortable.

|  | How to locate beginning of <br> Approach <br> Type | a frame. (Be certain to <br> specify the indications <br> provided by the physical <br> layer for this approach.) | How to avoid "false <br> framing." |
| :--- | :--- | :--- | :--- |
|  |  |  | What is the "cost" of this <br> approach? (i.e. how many <br> extra bits are added?) |
| Indicate <br> your first <br> framing <br> approach <br> here: |  |  |  |
|  |  |  |  |



| \| |  |
| :---: | :---: |

## Problem \#3

## ARQ vs $F E C+A R Q$ ( 30 possible points)

 duplex) that transfers data at a high data rate ( $100 \mathrm{Mbit} / \mathrm{sec}$ ). Due to the long fiber length, the (independent) bit error rate is quite bad $\left(10^{-3}\right)$. Our data packets will be 4500 bits long (including a 32 bit CRC); the acknowledgments will be 500 bits. We will use Go-Back-N for error control. The processing time in the nodes is zero. (Assume that light within this fiber propogates at a rate of 300,000 $\mathrm{km} / \mathrm{sec}$.)

## A) Please do the following analysis for the case of no Forward Error Correction (FEC).

i. What is the packet success rate? (i.e. the likelihood that a packet and its acknowledgment are received correctly.)
ii. What window size should be used?
iii. What is the realized transmission rate? (i.e. not including CRC, acks, etc.)
B) Now consider the case where we use a 127 bit BCH code that can correct for 1 error per block. (This code carries $\mathbf{1 2 0}$ bits of error-protected data per block.) You should probably calculate how many blocks are used for the data and acknowledgment packets first.
i. What is the packet success rate?
ii. What window size should be used?
iii. What is the realized transmission rate? (i.e. not including CRC, FEC, acks, etc.)
C) Now consider the case where we use a 127 bit BCH code that can correct for 2 errors per block. (This code carries 113 bits of error-protected data per block.) You should probably calculate how many blocks are used for the data and acknowledgment packets first.
i. What is the packet success rate?
ii. What window size should be used?
iii. What is the realized transmission rate?

## Problem \#4

## ATM Traffic Descriptors and Call Admission (25 possible points)

Suppose that you are an ATM network customer. You wish to transmit the periodic traffic stream with th eprofile $\mathrm{s}(\mathrm{t})$ as depicted in the figure below. Before you man begin transmitting your traffic, you must describe your traffic profile to the network. You will describe your traffic profile by specifying a pair of parameters ( $\mathrm{x}, \mathrm{y}$ ). These parameters indicates the "dimensions" of a buffer as shown the figure. (These parameters may also be used to indicate the parameters of a leaky-bucket traffice policer.)

A) Describe the trade-offs between $\mathbf{x} \boldsymbol{\&} \mathbf{y}$ os that the buffer never overflows.
i. calculate the amount of buffering required (x) to avoid buffer overflow using the link data rate (y) as a parameter.
ii. For $y=4$ : sketch the buffer occupancy $o(t)$ and the traffic profile of the output s_hat $(t)$.
iii. Leaving ( $\mathrm{x}, \mathrm{y}$ ) as parameters (but related as specified in part i ), express the average delay experienced by the traffic due to the buffer.

## B) Call Admission

i. Besides the traffice profile descriptor, what else does the network customer specify when requesting a connection?
ii. Suppose that a particular ATM switch in the network has 100 units of buffer space and 80 units of bandwidth. How many traffic sources with profile $s(t)$ may be admitted to this buffer?
iii. For your parameters from part ii, what is the statistical multiplexing again?

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