EE105, Spring 1997
Midterm #2
Professor R. T. Howe

(NOTE: Greek letters are sometimes written in Roman alphabet in all caps. Subscripts are written A_1, etc. Micro is sometimes represented by a 'u'.)

Default bipolar transistor parameters:

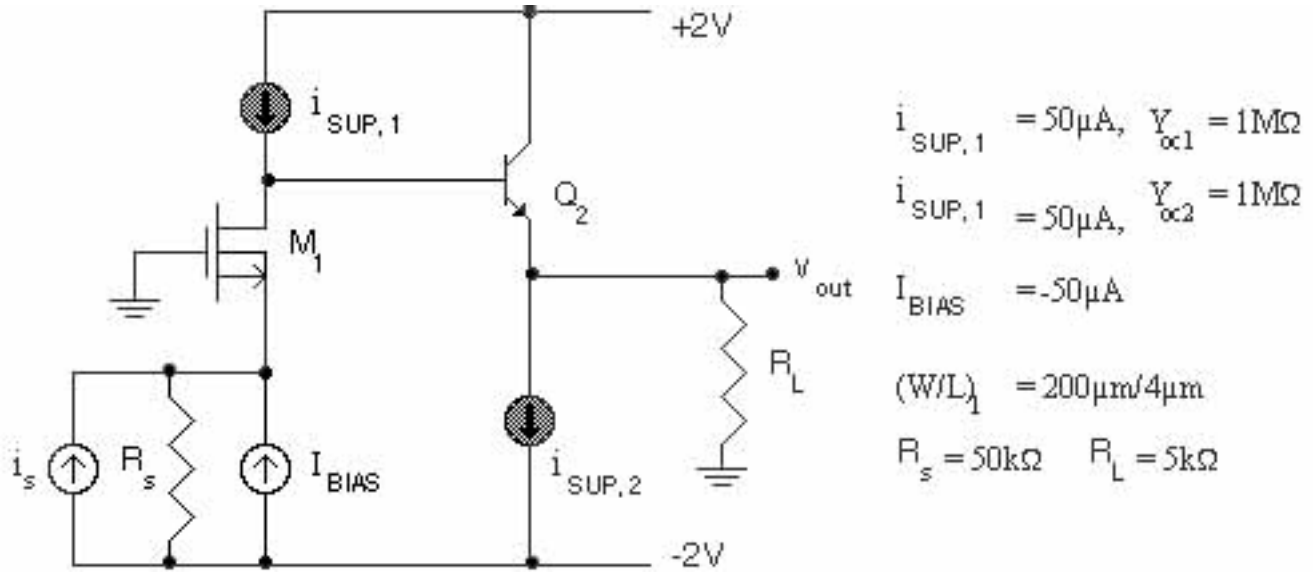
npn: BETA_n = 100, V_A_n = 50V, V_CE,sat = 0.2V.
pnp: BETA_p = 50, V_A_p = 25V, V_EC,sat = 0.2V.

Default MOS transistor parameters: note that LAMBDA depends on L!

NMOS: MU_nC_ox = 50 uAV^-2, LAMBDA_n = [0.1/L]V^-1(L in um) V_T_n = 1V.
PMOS: MU_pC_ox = 25 uAV^-2, LAMBDA_p = [0.1/L]V^-1(L in um) V_T_p = -1V.

Problem #1

BiCMOS Transresistance Amplifier [22 points]



(a) [4 pts.] Draw the two-port small-signal model for this two-stage amplifier, with the small-signal source (and R_S) and the load resistor R_L attached. Your model should show the cascaded models for each stage; there is no need to substitute the expressions for the input and output resistances and gain elements for each stage.

(b) [4 pts.] Find the numerical value of the input resistance of this amplifier, R_in.

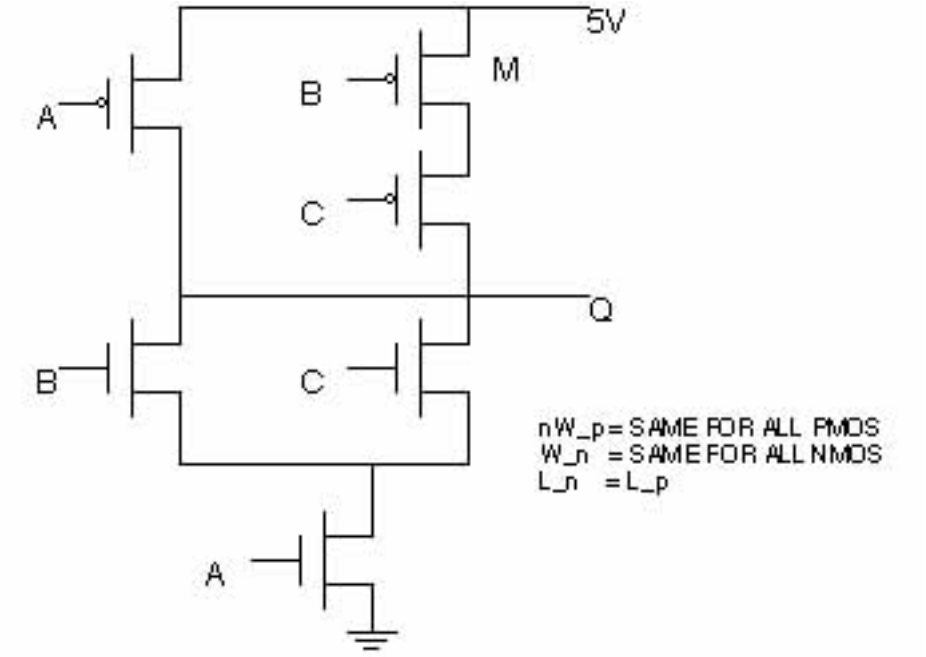
(c) [4 pts.] Find the numerical value of the output resistance of this amplifier, R_out. Your answer need only be correct to within plus or minus 5% for full credit.

(d) [6 pts.] Find the numerical value of the transresistance R_m. Note that R_S = infinity and R_L = infinity for calculating this two-port parameter. Your answer need only be correct to within plus or minus 5% for full credit.

(e) [4 pts.] If the current supplies I_BIAS, i_SUP,1, and i_SUP,2 all need a minimum voltage of 0.5 V across them in order to function, what are the maximum and minimum values of v_OUT? (In other words, find the output swing of the transresistance amplifier.)

Problem #2

Static CMOS Logic Gate [18 points]



(a) [5 pts.] What is the logic operation performed by the above circuit? In other words, what is the logical expression for Q in terms of the three inputs, A, B, and C? Note: you can use a truth table to answer this question.

(b) [4 pts.] We would like to have the worst case low-to-high and high-to-low propagation delays to be equal. Find the required relationship between the width-to-length ratio (W/L)_n of the NMOS transistor and the width-to-length ratio (W/L)_p of the PMOS transistors.

(c) [5 pts.] This logic gate has no load capacitance or wire capacitance (it does have parasitic drain-to-bulk capacitances, however.) Find the channel length transistors L_p = L_n so that the worst case low-to-high propagation delay t_PLH = 10^-11s = 100ps.

Given: MU_p = 100 cm^2/Vs, C_ox = 2.5 fF/um^2, and the drain-to-bulk capacitance of each transistor is C_DB = (1/3) C_ox W L.

If you couldn't solve part (b), you can assume that (W/L)_p = 2.5(W/L)_n for this part (not the correct answer to (b), of course.)

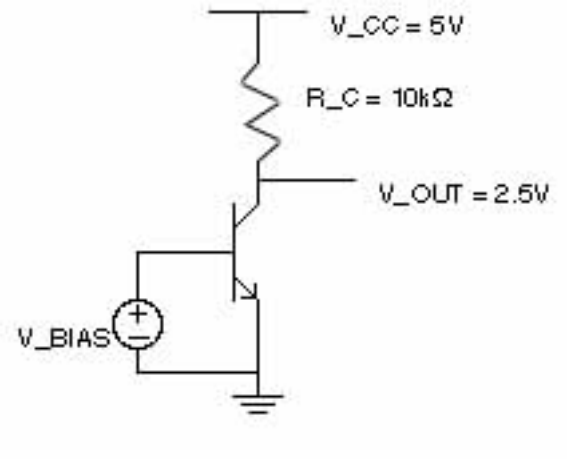
(d) [4 pts.] Find the ratio of the **best case** propagation delays.

t_PHL/t_PLH

If you couldn't solve (b), you can assume that (W/L)_p = 2.5 (W/L)_n for this part (not the correct answer to (b), of course.)

Problem #3

Bipolar Transistor Physics [10 points]



Note: the default npn transistor parameters **do not apply to this problem!**

Given:

N_dE = 10^18cm^-3,
N_aB = 5 X 10^16cm^-3,
N_dC = 4 X 10^15cm^-3.

The base and emitter widths are W_B = W_E = 0.25 um. The area of the emitter-base junction is A_E = 1000 um^2 and the area of the base-collector junction is A_C = 3000 um^2. The electron diffusion coefficient in the base is D_nB = 10cm^2/s and the hole diffusion coefficient in the emitter is D_pE = 5cm^2/s. The charge on an electron is q = 1.6 x 10^-19C.

(a) [5 pts.] For the bias condition where V_OUT = 2.5V, sketch the minority carrier concentration in the base on the graph below. Label the numerical value of n_pB (x = 0).

(b) [5 pts.] Find the numerical value for the bias voltage V_BIAS for which the bipolar transistor just enters saturation (V_OUT = 0.2V).

Solutions!
