Microelectronic Devices and Circuits - EECS105
Final Exam
Wednesday, December 9, 1998

Costas J. Spanos

Total: 100 points

MOS Device Data

*MU*n*C*ox = 50 uA/V^2, *MU*p*C*ox = 25 uA/V^2, *V*Tn = -*V*Tp = 1 V,

*LAMBDA*n = *LAMBDA*p = 0.1V^-1 um (i.e. *LAMBDA* is 0.1 V^-1 when *L* = 1 um, and is proportional to 1/*L*),

*C*ox = 2.3 fF/um^2, *C*jn = 0.1 fF/um^2, *C*jp = 0.3 fF/um^2, *C*jswn = 0.5 fF/um,

*C*jswp = 0.35 fF/um, *C*ovn = 0.5 fF/um = *C*ovp

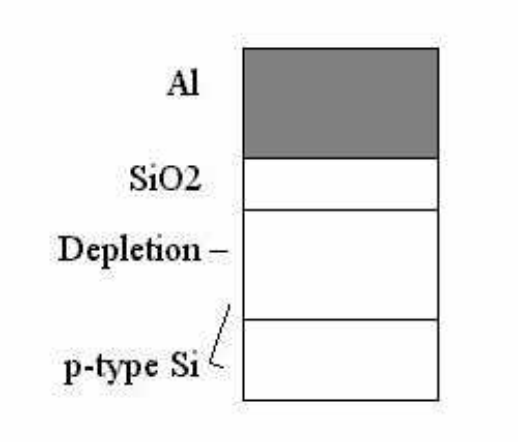
npn Bipolar Device Data

*I*s = 10^-17 A, *BETA* = 100, *V*a = 25 V, *TAU*f = 50 ps, *C*je = 15 fF, *C*mu = 10 fF

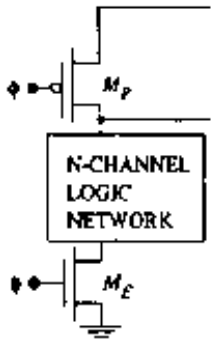
Problem #1 of 4: Answer each question briefly and clearly (3 points each, total 24)

a) What type of electrical current (drift or diffusion?) and what type of carriers (holes or electrons?) flows between the source and the drain of an n-channel MOS transistor?

b) Where is the *maximum* absolute electric field within an MOS capacitor in depletion, made of Al, SiO2, and p-type doped Silicon? (Mark your answer on the graph and give brief explanation)

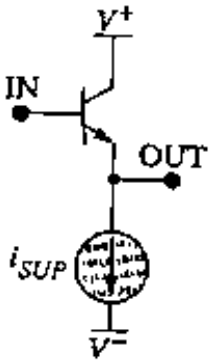


c) What are the noise margins of a dynamic logic gate that employs an n-channel logic network?

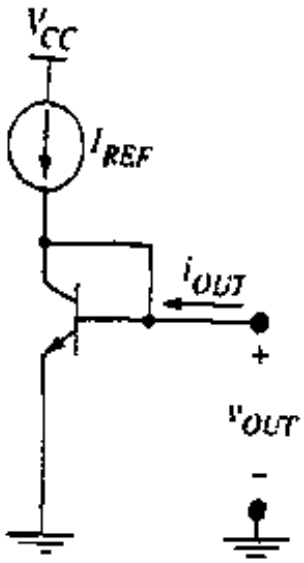


d) What physical aspect of a planar bipolar transistor determines its Early Voltage value?

e) Is it important to build a current supply source with an *extremely* high output resistance when biasing a common collector amplifier? Explain your answer.



f) What can a circuit designer do to adjust the output voltage of the following npn bipolar diode-connected voltage source?



A typical value for this voltage source is about: _____

To reduce this value, the designer must:

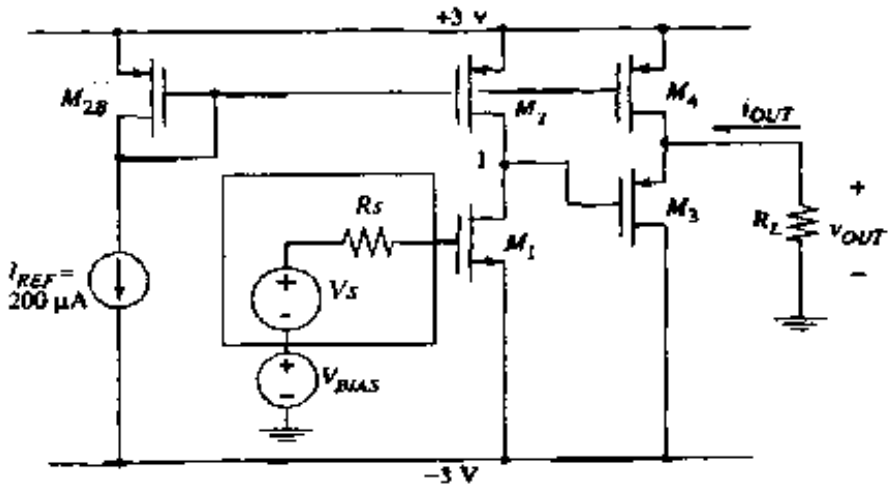
To increase this value, the designer must:

g) What single-stage amplifiers suffer from the so-called "Miller effect" that limits their frequency response?

h) What is the definition of the common-mode rejection ratio of a differential amplifier?

Problem #2 of 4 (26 points)

Below is given a voltage amplifier with *(W/L)*1 = 50/2, *(W/L)*3 = 100/2, and *(W/L)*2B = *(W/L)*2 = *(W/L)*4 = 50/4. Assume that all backgates are shorted to their respective sources. Assume that *V*bias is set such that all devices are operating in their constant current region.



For each of the following questions, make sure that you show the expressions before you plug in the specific values. A correct expression is worth 70% of the credit, even if the numerical calculation is incorrect!

a) Draw thee small signal model for the CS-CD stages, including parasitic capacitances. (5 points)

b) Calculate the following parameters of this two stage (CS-CD) amplifier:

*A*v (i.e. unloaded DC voltage gain of the entire amplifier), *R*in and *R*out. Also calculate the DC voltage gain *V*out/*V*s when *R*s = 5kOhms and *R*l = 500 Ohms (5 points)

Parameter	Value	Unit
Av		
Rin		
Rout		
Vout/Vs		

c) Find the *OMEGA*3DB for this amplifier using the method of open-circuit time constants. (Hint #1: make sure that you include these parasitic capacitances: *C*gs1, *C*gd1, *C*db1, *C*db2, *C*gd3, *C*gs3, *C*db3 and *C*db4. Hint #2: all these capacitances combine to *five* distinct capacitances, for which you will then have to calculate the open circuit time constants.) Answer this question in the following four steps:

c1) From part (a), combine all these capacitances to the following five, and calculate their values. (3 points)

*C*gs1 =

*C*gd1 =

*C*1 (capacitance between ground and node "1") =

*C*gs3 =

*C*l =

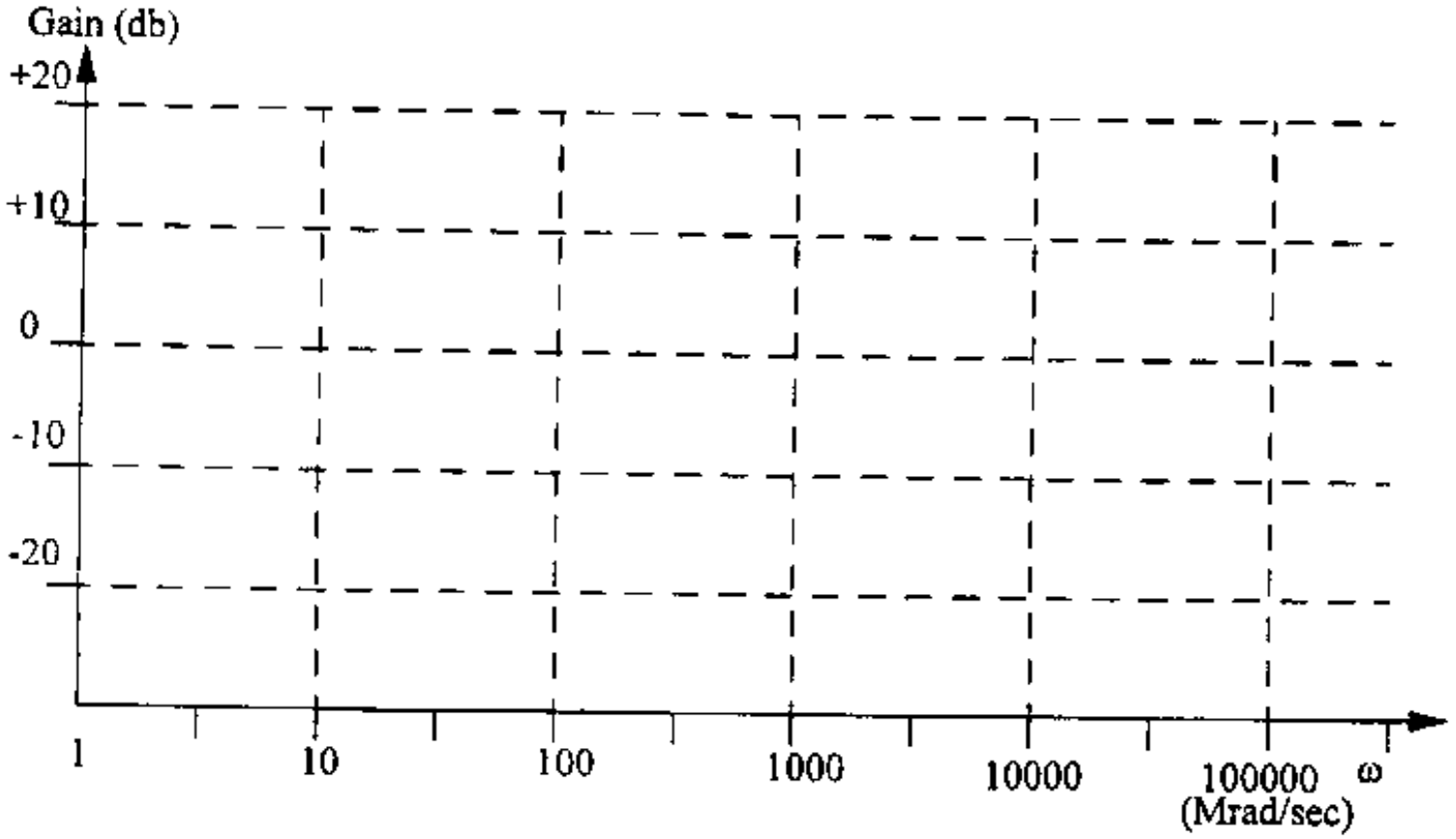
c2) Calculate the resistance "seen" by each of the above capacitances. (2 points)

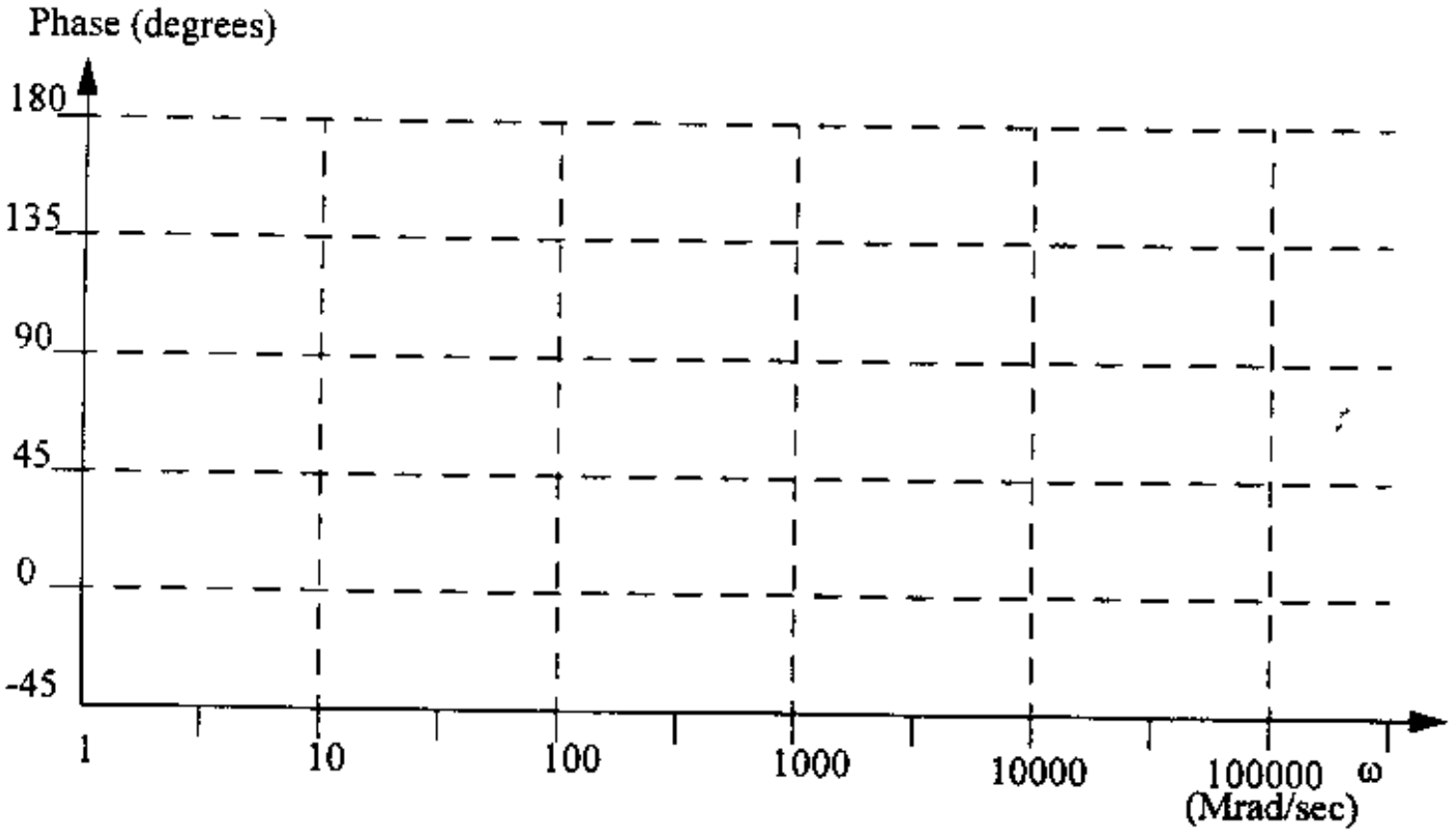
c3) Calculate the dominant pole for the circuit. (1 point)

d) Assuming that, in addition to the dominant pole you found in part (c), this amplifier has a *second* pole at 1000 Mrad/sec, draw the amplitude and phase diagrams. (5 points)

If you could not find the loaded DC voltage gain in (b), assume it is -20 V/V and check here: _____

If you could not find the dominant pole *OMEGA*3db in (c), assume it is 30 Mrad/s and check here: _____


Gain (db)
+20
+10
0
-10
-20
1
10
100
1000
10000
100000
ω
(Mrad/sec)

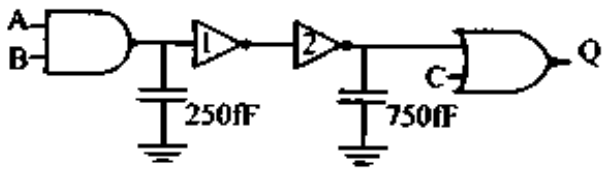

Phase (degrees)
180
135
90
45
0
-45
1
10
100
1000
10000
100000
ω
(Mrad/sec)

e) Quite frankly, this is not a very good amplifier, so go ahead and replace *M*1 with an npn bipolar transistor, redraw the circuit and calculate the new loaded DC voltage gain. (5 points)

Problem #3 of 4 (25 points)

Consider the following static CMOS logic circuit. The two capacitances on the schematic represent the capacitance of the wiring connecting these gates.

For each of the following questions, make sure that you show the expressions before you plug in the specific values. A correct expression is worth 70% of the credit, even if the numerical calculation is incorrect!



a) Write the logical expression for *Q* in terms of *A*, *B* and *C*, and fill out the truth table. (3 points)

Q =

A	B	C	Q
0	0	0	
0	1	0	
1	0	0	
1	1	0	
0	0	1	
0	1	1	
1	0	1	
1	1	1	

b) Re-draw this circuit showing all the transistors that implement the logical functions depicted above in CMOS static logic, using a 5 V supply voltage. (4 points)

c) All transistors have a channel length L = 2um. The widths of the n-channel transistors for the inverters and logic gates are as follows:

NAND gate: Wn = 4 um, Inverter 1: Wn = 6 um, Inverter 2: Wn = 18 um, NOR gate: Wn = 4um.

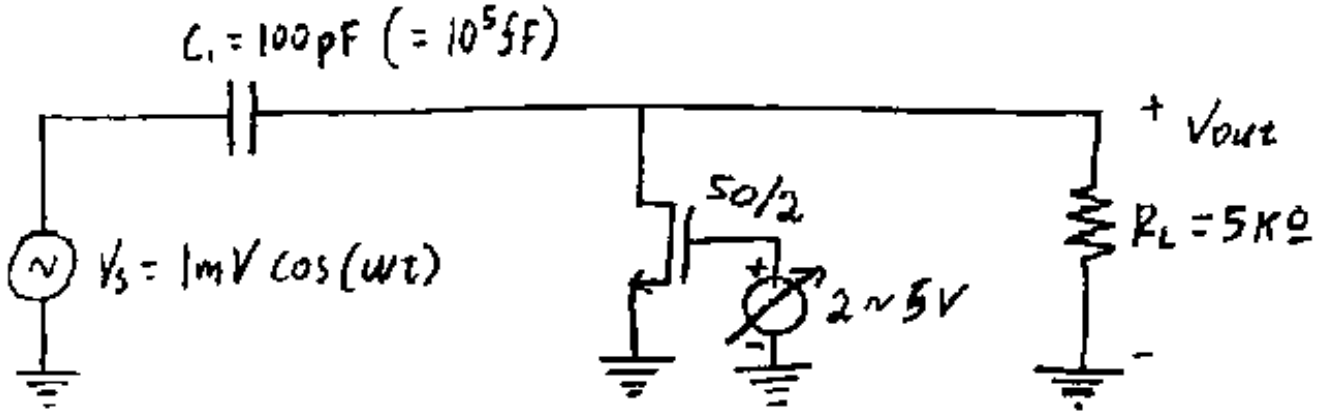
Determine the widths of the p-channel transistors in the circuit such that the inverters have equal propagation delays tPHL = tPLH and that the logic gates have equal worst-case propagation delays. (6 points)

d) Find the numerical value of the worst-case propagation delay tp for the NAND gate. The drain-bulk capacitances can be neglected because of the large wire capacitance. (But do take into account the effect of the gate capacitance through Cox!) (6 points)

e) Find the numerical value of the worst-case propagation delay tp from the input to Inverter 1 to the output of Inverter 2. The drain-bulk capacitance can be neglected because of the large wire capacitance. (Again, do take into account the gate capacitances of the driven gates). (6 points)

Problem #4 of 4 (25 points)

Consider the following circuit. Note that this is NOT a common gate amplifier, since the transistor is only going to be operating in the *triode* region.



a) Note that this transistor is operating in the triode region and is playing the role of a variable resistor. Calculate the sheet resistance of the channel of this transistor, as a function of *V*gs. Do this calculation for *V*gs values of 2, 3 ,and 5 V. (5 points)

V_{GS} (V)	$R_{\square}$ (Ohms/□)
2	
3	
5	

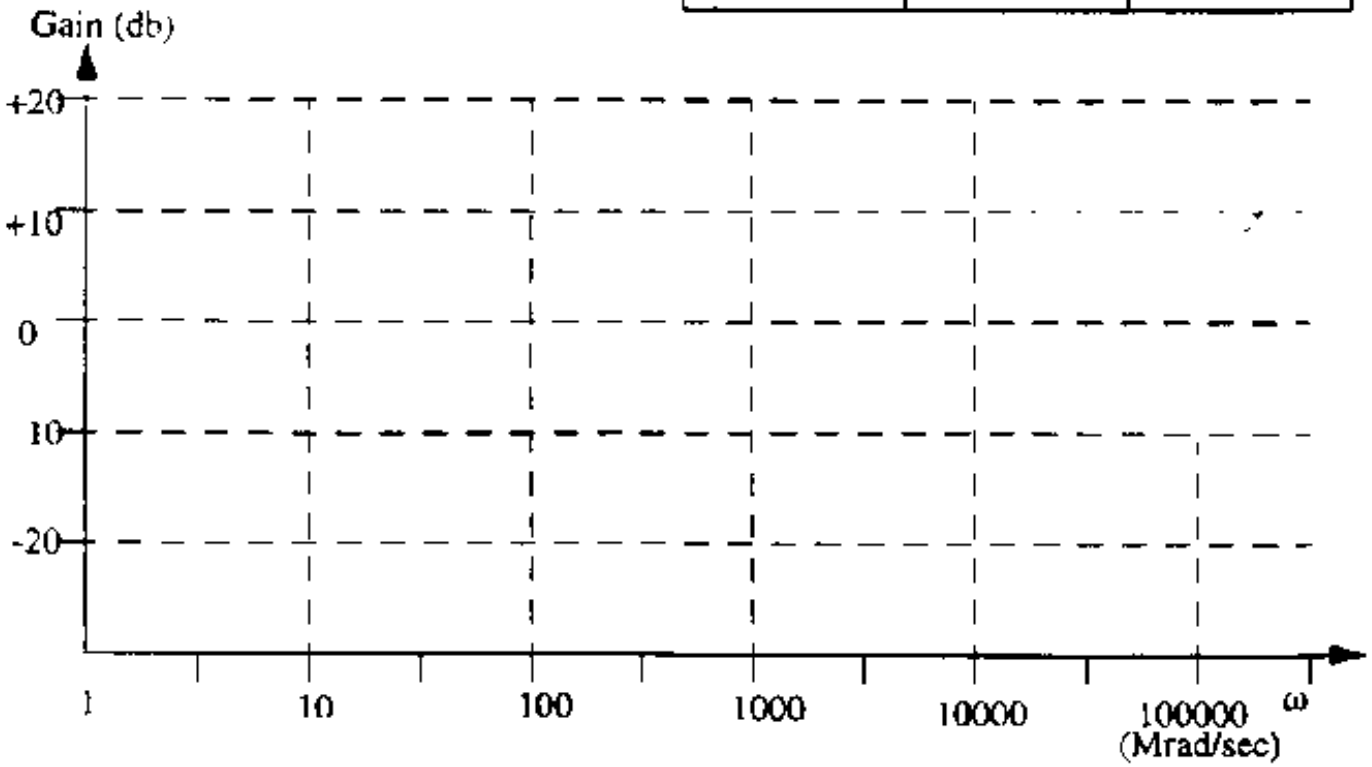
b) Given that the size of this transistor is 50/2, calculate the equivalent small signal channel resistance for its channel. (Hint: the small channel resistance in this case is NOT determined by the *LAMBDA* of the transistor!) (5 points)

Vgs (V)	*Rchannel (Ohms)*
2	
3	
5	

c) Write the small signal model and include and calculate the parastic capacitances. Note that the size of the drain is 10 um long by 50 um wide. Also note that the *C*gd for a transistor in a triode mode is given by the formula *C*gd = *W*L*C*ox/2 + *W*C*ov. (5 points)

d) Calculate the first pole and first zero for this circuit for *V*gs values of 2 and 5 volts and draw the two voltage transfer characteristics versus frequency for each value of *V*gs. (Use the same graph for both plots, but make sure you mark each carefully.) (5 points)

Parameter	Value when $V_{GS} = 2V$	Value when $V_{GS} = 5V$
first zero		
first pole		



e) What amplifier stage would you consider adding between this filter and the load in order to make the frequency response of the entire circuit largely independent of the value of the load? (Note that you have to use a transistor type and an amplifier stage that will not limit the high frequency response of this filter). Draw the new circuit and explain your choice. (5 points)