UNIVERSITY OF CALIFORNIA

College of Engineering
Department of Electrical Engineering
and Computer Sciences

Professor Oldham

Spring 1999

EECS105 — Midterm 1

Thursday, 25 February 1999

Your name: _____ _____
first last

Your discussion TA: ❒ Allan Chang ❒ Lily Tam

- This is a closed book exam, but you may use your page of notes.
- Please do all your work on the pages of this exam. Ask if you need extra paper.
- Full credit will be given only when you indicate the source of your answer, such as a table, graph, or calculation.
- Please write your name in the above space
- Special notes:

1. SOME GRAPHS AND FORMULAS ARE GIVEN AS APPENDICES TO THIS EXAM. BE SURE TO LOOK THESE OVER.

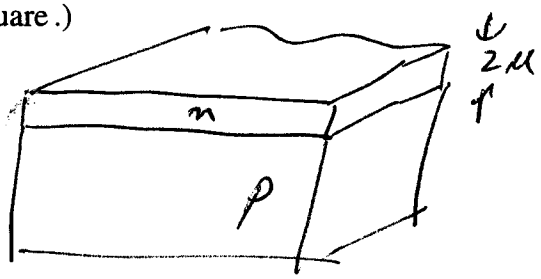
   ☐ Yes, I have looked these over. (Check box)

2. SOME PARTS OF THE EXAM ARE GRADED WITH NO PARTIAL CREDIT. They are noted. You may wish to double check your answers on those parts.
3. ONCE IN A WHILE SOME EXTRA CREDIT IS POSSIBLE FOR CLEVER INSIGHT. Again, these places are noted. But we will not answer questions about these problems. Just be very clear in your work.

	SCORE
Problem 1 (20 pts.)	
Problem 2 (25 pts.)	
Problem 3 (30 pts.)	
Problem 4 (25 pts.)	
TOTAL (100 pts.)	

Problem 1 (20 pts.)

a. [No partial credit] In a certain process, a 2μm thick layer of n-type silicon (doping = $2 \times 10^{15}/cm^3$ is created over a p-type substrate. It is to be used for the purpose of making integrated circuit resistors. What is the sheet resistance of this layer? (Units must be Ω/square.)



$R_\square = \rho/t = \frac{1}{q\mu_n n t} \quad t = 2\times10^{-4}$

(FROM PLOT ~1350)

$= 11.6 K\Omega$

11.6KΩ

b. Using the layers of (a), above, you need to make a resistor with value of $200K\Omega$. It is 5μm wide. What must its length be (ignoring contact effects)?

$R = \left(\frac{W}{L}\right)^{-1} R_\square \qquad \frac{L}{W} = \frac{200K}{11.6K} = 17.25$

$L = W \times 17.25$

86 μm

c. Someone properly points out to you that the layer in part a), though it is physically 2μm thick, is electrically somewhat thinner, because there must be a depletion layer at the n-p interface. (You are to ignore this in part a.) Suppose the doping in the p region is also $2 \times 10^{15}/cm^3$ (but acceptors instead of donors). At zero applied voltage between the n and p regions (i.e., in thermal equilibrium), just what is the net electrical thickness of the n-region? (Thickness minus depleted portion.)

$X_{d_n} = \sqrt{\frac{2\epsilon V}{qN_A}} \leftarrow \phi_B/2 = .32V$

(BECAUSE THE JUNCTION IS SYMMETRIC)

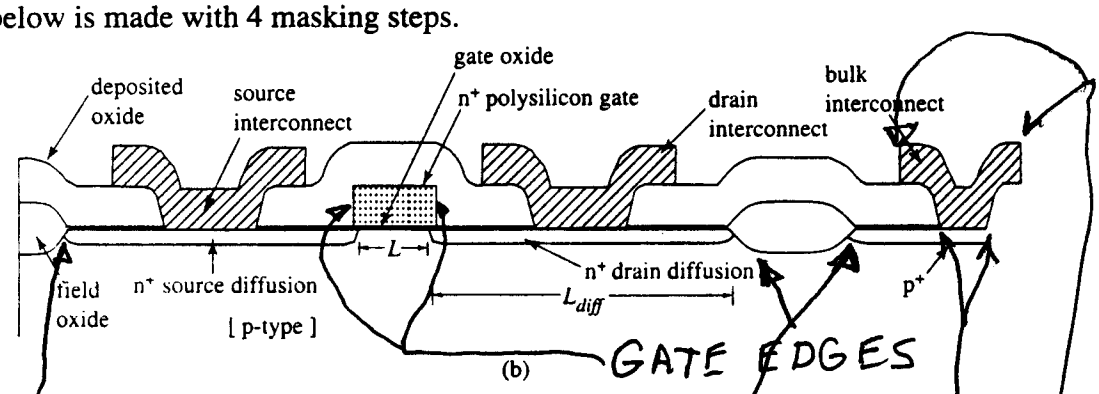
$= 0.45\mu m$

$2 - 0.45$ (μm)

$= 1.55\mu m$

Problem 2 (25 points)

The structure below is made with 4 masking steps.



Four-mask layout and cross section of an integrated n-channel MOSFET.

a. Name the masks (use the terminology within the figure in the names, if possible).

(1) FIELD OXIDE/ACTIVE AREA MASK
(2) GATE MASK
(3) CONTACT MASK
(4) METAL/INTERCONNECT MASK

b. For each mask name point to two edges in the cross-section which come about as a result of the application of that mask (photolithography and etching.) The gate edges are identified as an example.

c. If this structure represents the n-mos transistor in my 450MHz pentium processor (made with a so-called "quarter-micron process," can you give me approximate values for the size of the following:

c.1) L		~0,25μm
c.2) L_{diff}	(½μm to 2μm)	~1μm
c.3) gate oxide thickness	(5nm to 40nm)	~20nm
c.4) metal thickness	(200 to 1000nm)	~½μm
c.5) n^+ layer thickness	(20 to 200nm)	~50nm

d. Why is L_{diff} so much bigger than L? Is this not wasted space? [Extra credit possible]

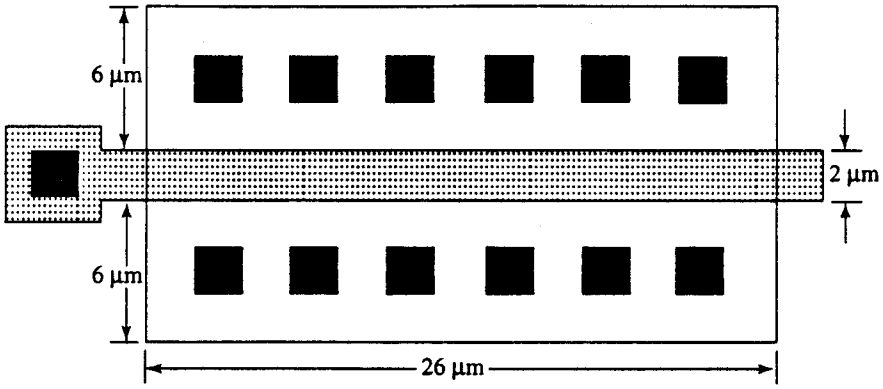
CONTACT - GATE SPACING REQUIRED (DESIGN RULE)
CONTACT - N+ SPACING REQUIRED (" ")
CONTACT SIZE

e. If this is an n-channel MOS transistor, what is the purpose of the p^+ region?

SUBSTRATE CONTACT

Problem 3 (30 points)

An MOS structure is made with the layout



$\frac{W}{L} = \frac{26}{2}$

The cross-section is the same as the left-hand part of the figure in Prob. 2.

The substrate is doped $2 \times 10^{15}/\text{cm}^3$ with acceptors and the gate oxide is 40nm thick.

a. [No partial credit] What is the flat-band voltage V_{FB}?

ϕ n+ → 0.55 } 0.85
ϕ P → −.32 }

-0.87 V

b. [No partial credit] What is the capacitance of the gate to substrate for $V_{SB} = 0$ and $V_{GS} < V_{FB}$? (Ignore overlap and other second order effects.)

ACCUMULATION

$$\frac{A\,\epsilon_{ox}}{t_{ox}} = \frac{2 \times 26 \times 10^{-8} \times 3.9 \times 8.854 \times 10^{-14}}{40 \times 10^{-7}}$$

0.045 (pF)

c. What is the Threshold voltage V_{Tn}?

$$V_T = V_{FB} - 2\phi_p + \frac{\sqrt{2\epsilon_{si}(-2\phi_p)qN_A}}{C_{ox}}$$

$-.87$ $+.636$ $.238$

$+.006$ V

d. Now we adjust the flat-band voltage (and thus the threshold voltage) with an ion implant just at the bottom of the gate oxide. We set the implant value to get a final threshold V_{Tn} of 0.5 V. In testing the device we short source to body, i.e., $V_{SB} = 0$.

d.1) [No partial credit] What is V_{DSAT} of this device if we set $V_{GS} = 2$ V?

$V_{DSAT} = V_{GS} - V_T = 1.5V$

1.5V

d.2) Neatly sketch the I-V characteristics on the linear axes below for three cases: $V_{GS} = 0.5$ V, $V_{GS} = 1$ V, and $V_{GS} = 2$ V. Cover the range $V_{DS} = 0$ to 5 V. Assume the electron mobility in the channel is 500 $cm^2/Vsec$. You must put a scale on the current axis. (Note that partial credit will only be possible if you very carefully show your work, including giving any formulas you are using before evaluation.)

$I_{DSAT}(1V) = \mu C_{ox} \frac{W}{L} \frac{1}{2} (V_{GS} - V_T)^2 = 7 \times 10^{-5} = .07mA$

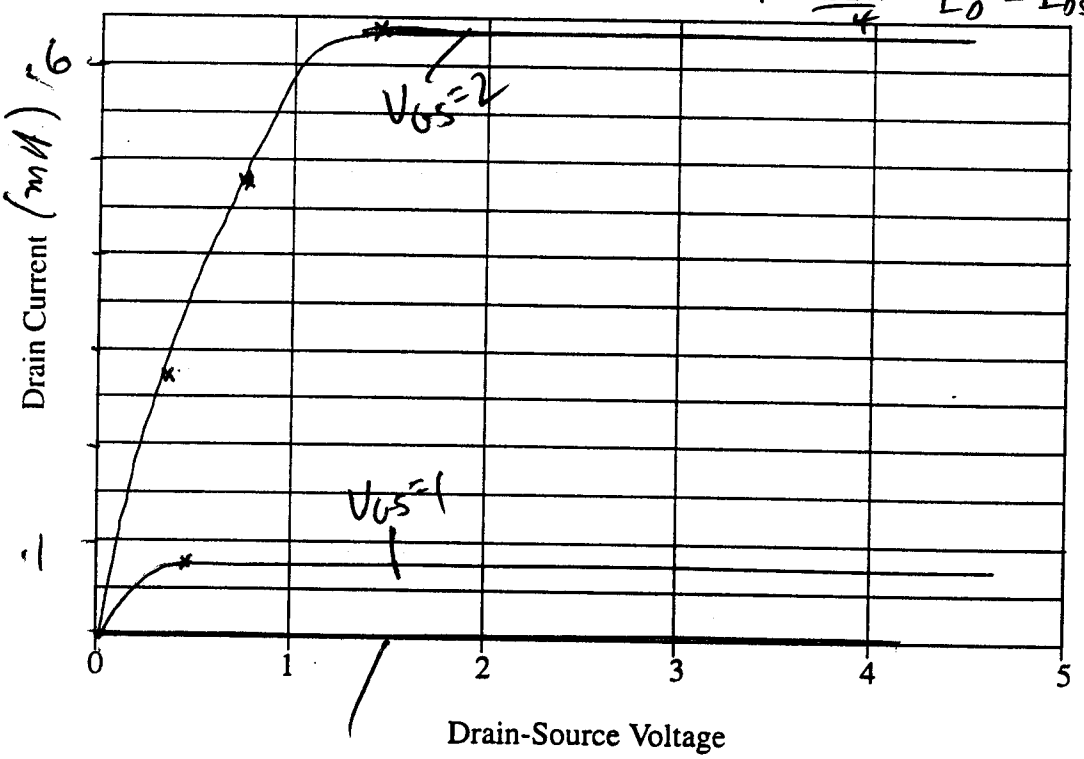
500 $\frac{\epsilon_{ox}}{t_{ox}} = 8.6 \times 10^{-8}$

$I_{DSAT}(2V) = I_{DSAT}(1V) \times \left(\frac{1.5}{.5}\right)^2 = 6.3 \times 10^{-4} = .63mA$

Note at $\frac{V_{DSAT}}{2}$ $I_D = I_{DSAT} \times .75$

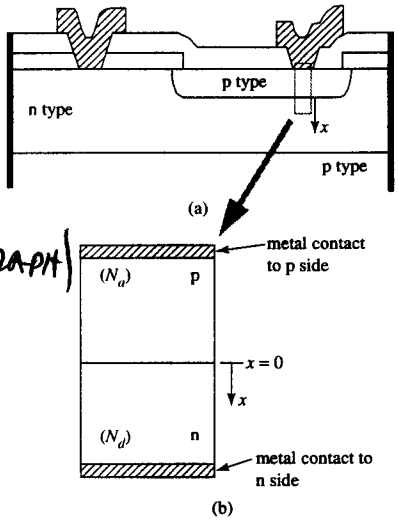
at $\frac{V_{DSAT}}{4}$ $I_D = I_{DSAT} \times \frac{7}{16}$

Drain Current vs VDS



Problem 4 (25 points)

A p-n junction capacitor is made in an integrated circuit with the cross-section as shown below. The p-region is very heavily doped compared to the n-region (it is a p^+n junction) and the n-region doping is $1 \times 10^{14}/cm^3$. The junction area is $100 \times 200\mu m$, or $2 \times 10^{-4}\ cm^2$.



$\phi_p = -.55$ (SEE ϕ vs n, p GRAPH)

$\phi_n = .06 \times 4 = .24$

$\phi_{BI} = .79$

a) Make a sketch of the charge density ρ (C/cm^3), the electric field E (V/cm), and the potential ϕ versus x for this structure at 5V reverse bias. The "graph paper" is provided on the page opposite. As part of the calculation to prepare these graphs, please compute the following:

a.1) The built in voltage

0.79 (V)

a.2) The depletion width at 5V reverse bias

$$x_d = \sqrt{\frac{2\epsilon \times (\phi_{BI} + 5)}{qN_D}}$$

8.65 (μm)

a.3) The peak electric field at 5V reverse bias

$$\frac{Q}{\epsilon_{Si}} = \frac{qN_D x_d}{8.85 \times 10^{-14} \times 11.7}$$

13.3×10^3 (V/cm)

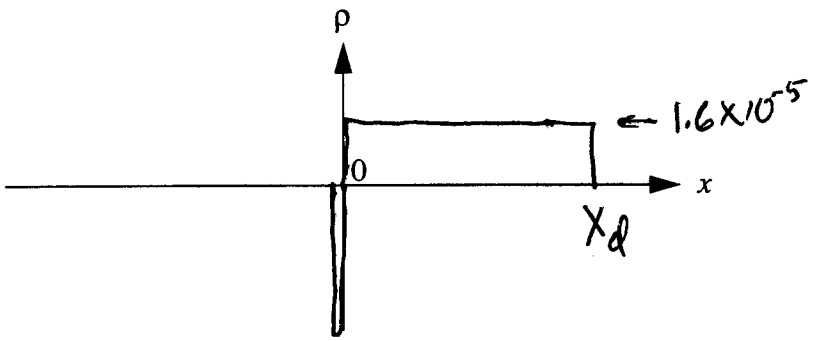
b) What is the small-signal capacitance at 5V reverse bias?

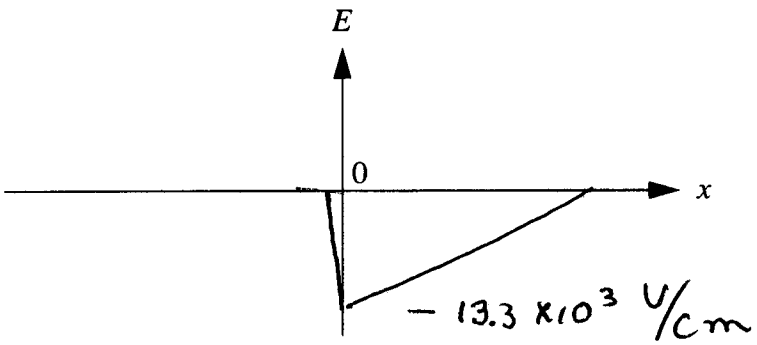
$$\frac{A\epsilon_{Si}}{x_d} \quad \frac{10^{-12}}{8.5 \times 10^{-4}} \quad 2 \times 10^{-4}$$

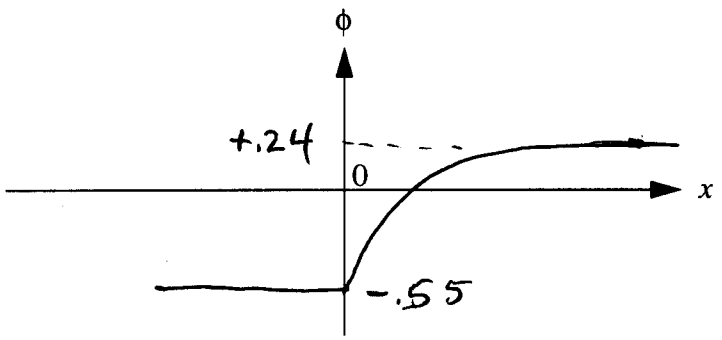
Formula (in terms of known quantities) $A\epsilon_{Si}/x_d$ F

Value 0.235 pF

Prob. 4 (cont.)







c) The n-region ends in an ohmic contact at x = 15μm. Taking into account the answer to part a.2, calculate the current at 0.7V forward bias.

BUT $W_B = 15 - X_B$ (0.7V FWD BIAS)

c.1) First give the formula for the current in terms of doping, geometry, etc. (All must be known quantities.)

$I = A \cdot qD_p p_{no} e^{V/V_{th}} / W_B$ ← A

c.2) List the values of all the quantities in the formula above

2×10^{-4} | 1.6×10^{-19} | $.026\times500$ | $10^6 \times e^{.7/.026}$ | $15 - X_B$ (1.06) $\times10^{-4}$

c.3) Evaluate the current

$X_B = \sqrt{\frac{2\epsilon \times (.79-.7)}{qN_B}} \simeq 1.06\mu m$

0.15 μA

ie 150,000 μA