EE 105, Spring 1998
Midterm #2
Professor R.T. Howe

(Note: Greek letters are in caps, "micro" is represented by a 'u'.)

Default bipolar transistor parameters:

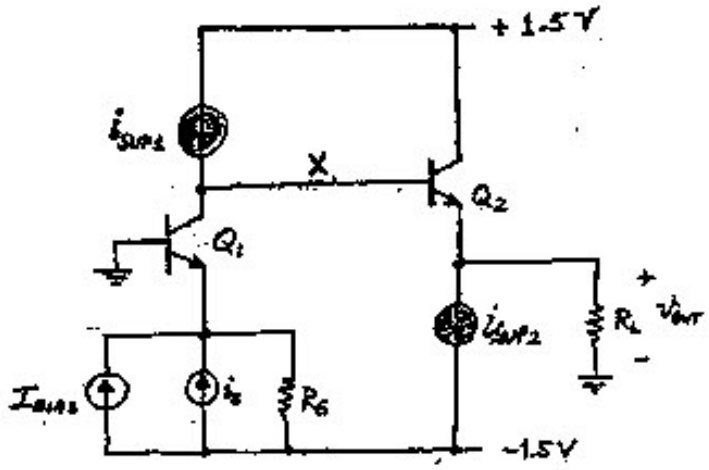
npn: $BETA_o$ = 100, V_{An} = 50 V, $V_{BE,\,oh}$ = 0.7 V, $V_{CE,\,sat}$ = 0.2 V, V_{th} = 25 mV.

Default MOS transistor parameters: note that LAMBDA depends on L!

NMOS: u_nC_{ox} = 50 uAV^-2, $LAMBDA_n$ = [0.1/L] V^-1 (L in um), V_{Tn} = 1V, C_{ox} = 2 fF/um^2, C_{Jn} = 0.1fF/um^2, C_{JSWn} = 0.5fF/um.

PMOS: u_pC_{ox} = 50 uAV^-2, $LAMBDA_p$ = [0.1/L] V^-1 (L in um), V_{Tp} = -1V, C_{ox} = 2 fF/um^2, C_{Jp} = 0.1fF/um^2, C_{JSWp} = 0.5fF/um.

Problem #1 : Bipolar Transresistance Amplifier [20 points]



Given:
ISUP1 = 200uA; ROC1 = 750kOMEGA
VSUP1, min = 0.15V, 0.45V

ISUP1 = 100uA; ROC2 = 200kOMEGA
VSUP2, min = 0.3V

IBIAS = -200uA, VOUT = 0V

(a) [2 pts.] Identify the stages of this two-stage transresistance amplifier by labeling the two-ports below with "CE", "CB", or "CC" for common-emitter, common-base, or common-collector. Also, label node "X".

(b) [3 pts.] Find the numerical value of the small-signal input resistance of this amplifier, R_{in}.
Your answer need only be correct to within (+/-)5% for full credit.

(c) [3 pts.] Find the numerical value of the small-signal output resistance of this amplifier, R_{out}.
Your answer need only be correct to within (+/-)5% for full credit.

(d) [5 pts.] Find the numerical value of the "two-port" transresistance R_m of this amplifier (with R_S = infinity and R_L = infinity). *Your answer need only be correct to within (+/-)5% for full credit.*

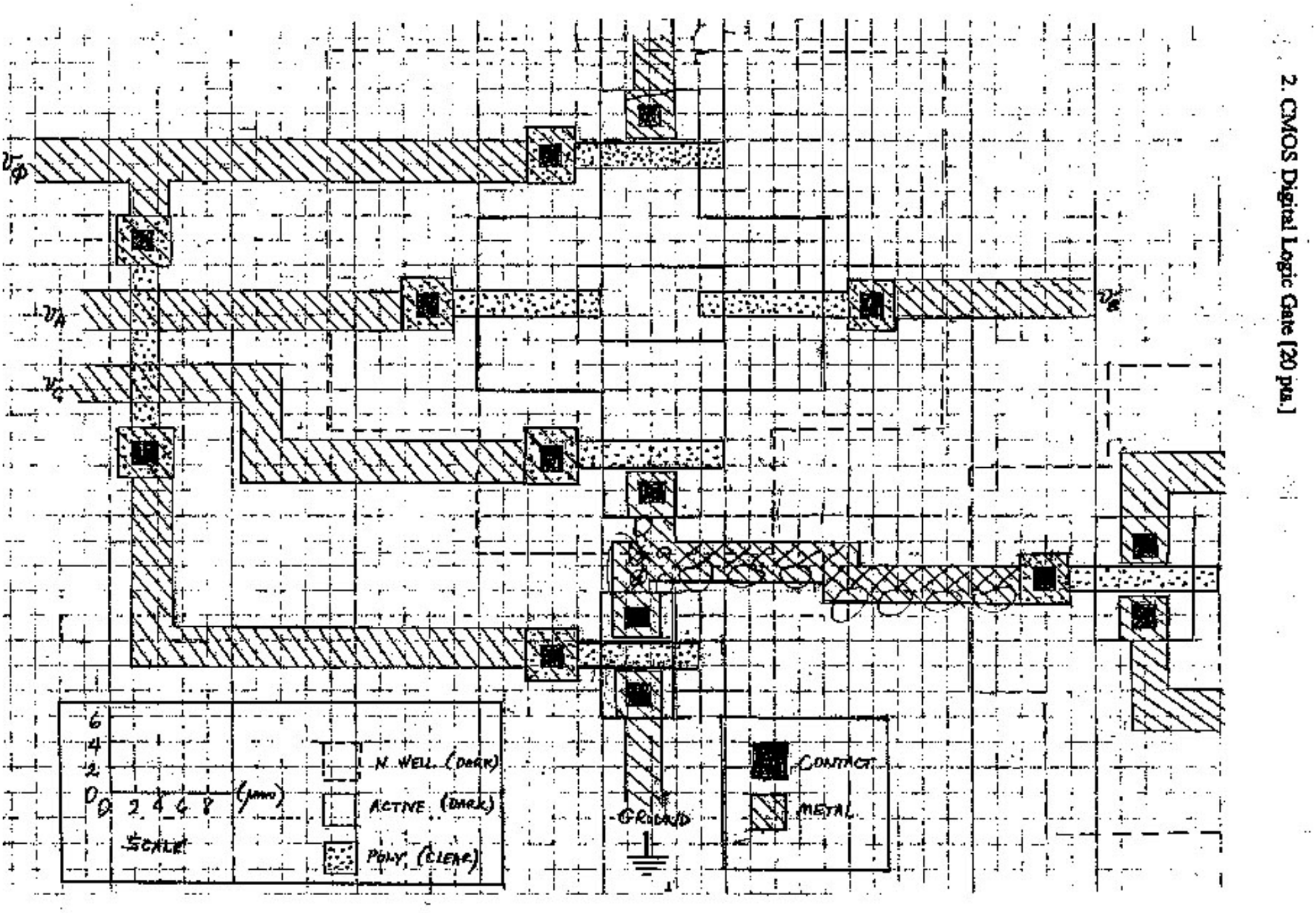
(e) [3 pts.] Find the numerical value of v_{out}/i_S for R_S = 500 OMEGA and R_L = 10 kOMEGA. If you couldn't solve parts (b)-(d), you can assume without loss of credit that R_{in} = 2.2 kOMEGA, R_{out} = 4 kOMEGA, R_m = -185 kOMEGA. Needless to say, these are not the correct answers to (b)-(d).

(f) [2 pts.] Find the numerical value of the minimum output voltage $V_{OUT,\,min}$ of this amplifier.

(g) [2 pts.] Find the numerical value of the maximum output $V_{OUT,\,max}$ of this amplifier.

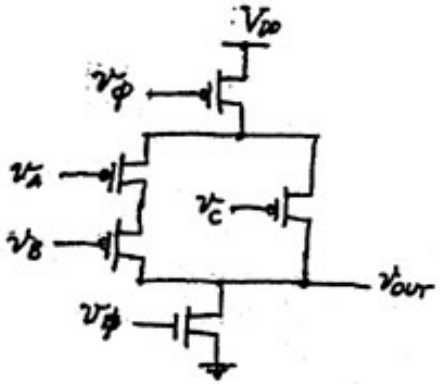
Problem #2 : CMOS Digital Logic Gate [20 pts.]

2. CMOS Digital Logic Gate [20 pts.]



(a) [5 pts.] Draw the schematic for this Logic gate, including the (*W/L*)'s of the transistors in (um/um). Substrate and well contacts are omitted for this simplified layout; you can consider that the "select" mask is the same as the "n well" mask.

(b) [2 pts.] Write the logic function implemented by this logic gate. If you couldn't do part (a), you can use the following circuit instead.



(c) [4 pts.] find the numerical value of C_{db} for this logic gate in fF. You should identify clearly which areas on the layout contribute to C_{db}. Note that you don't need to have done part (a) in order to answer this part; useful device information is located on the cover page of the exam.

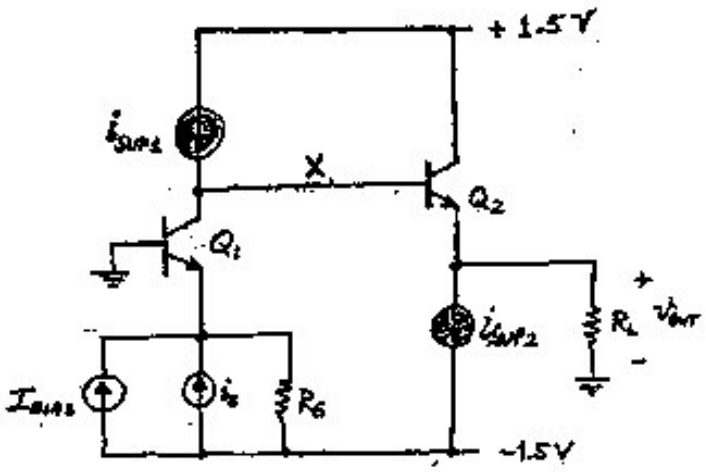
(d) [3 pts.] Find the numerical value of C_w for this logic gate in Ff. Note that you don't need to have done part (a) in order to answer this part. The wiring capacitance per unit area is C_w = 0.1fF/um^2.

(e) [2 pts.] Find the numerical value of C_g for this logic gate in fF. Note that you don't need to have done part (a) in order to answer this part.

(f) [2 pts.] What is the worst-case *charging* current for the load capacitance C_L for this amplifier in uA? If you couldn't do part (a), you can use the substitute logic gate given in part (b).

(g) [2 pts.] What is the worst-case *discharging* current for C_l of this amplifier in uA? If you couldn't do part (a), you can use the substitute logic gate given in part (b).

Problem #3 : Current Sources [10 points]



(a) [4 pts.] Using exactly 4 transistors, draw the circuit schematic of a CMOS current source that will implement i_{SUP} (sourcing current from the positive supply), using I_{REF} as a reference.

(b) [3 pts.] *Given:* I_{REF} = 25 uA and I_{SUP}= 75 uA. If all except one of the transistors have widths W = 10 um and all of the transistors have lengths L = 2 um, find the width of the remaining transistor. There may be more than one correct answer to this part.

(c) [3 pts.] Find the maximum voltage $V_{OUT,\,max}$ for which this current supply will have all of its transistors in operating the constant-current region. If you were unable to solve (b), assume that the width of the PMOS current-source output transistor is W = 100 um.
