EE105 Fall, 1995
Midterm 1
B.E. Boser

Device Parameters: (use in all problems)

	NMOS	PMOS
threshold voltage	0.7V	-0.7V
gate oxide	2fF/um^2	2fF/um^2
mobility	400 cm^2/V-s	150 cm^2 / V-s

Problem #1

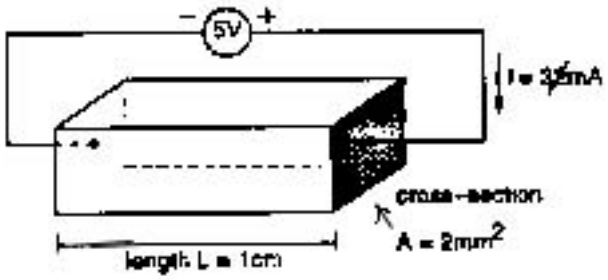
Doped Silicon (20 points)

A sample of Boron doped Silicon is 1 cm long and has cross-section with A=2mm^2

Paramaters: u sub n = 400 cm^2/V-s, u sub p = 150 cm^2 / V-s

(a) [5 points] Is the sample n-type or p-type?

(b) [5 points] If a 5V battery is connected across the Silicon sample, a current of 3mA flows. What is the majority carrier (doping) concentration of the sample?



(c) [5 points] With the voltage source removed, what are the electron and hole concentration in the Silicon sample at room temperature?

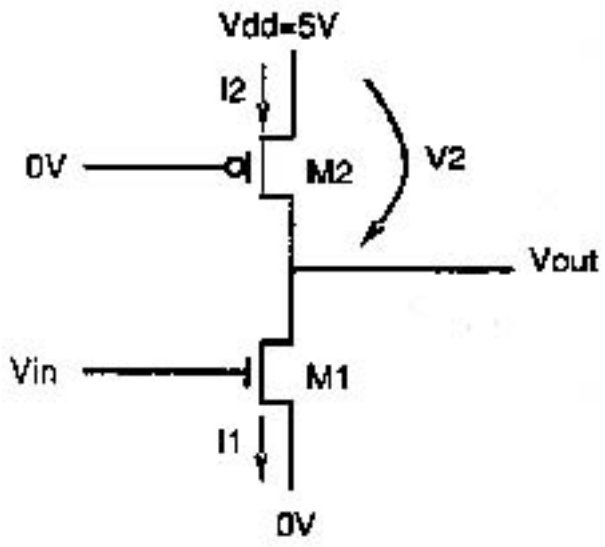
(d) [5 points] What concentration of Arsenic doping is needed to get a current of 100mA when the experiment described in part (b) is repeated?

Problem #2

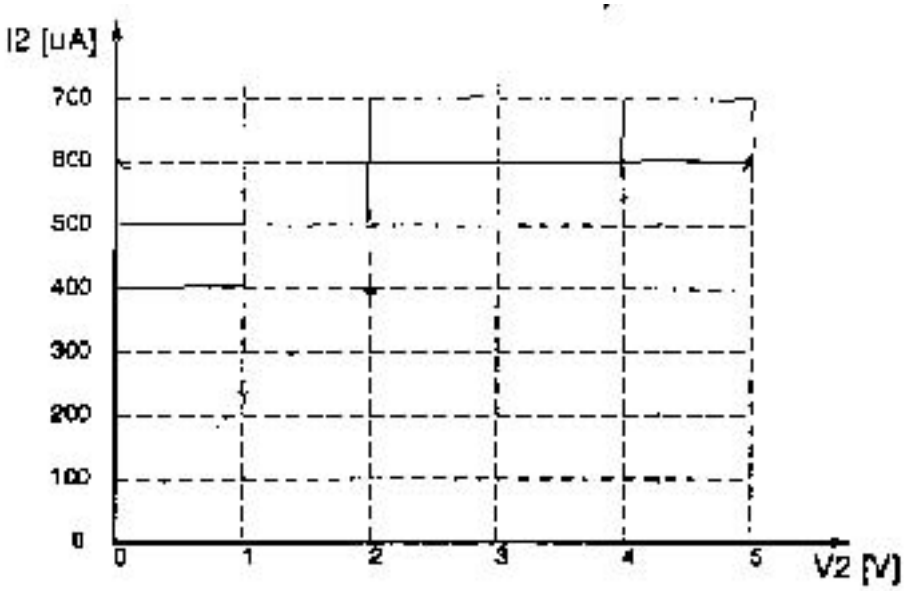
Inverter with PMOS current source load (30 points)

You are a supervisor at SmartLogic Inc. One of your engineers has invented the "new" inverter shown below and proposes to use it in your next project (note that the gate of the PMOS is tied to the ground, rather than the input of the inverter). You are suspicious and first analyze its performance ...

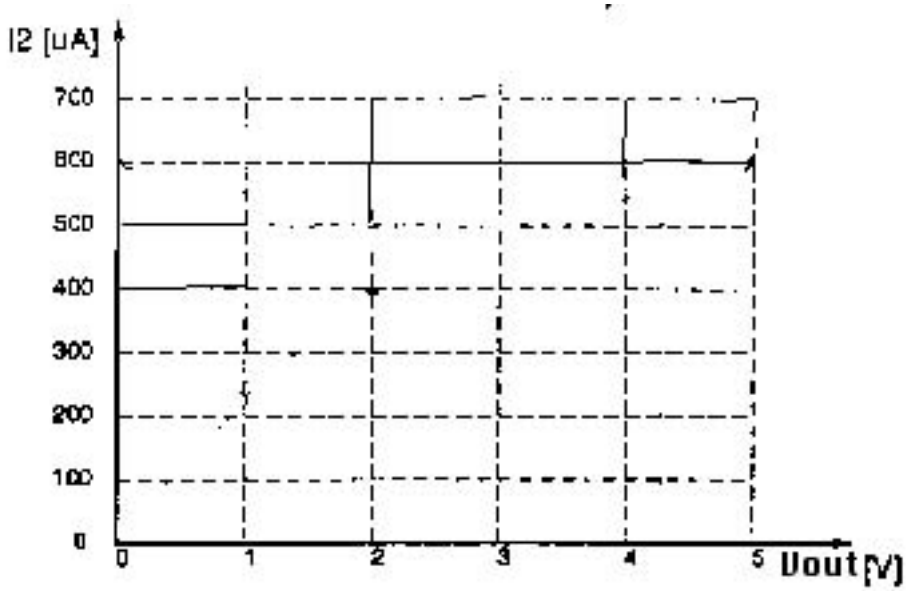
Parameters: V sub DD = 5V, W sub M1 = 4um, W sub M2 = 2um, L sub M2 = 1um



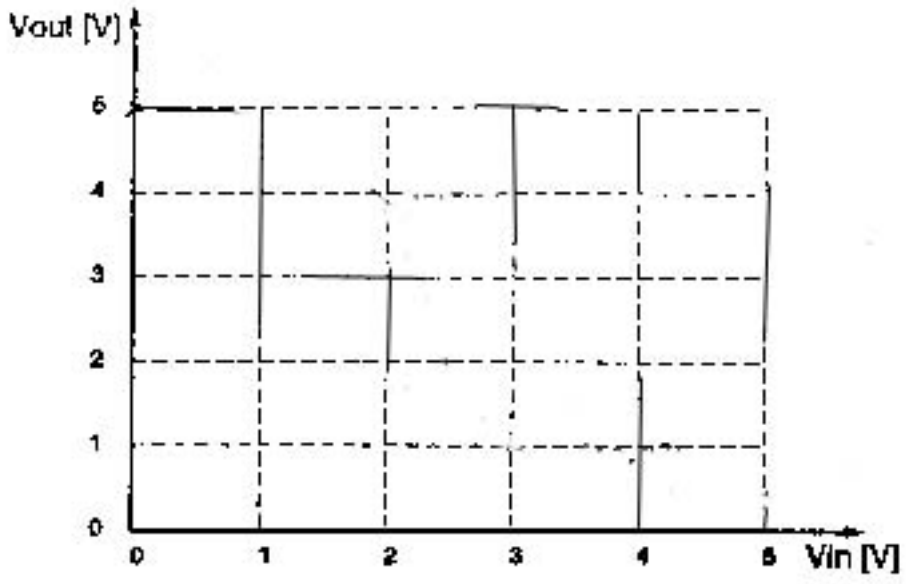
(a) [5 points] On the graph below, sketch carefully, I2 vs V2. Mark the regions of operation (i.e. off, triode, or saturation) and compute the transition points accurately (indicate voltage and current values in graph).



(b) [5 points] On the graph below, sketch carefully, I1 vs Vout for M1 and I2 vs Vout for M2. In the saturation region, the plot should be accurate. Use Vin = 0, 1,2,2.5,3,3.5V. Indicate transition points between different regions of operation in the graph.



(c) [5 points] Using your results from (b), construct graphically the voltage transfer characteristics of the inverter, Vout vs Vin on the graph below. Calculate V-OH and V-OL



(d) [5 points] Calculate the threshold of the inverter.

(e) [5 points] What is the static power dissipation of this inverter when the input voltage Vin is 0V or 5V, respectively?

(f) [5 points] Find the average power dissipation of this inverter driving C-L = 100fF at f-clk = 100 MHz. Ignore "switching power", but include static power dissipation, if any.

Problem #3

NOR gate (25 points)

Paramaters: all device sizes (NMOS and PMOS) L = 1um, W = 5um, VsubDD = 5V

(a) [5 points] Draw the transistor level circuit diagram of a static 3-input NOR gate. Label the inputs, A, B, and C, the output Y, and the supplies, DsubDD and GND.

(b) [5 points] What is the threshold voltage VM of the gate?

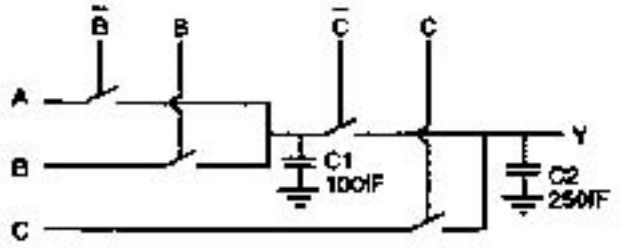
(c) [5 points] Find the input capacitance C-gate for each input.

(d) [5 points] Assuming that the gate drives a load C-L = 200fF, find the worst-case delays t-PLH and t-PHL.

Problem #4

Pass transistor logic (25 points)

Parameter: V-DD = 3V



(a) [7 points] Write the truth table for the gate shown above with inputs A, B, and C, and output Y

(b) [2 points] What logic function does the gate realize?

(c) [4 points] Draw the minimum complexity transistor level implementation for the same logic function using static CMOS gates. What is the minimum number of transistors needed?

(d) [6 points] Find the width W-n and W-p of the NMOS and PMOS transistors of a CMOS transfer gate with R-on = 5kOhms for V-in = V-DD. Assume L-n = L-p = 1um and ignore body effect. Beware: V-DD = 3V

(e) [6 points] Assuming R-on = 5kOhm, find the worst-case propagation delay t-p when input A is switching.
