University of California at Berkeley
College of Engineering
Department of Electrical Engineering
and Computer Sciences

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EECS 105
Final Examination: May 17, 1993

Ground Rules:

- Closed book; three 8½ " x 11" crib sheets (both sides)
- Do all work on exam pages
- Answers within ± 10% of the correct answer will recieve full credit.
- Default bipolar transistor parameters:
  npn: β_n=100, V_{A_n}=100 V, C_π=15pF, C_μ=1pF
  pnp: β_p=50, V_{A_p}=50 V, C_π=30pF, C_μ=2pF
- Default MOS transistor parameters:
  NMOS: $\mu_n C'_{ox}=25\mu A/V^2$, $\lambda_n=0.01\ V^{-1}$, $V_{T_n}=1$ V
  PMOS: $\mu_p C'_{ox}=10\mu A/V^2$, $\lambda_p=0.02\ V^{-1}$, $V_{T_p}=-1$ V

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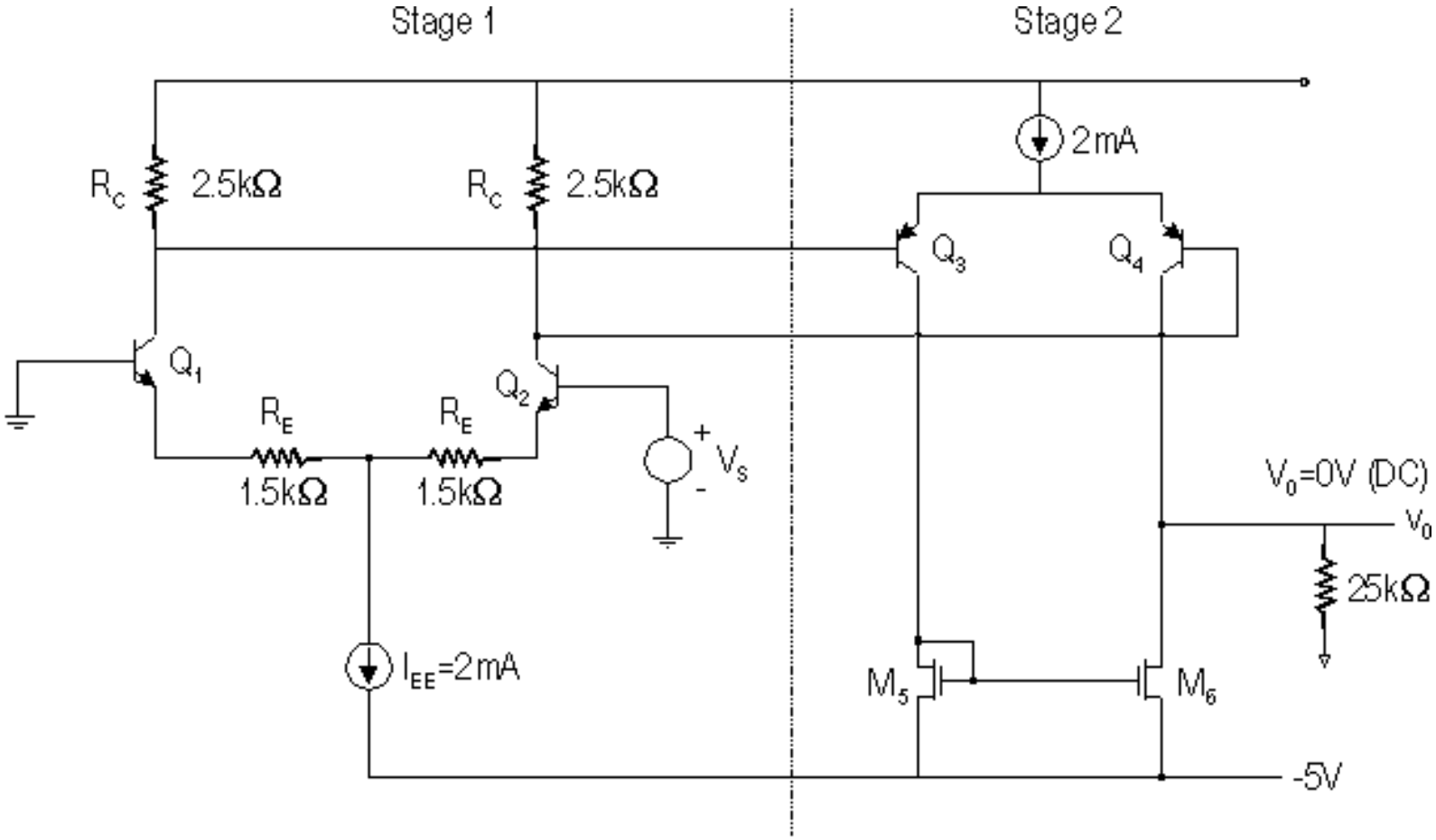
1. Two-Stage BiCMOS Differential Amplifier [20 points]



(a) [2 points] Draw the differential half circuit for *Stage 1*.

(b) [4 points] Draw the differential two-port small-signal model for *Stage 1* and find the numerical values of its parameters.

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(c) [4 points] Draw the differential two-port small-signal model for *Stage 2* and find the numerical values of its parameters.

(d) [4 points] Find the numberical value of the small-signal gain v_o/v_s.

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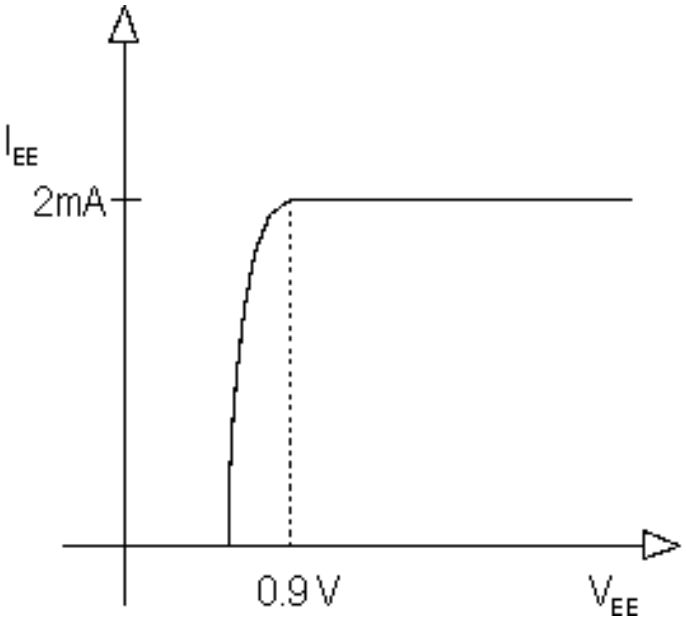
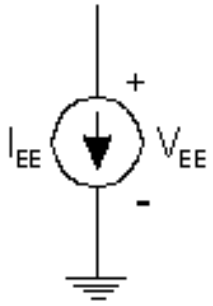
(e) [2 points] What is the maximum DC common-mode input voltage, $V_{CM,max}$, for which all devices are forward active (BJT) or saturated (MOS)?

(f) [2 points] What is the minimum DC common-mode input voltage, $V_{CM,min}$, for wich all devvices are forward active (BJT) or saturated (MOS)?





(g) [2 points] What is the DC power dissipation for this amplifier?

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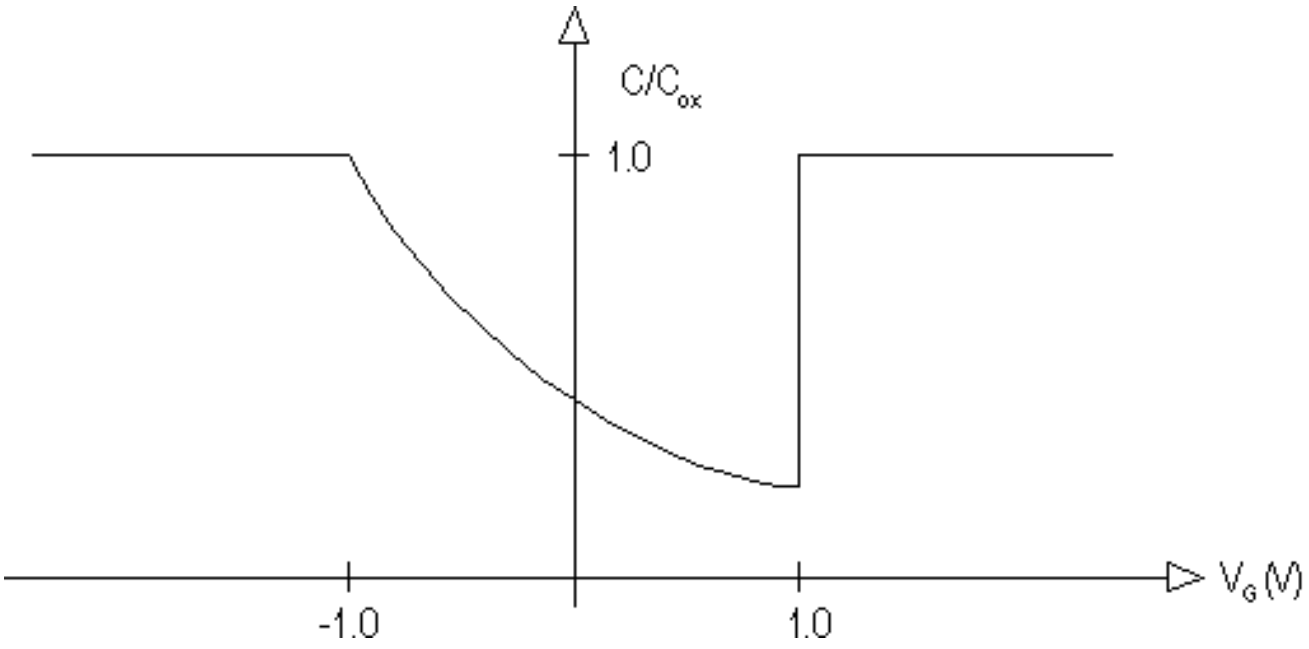
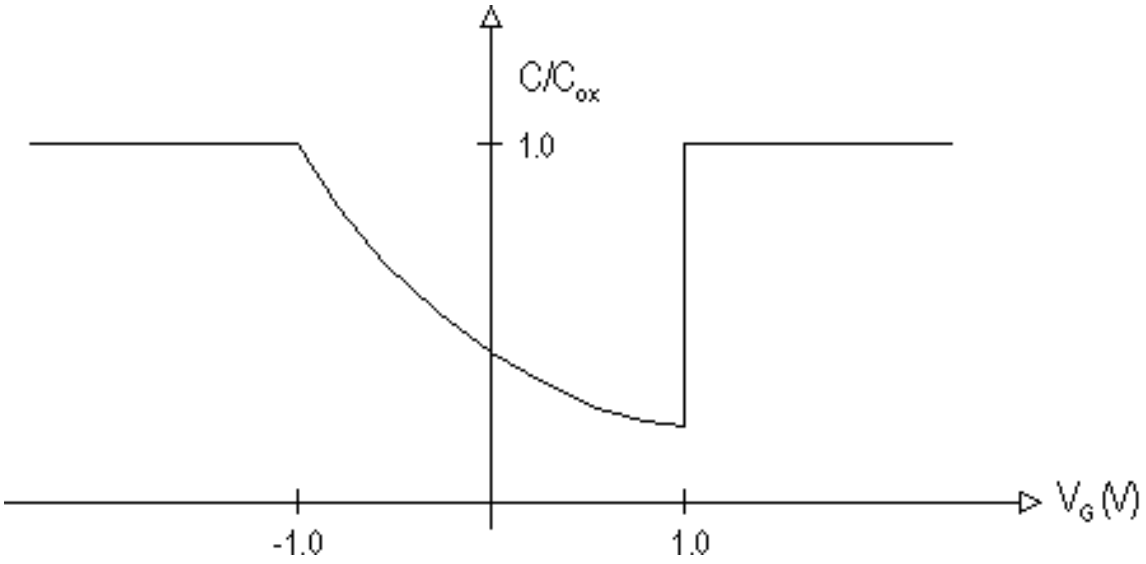
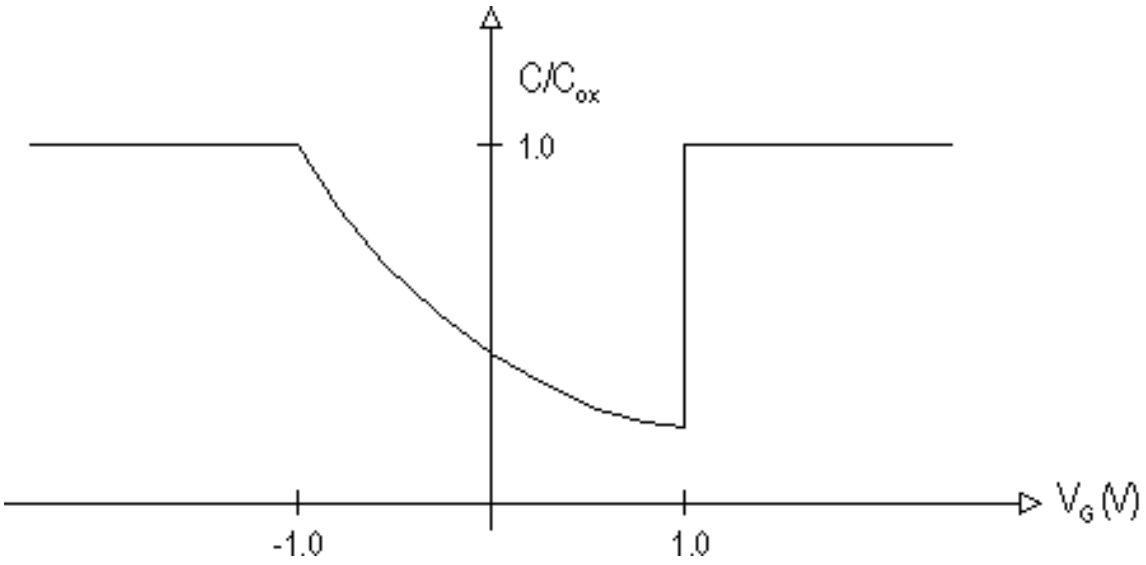
2. Pictorial MOS Electrostatics [20 points]



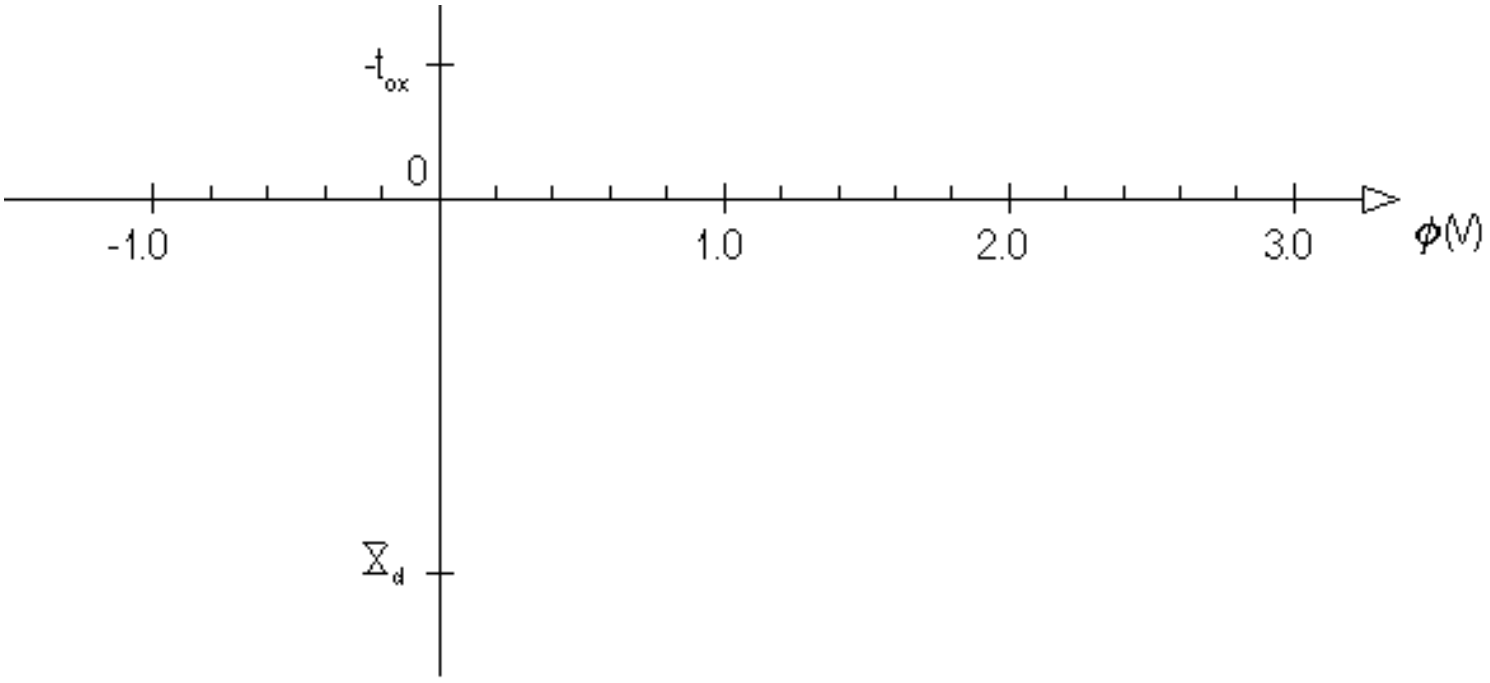
A MOS C-V curve is shown above for an n+ polysilicon gate and a p-type substrate, with N_a=1E-16 cm^{-3}.
(a) [5 points] Sketch below the C-V curve for this structure when the oxide thickness t_{ox} is reduced. Your plot should be *qualitatively correct* -- the original C-V curve is reproduced to make comparison easier.



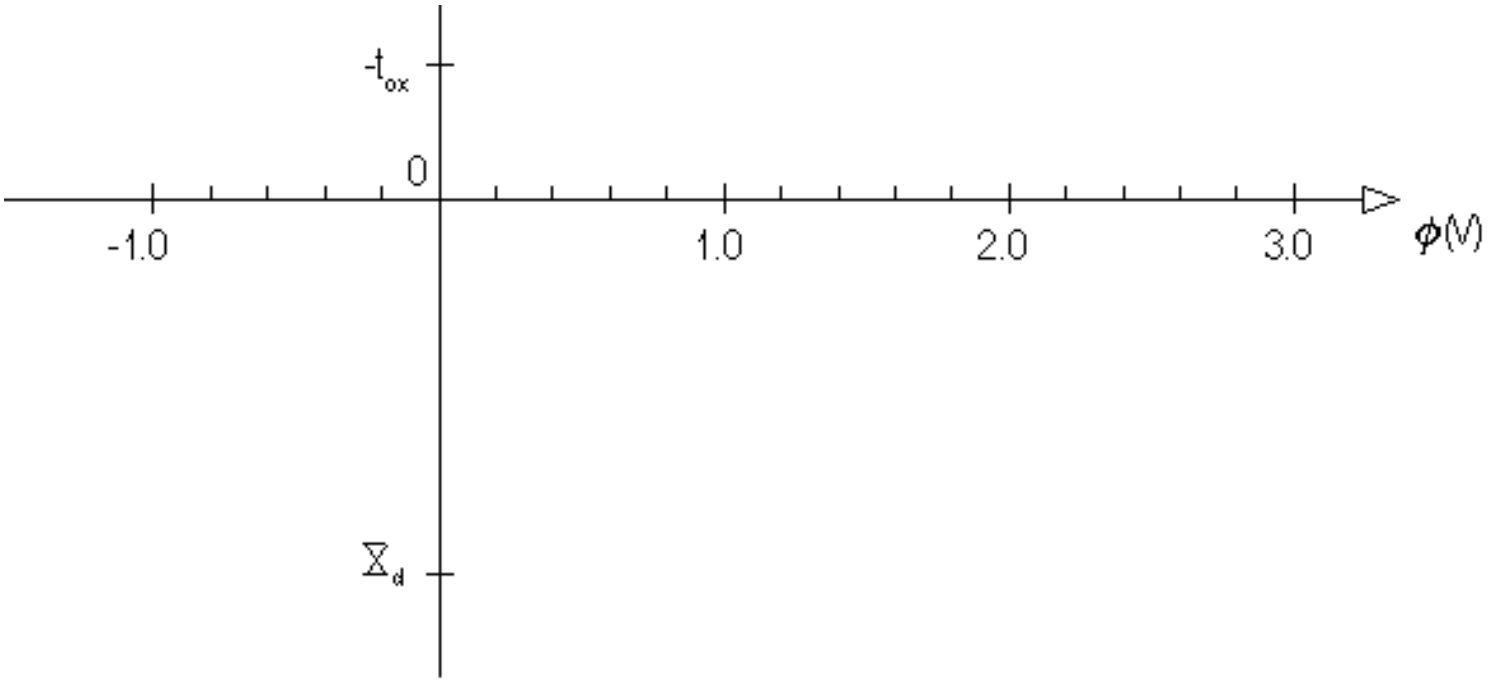
(b) [5 points] Sketch below the C-V curve for the *complemenatary* structure, for which the gate is p+ polysilicon and the substrate is n-type with N_a=1E-16 cm^{-3}. Your plot should be *qualitatively correct* -- the original C-V curve is reproduced to make comparison easier.



(c) [5 points] Sketch the electrostatic potential throught the original structure when it it sin *thermal equilibrium* (V_G=0V). *Given* the polysilicon potential is ϕ_{n+}=0.55 V, surface potential $\phi_s=\phi$(x=0)=0V, x=0 corresponds to the oxide/silicon interface.



(d) [5 points] Sketch the electrostatic potential throught the original structure when V_G=2V



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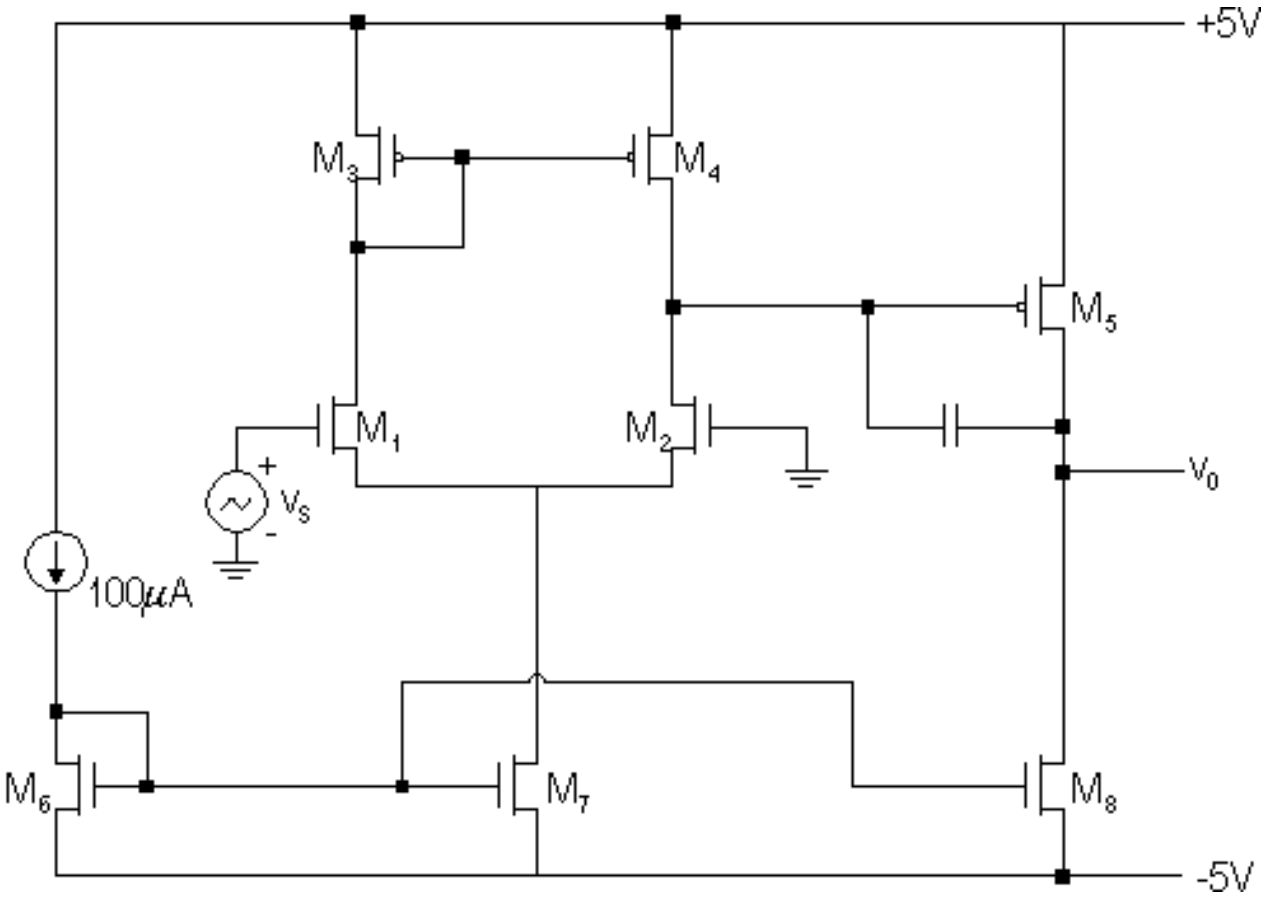
3. MOS Amplifier Frequency Response [20 points]



Given:

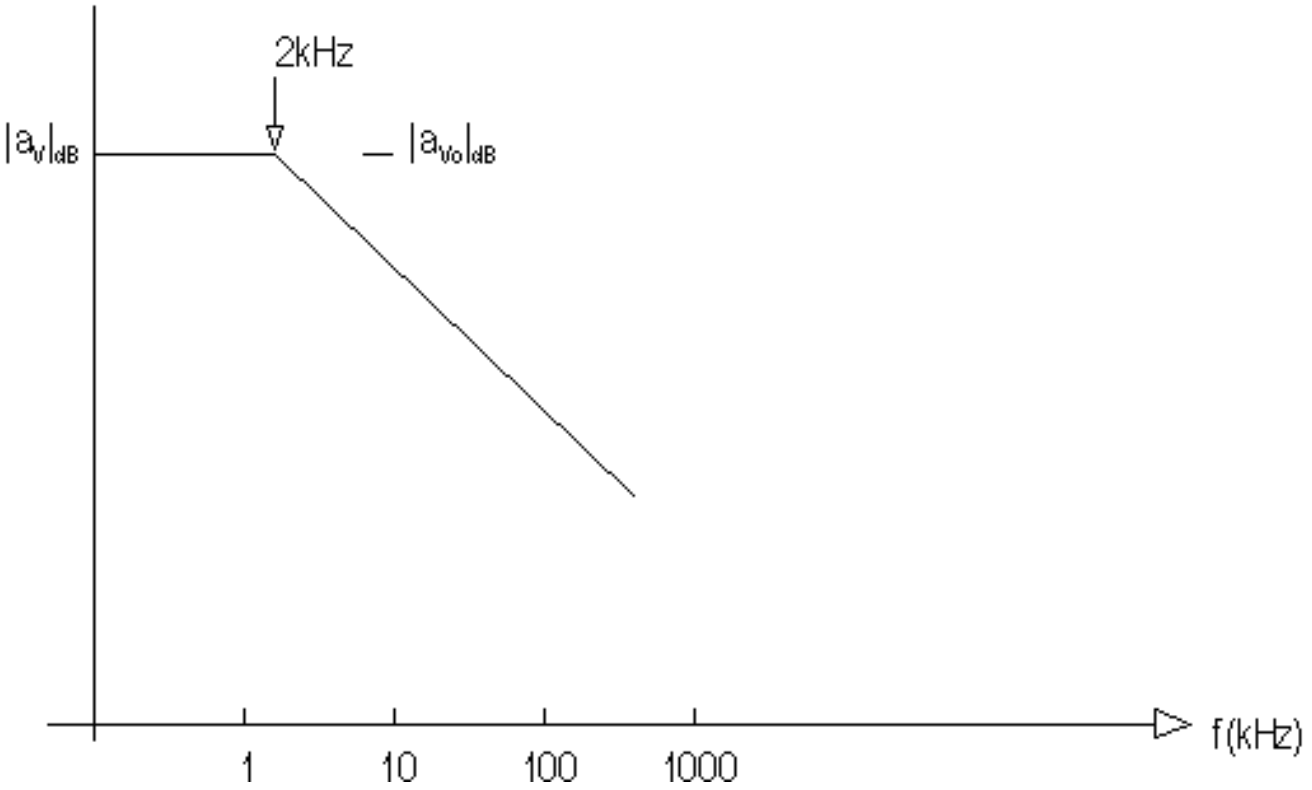
$$\left(\frac{W}{L}\right)_7 = 2\left(\frac{W}{L}\right)_8 = 2\left(\frac{W}{L}\right)_6$$
$$= 20$$

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_3$$
$$= \left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)_5 = 50$$

(a) [4 points] Find the DC voltages at the drain of M_2 and at the source of M_2.

(b) [4 points] Find the small-signal voltage gain $a_{vo}=v_o/v_s$ at low frequencies (consider C_c open).

(c) [4 points] Given that the magnitude (in dB) plot for the voltage gain has a pole at 2kHz (see plot), find the numerical value of C_c. You may assume that any Miller capacitor dominates all other device capacitors (e.g., C_{gs}).



(d) [4 points] Find the frequency for which the magnitude of the small-signal voltage gain $|a_v|_{dB}$=0dB. If you couldn't solve part (b), assume that a_{vo}=14,000.

(e) [4 points] Given that the channel length of all MOSFETSs is L=3 µ m and that the oxide capacitance per unit area is C_{vo}=14,000.

(d) [4 points] Given that the channel length of all MOSFETs is L=3 µ m and that the oxide capacitance per unit area is C_{ox}=0.5 fF/µ m² (1 fF=1E-15 F), find the differential imput *capacitance* of this op amp.

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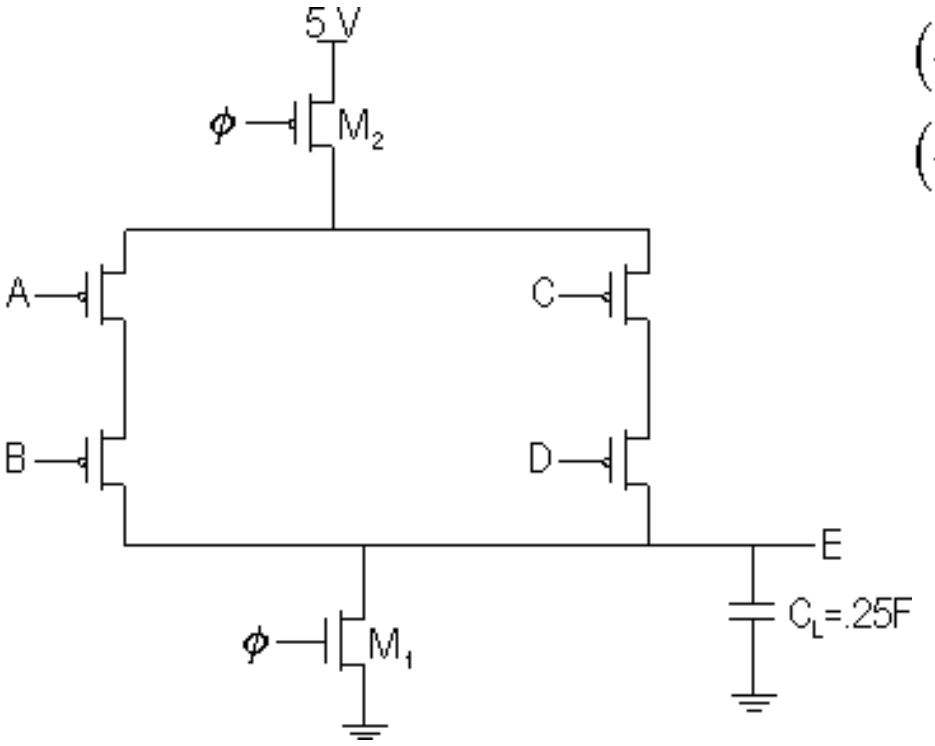
4. Dynamic MOS Logic [20 points]



$$\left(\frac{W}{L}\right)_{1,2} = 50$$

$$\left(\frac{W}{L}\right)_{A,B,C,D} = 5$$

(a) [4 points] What logic function is implemented by this dynamic logic gate? Use the + sign for "OR", a dot for "AND", and an oversocre for "NOT". There is no need to simplify the expression. *Hint*: transistor M1 fuctions to "pre-ground" the load capacitance CL, using clock waveform ϕ(t).

(b) [4 points] How short a 5-V clock pulse (length T_ϕ) can be used to pre-gound the load capacitance, assuming that the minimum T_ϕ is 5 times the propagation delay found in discharaging CL from 5 V ot 0 V? *Hint*: consider the appropriate transistor to be saturated in finding the propagation delay.

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(c) [4 points] Sketch vE(t) on the graph below, for the case where A, B, C, and D are 0 V when t=T_ϕ. You are given that $v_E(0^-)$=5 V just before the clock transitions to 5 V at t=0.

(d) [4 points] What is the propagation delay for the situation in part (c) (all inputs low when the clock goes low)? You can consider that M2 is so wide that it fuctions as a short-circuit when it's "on".

(e) [4 points] What is the propagation delay when A, B, D = 0 and C = 1 (5 V) when the clock ϕ(t) goes low? If you couldn't solve part (c), assume that its answer was t_P=1 ns.

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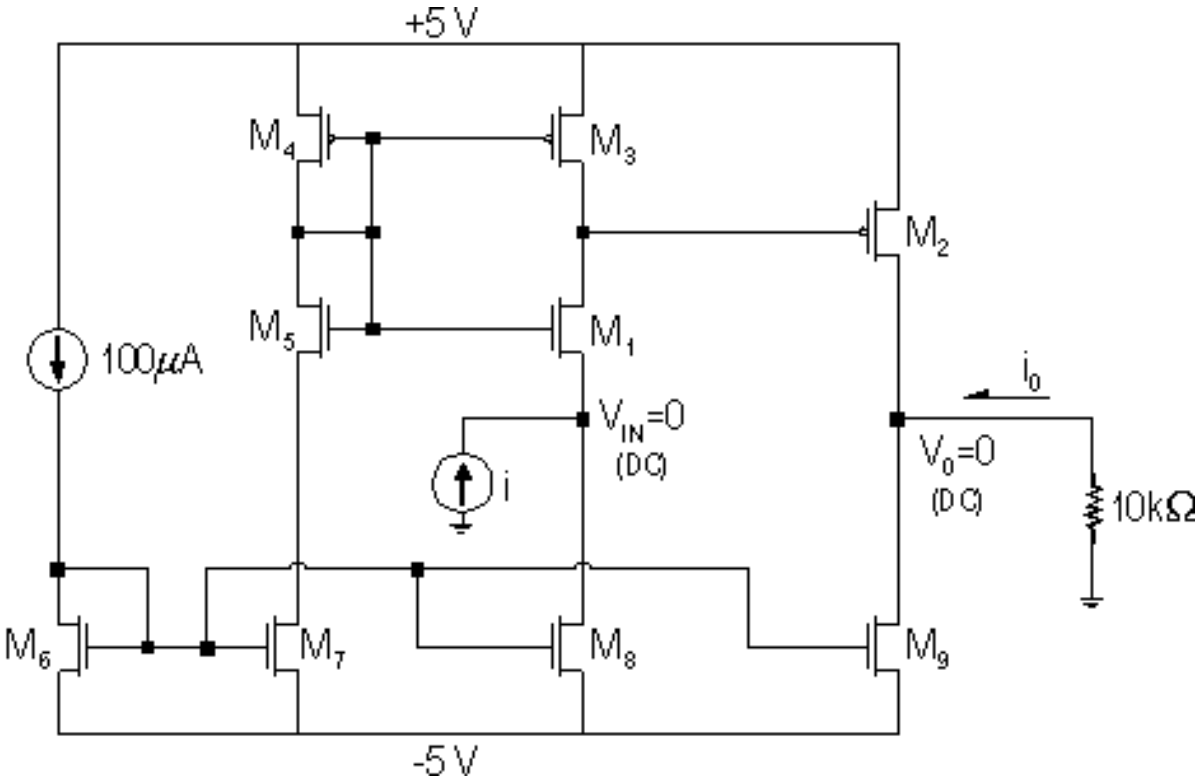
5. Small-signal CMOS current amplifier [20 points]



$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_5 = 50$$

$$\textit{rest have } \left(\frac{W}{L}\right) = 20$$

(a) [4 points] Redraw the schematic, replacing all transistor current sources by the current-source symbol (with the numerical value indicated) and all transistor voltage sources by batteries (with the numberical value indicated).

(b) [4 points] What is the numerical value of the input resistance R_i of this current amp?

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(c) [4 points] What is the numerical value of the output resistance (don't include the load resistor, of course!) for this current amp?

(d) [4 points] What is the short-circuit current gain A_i (v_o a small-signal short to ground) for this current amplifier? Draw the two-port model for the amp.

(e) [4 points] What is the overall current gain i_o/i_{in} with the 100 kΩ load resistor connected to the amplifier?

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translated to HTML by Walter Hsiao
Eta Kappa Nu (November 1995)