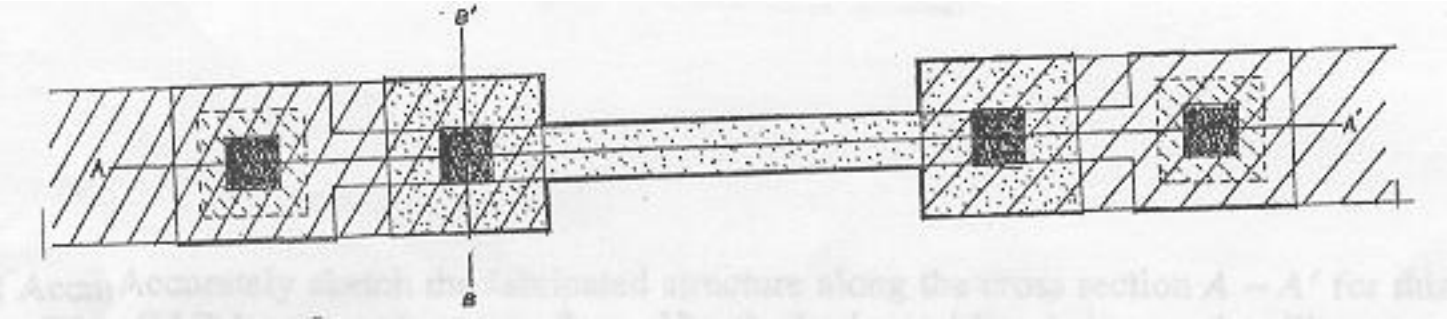
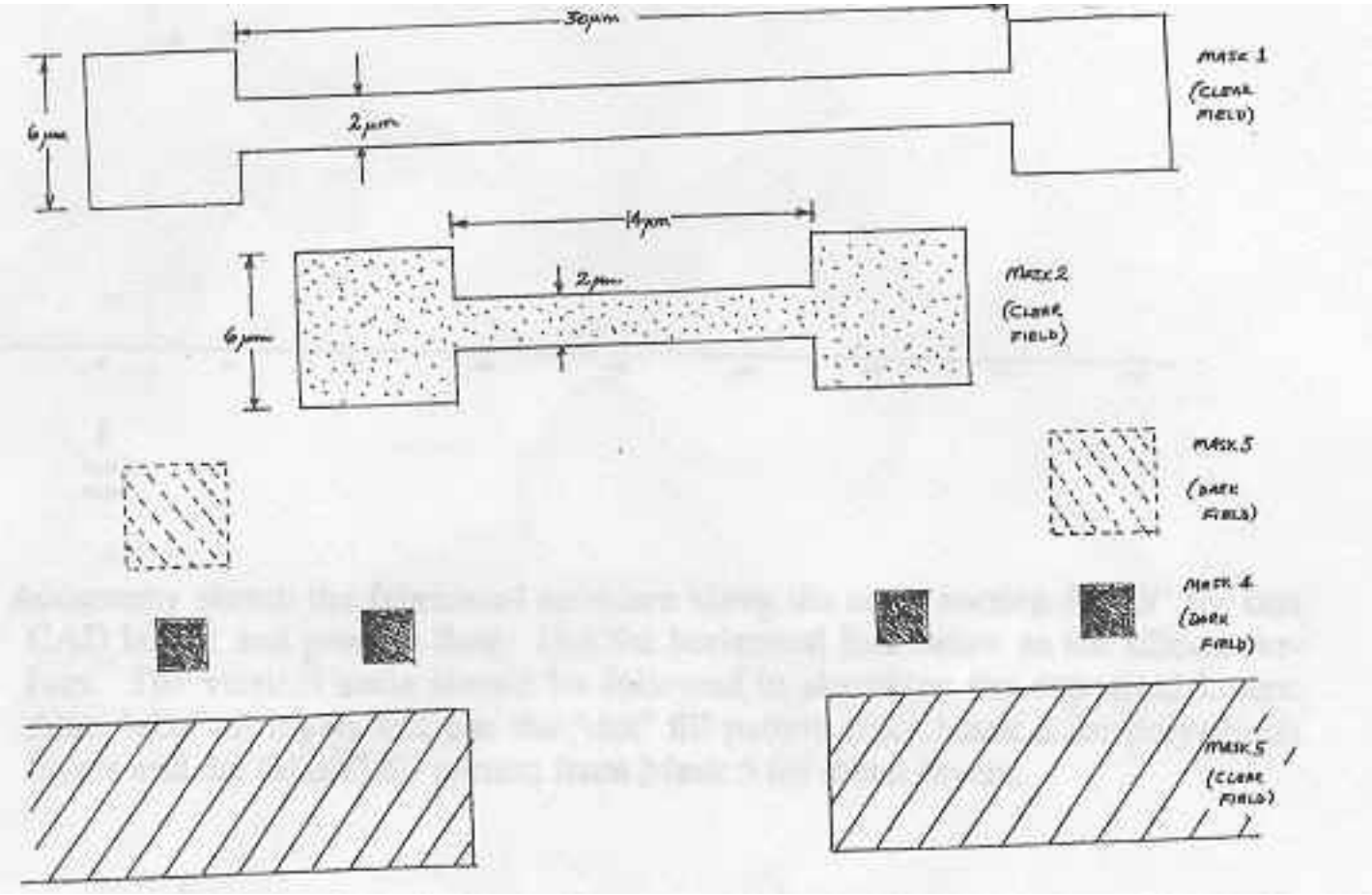
EECS 105
Midterm #1: Spring 1997
Professor R.T. Howe

(Total: 50 points)

Question #1 Multi-layer Resistor Layout [18 points]



The CAD layout for a two-level resistor is shown above; the patterns are shown separately below.



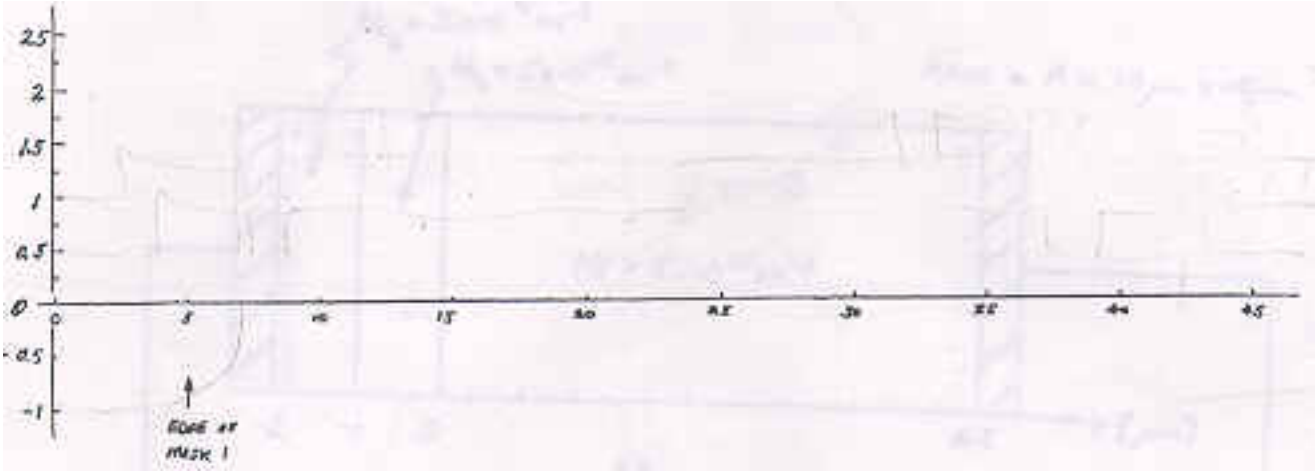
Process Flow

0. Starting material: lightly doped n-type silicon wafer.
1. Deposit .5 um of SiO_2 and pattern using Mask 1.

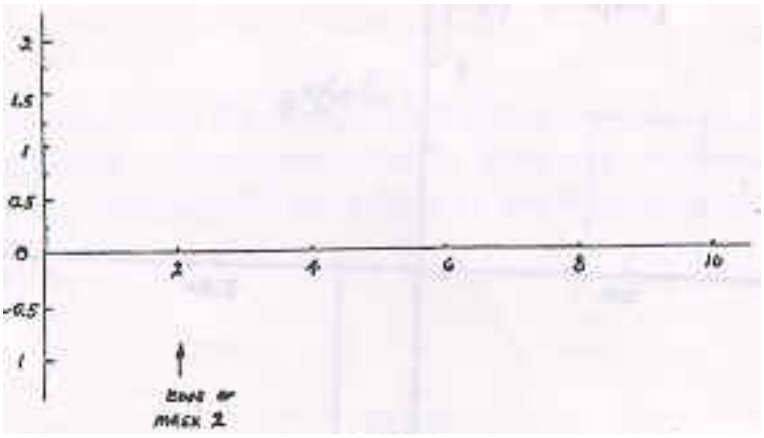
2. Implant boron (dose $Q_a = 10^{14}cm^{-2}$) and anneal to obtain a junction depth x_j = 1 um.
3. Deposit .5 um of SiO_2.
4. Deposit .5 um of polysilicon (sheet resistance 200 Ohms per square) and pattern using Mask 2.
5. Pattern .5 um oxide layer using Mask 3.
6. Deposit .5 um of SiO2 and pattern using Mask 4.
7. Deposit 1 um of aluminum and pattern using Mask 5.

(a) [4 pts.] Find the numerical value of the sheet resistance of the implanted layer formed in step 2, given that the hole mobility in this layer is $u_p = 150\ cm^2/(Vs)$

(b) [5 pts.] Accurately sketch the fabricated structure along the cross section A - A' for this CAD layout and process flow. Use the horizontal line below as the silicon surface. The vertical scale should be followed in sketching the deposited layers. Use the "dot" fill pattern from Mask 2 for polysilicon layer and the "slash' fill pattern from Mask 5 for metal layers.



(c) [5 pts.] Accurately sketch the fabricated structure along the cross section B - B' for this CAD layout and process flow. Use the horizontal line below as the silicon surface. The vertical scale should be followed in sketching the deposited layers. Also, label all layers and use the "dot" fill pattern from Mask 2 for polysilicon layers and the "slash" fill pattern from Mask 5 for metal layers.

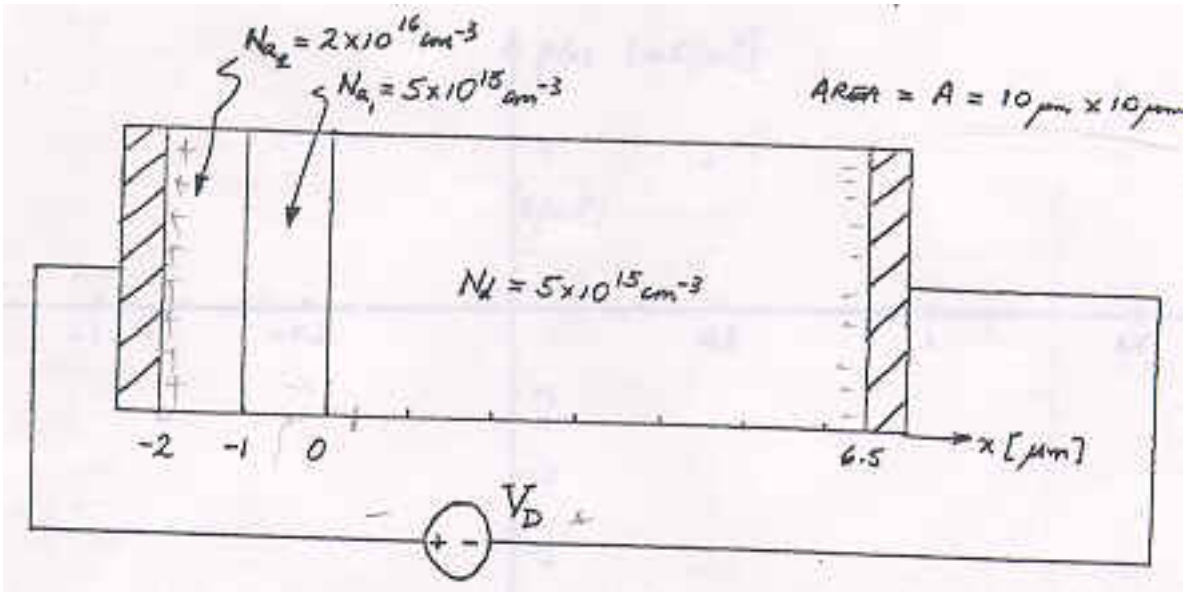


(d) [4 pts.] Given that the "dogbone" contact regions used for both the implanted resistor and the polysilicon resistor contribute 0.6 squares, find the resistance between the metal interconnections in kilo-Ohms. If you couldn't solve part (a), you can assume that the implanted layer has a sheet resistance of 250 Ohms per square.

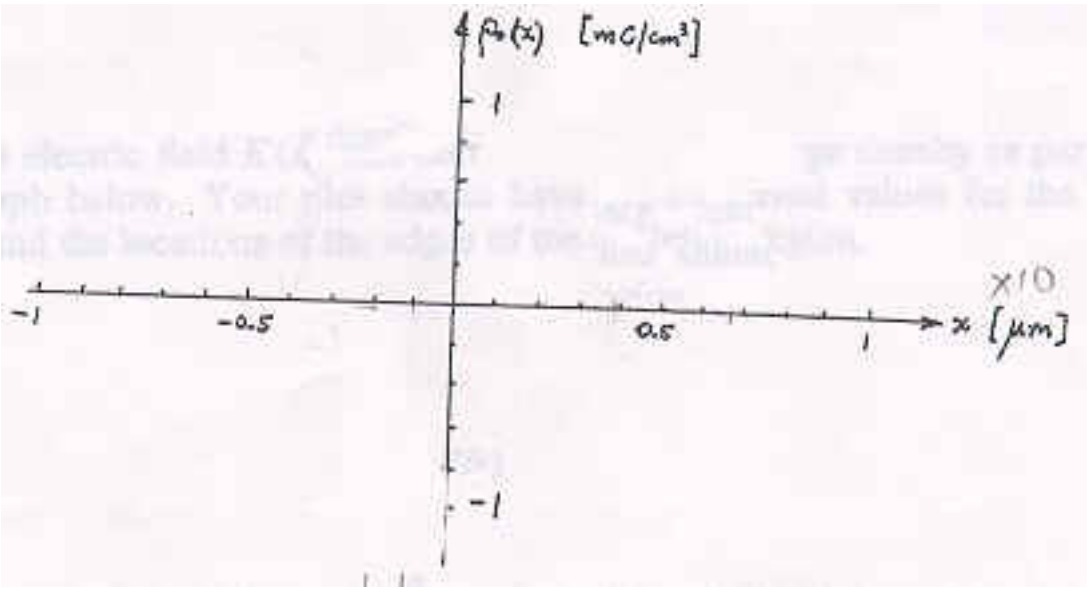
Question #2 pn Junction Electrostatics [17 points]

Given:
$q = 1.6 * 10^{-19}$ C, $E_s = 11.7\ E_0 = 1.04 * 10^{-12}$ F/cm, 1 um = 10^{-4} cm

The p-side of this pn junction has two levels of acceptor concentration.

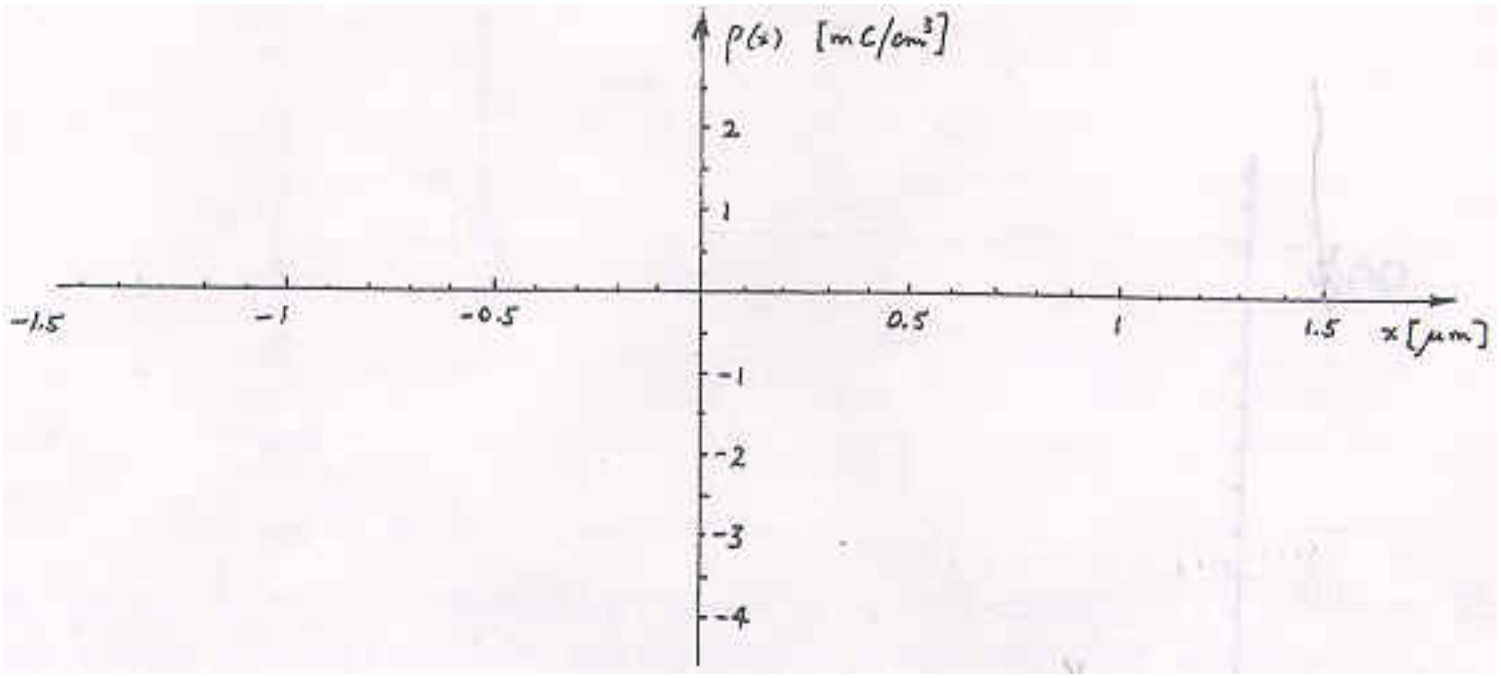


(a) [3 pts.] Given that the edge of the depletion region on the n-side of the junction is located at x_{no} = .4 um in thermal equilibrium (V_d = 0 V), plot the thermal equilibrium charge density $p_0(x)$ on the graph below.

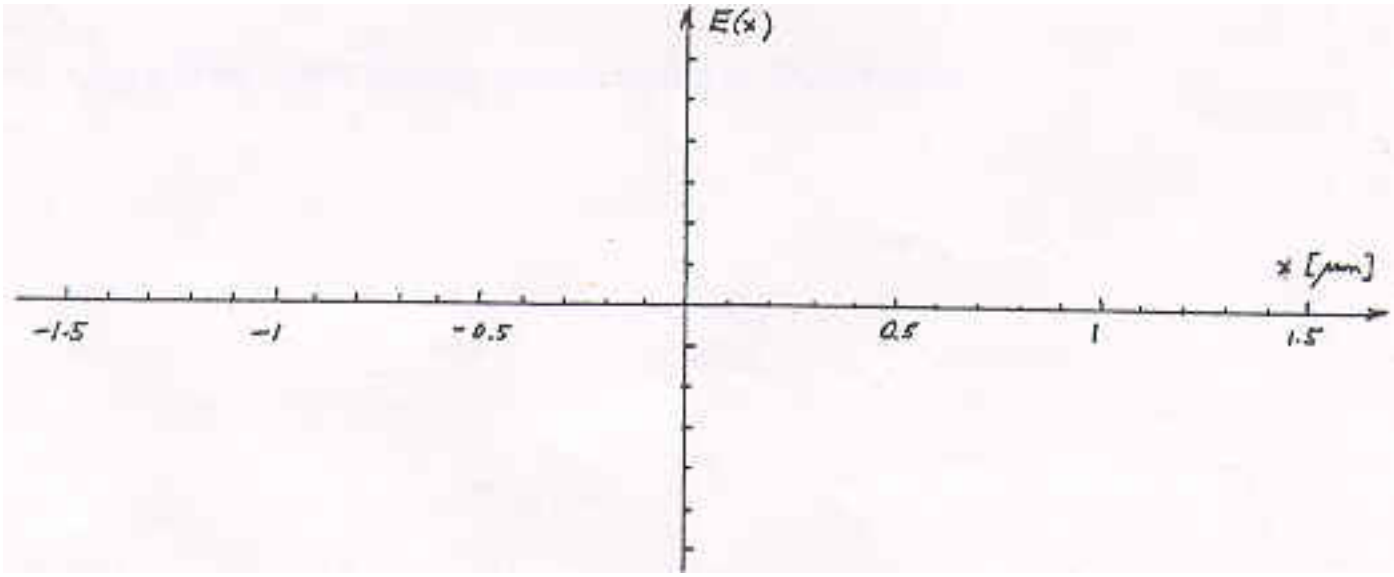


(b) [3 pts.] Find the numerical value of the depletion capacitance in thermal equilibrium C_{jo} in fF (1 fF = 10^{-15} F).

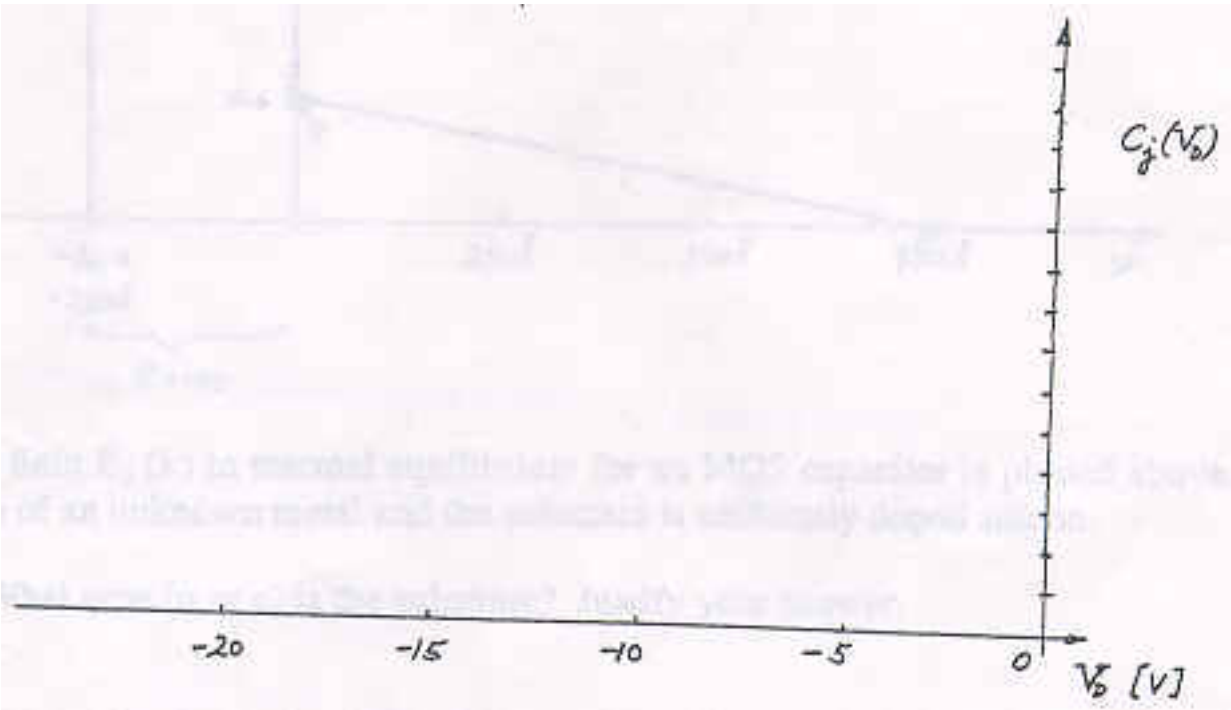
(c) [4 pts.] For V_D = -12 V, the edge of the depletion region on the n-side of the junction is located at x_n = 1.5 um. Plot the charge density p(x) for this reverse bias on the graph below.



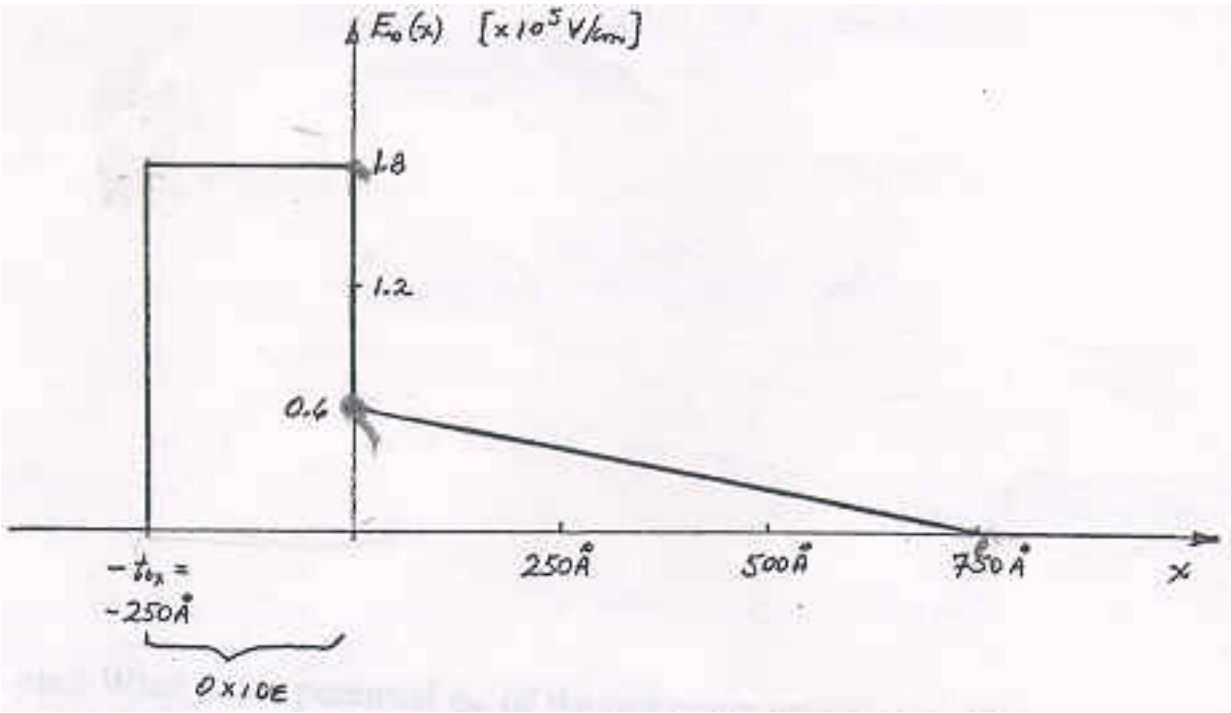
(d) [4 pts.] Plot the electric field E(x) that corresponds to the charge density in part (c) on the graph below. Your plot should have the numerical values for the field at x = 0 and the locations of the edges of the depletion region.



(e) [3 pts.] **Sketch** the depletion capacitance $C_j(V_D)$ on the graph below. Given: for V_D = -4V, the depletion region edge on the n-side of the junction is x_n = 1 um. Clearly indicate any breakpoints where the capacitance function changes.



Question #3 MOS Electrostatics [15 points]



The electric field $E_0(x)$ in thermal equilibrium for an MOS capacitor is plotted above. The gate is made of an unknown metal and the substrate is uniformly doped silicon.

(a) [4 pts.] What type (n or p) is the substrate? Justify your answer.

(b) [4 pts.] What is the doping concentration in the substrate?

(c) [4 pts.] What is the numerical value of the voltage drop $V_{ox,o}$ in thermal equilibrium? *Hint*: the electric field plot is all that you need!

(d) [3 pts.] What is the potential phi_g of the unknown gate material?