Microelectronic Devices and Circuits- EECS105

Second Midterm Exam

Friday, November 20, 1998

Costas J. Spanos

University of California at Berkeley

College of Engineering

Department of Electrical Engineering and Computer Sciences

Your Name: ____

(last) (first)

Your Signature: ____

1. Print and sign your name on this page before you start.

2. <u>You are allowed two, 8.5"x11" handwritten sheets with formulas. No books or notes!</u>

3. Do everything on this exam, and make your methods as clear as possible.

Problem 1 ______ / 30

Problem 2 ______ / 35

Problem 3 ______ / 35

TOTAL ______ / 100

Problem 1 of 3 Answer each question briefly and clearly. (30 points)

How is the voltage gain of a CMOS inverter related to the transconductances of its transistors? (5 pts)

Why are CMOS NAND gates preferable to CMOS NOR gates? (5 pts)

Why do you need an n-channel *and* a p-channel transistor in parallel in order to have a proper "pass" logic gate? (5 pts)

What is a "unilateral" amplifier? (5 pts)

Please indicate with an up or down arrow the effect of the following on the voltage gain (Av) of a common source amplifier (5 pts)

Parameter	Effect on Av	Brief Explanation (optional)
W/L		
Idsat		
L		
$\mu_n C_{ox}$		

-

What single-transistor amplifier stage can be used to ensure very high output resistance? (5 pts)

Problem 2 of 3 (35 points)

In this problem you will size a CMOS inverter with process parameter V_{Tn} = 0.7V, V_{Tp} = -0.9V,

μ_n Cox = 50μ A / V^2, μ_p Cox = 25μ A / V^2, $\lambda_n = \lambda_n = 0.1V^{-1}\mu\, m^{-1}$. Assume equals lengths and V_{DD} = 5V.

For each of the following questions, make sure that you show the expressions before you plug in the specific values. A correct expression is worth 70% of the credit, even if the numerical calculation is incorrect!

a) Calculate the ration W_n / W_p, such that V_M = 2.5V (for this question you can ignore the channel-length modulation effect). (7 pts)

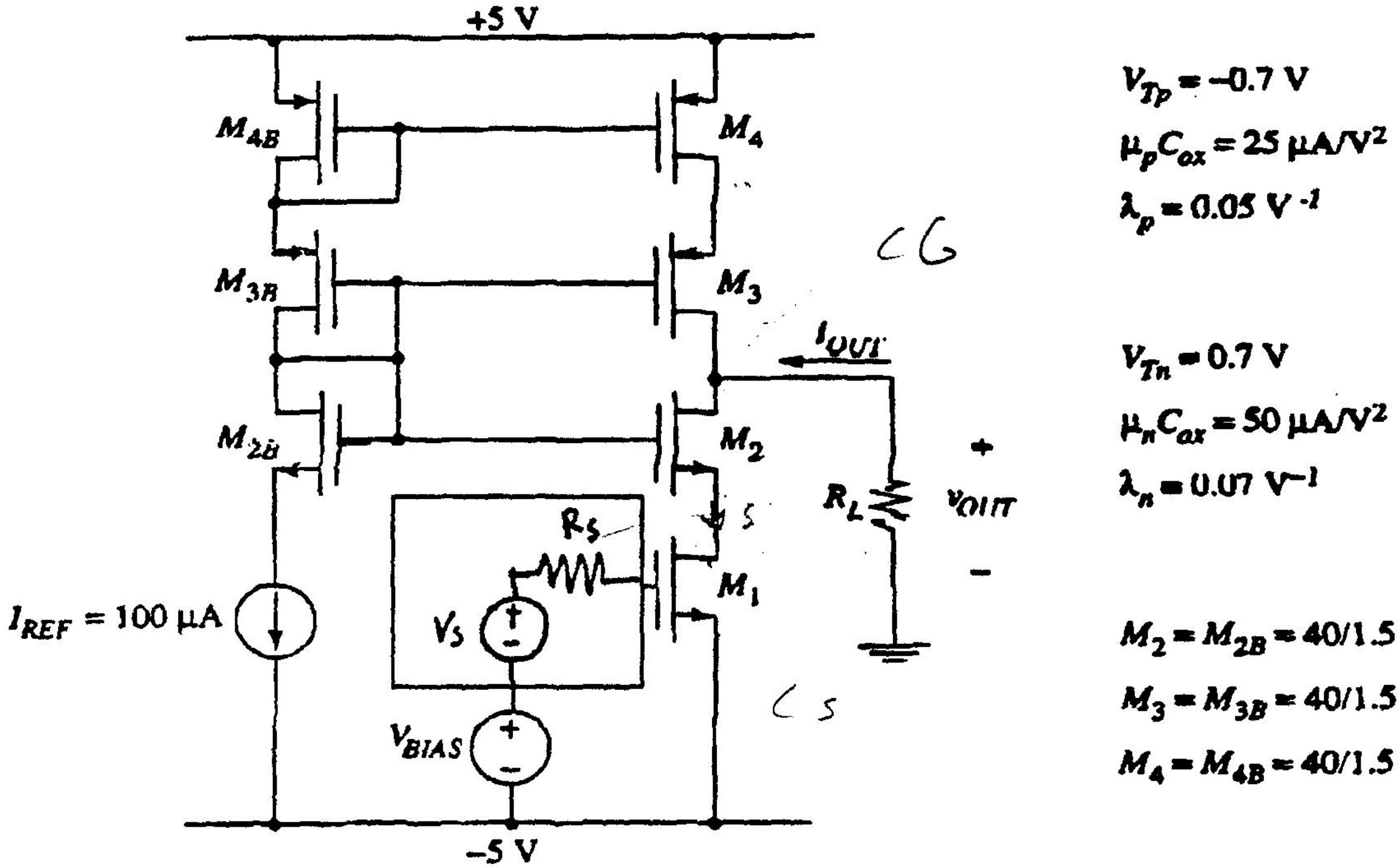
b) When $V_{in} = V_M$ we want the current through the inverter to be 1mA. What is W_n and W_p assuming that the channel length of both devices is 2μ m? (7 pts)

c) Sketch and label the voltage transfer characteristic with V_{IL}, V_{IH}, V_{OL}, V_{OH}, V_M. (7 pts)

d) What are the values of NM_L and NM_H? (7 pts)

e) Would noise margins improve if you made the devices longer, while keeping everything else fixed? (Give a yes / no answer and explain it in brief qualitative terms) (7 pts)

Problem 3 of 3 (35 points)



A CMOS cascade transconductance amplifier and the device data are shown above. There is no backgate effect.

For each of the following questions, make sure that you show the expression <u>*before*</u> *you plug in the specific values. A correct expression is worth 70% of the credit, even if the numerical calculation is incorrect!*

(a) Find the $(W/L)_1$ for M_1, so that the small signal transconductance i_{out}/v_s = 1mS. Assume $R_L = 0\Omega$ (short circuit output current) for this part. (7 pts)

(b) Calculate the value of V_{BIAS} using the $(W/L)_1$ calculated in part (a) such that I_{OUT} = 0A. (7 pts)

(c) Calculate the output resistance of this transconductance amplifier. (7 pts)

(d) What is the maximum value of the load resistor RL at which the overall transconductance is degraded by 20% from the original value of 1mS? (7 pts)

(e) Calculate the maximum voltage swing at the output of this amplifier. (7 pts)
