EE 105 Midterm I

Fall 2001

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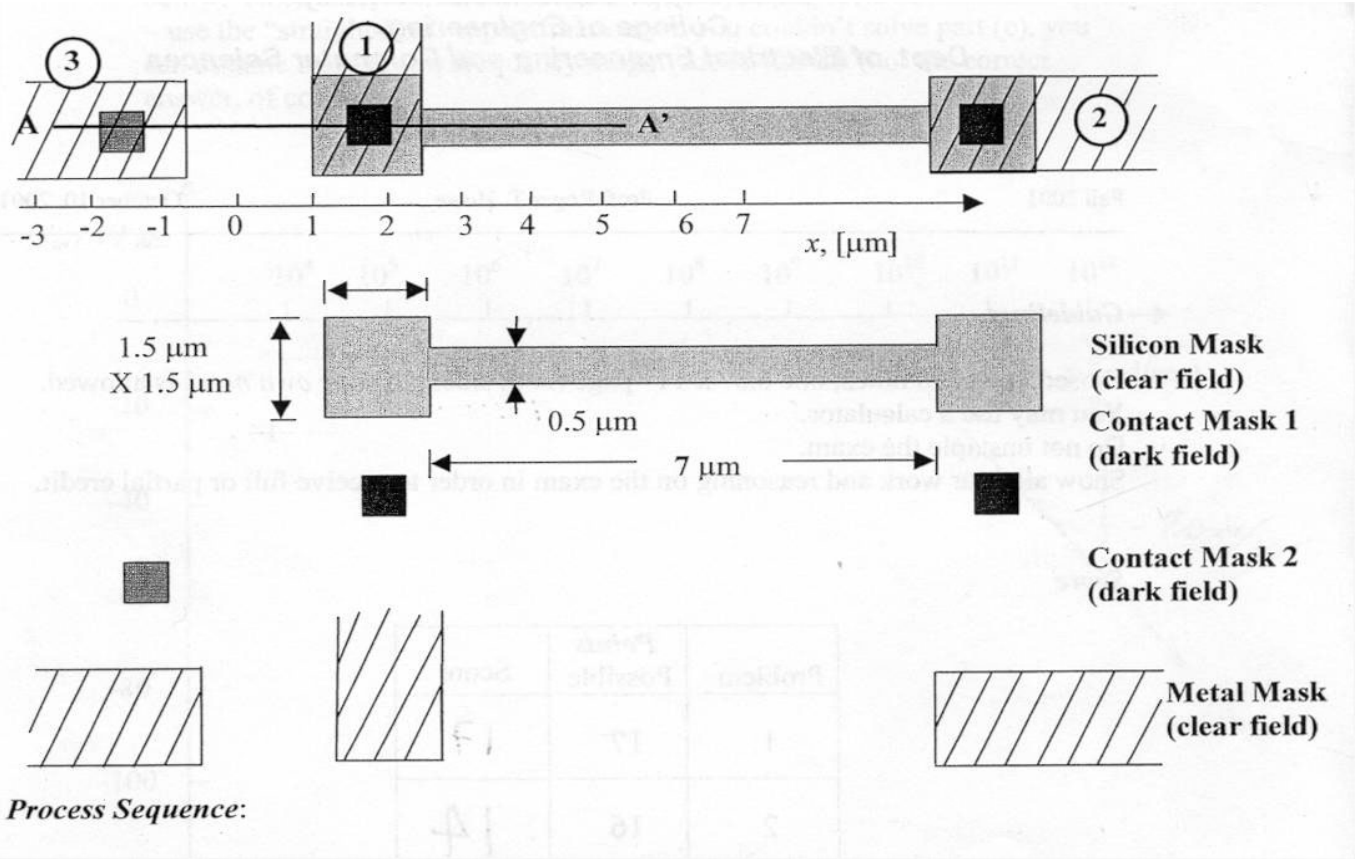
1. Silicon-on-Insulator (SOI) Resistor [17 points]

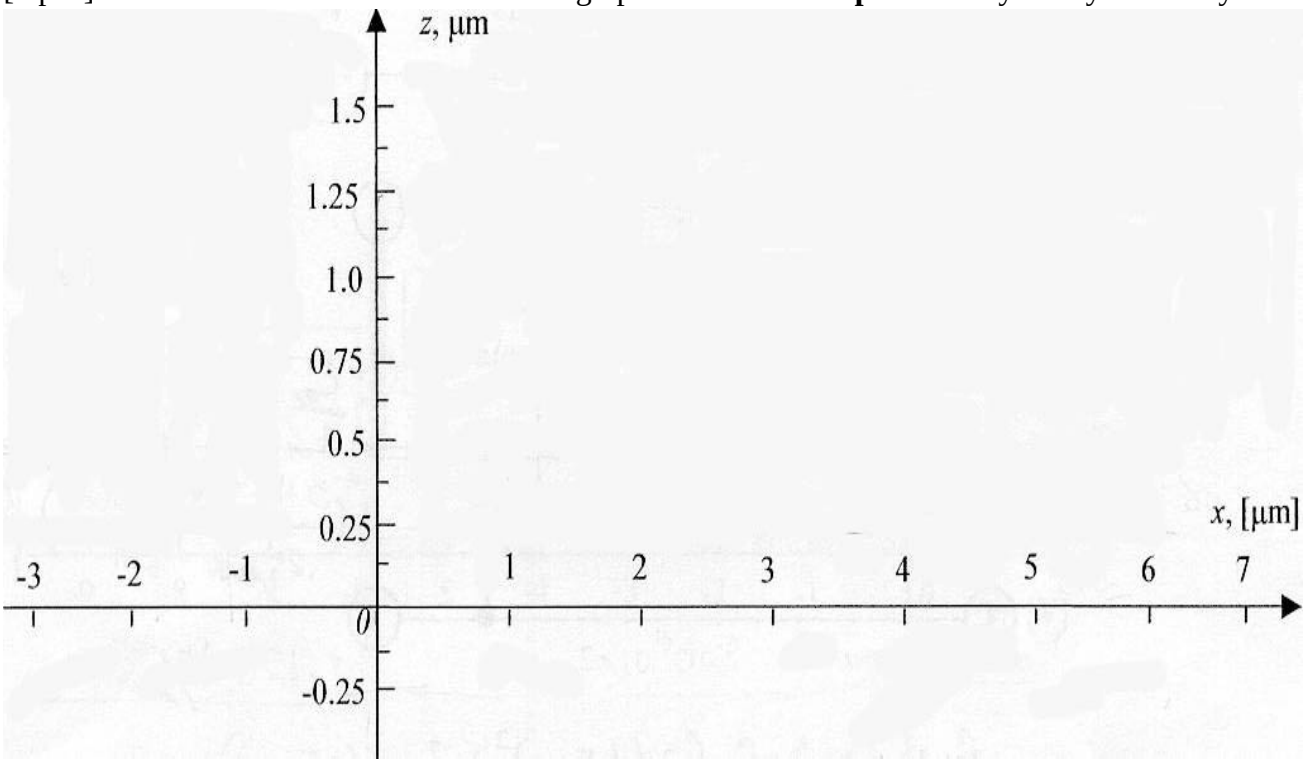


Process Sequence:

1. *Starting material:* silicon-on-insulator substrate, which is a 500 um-thick, heavily doped n-type silicon wafer, on which a 0.25 um-thick "buried oxide" is grown, over which is grown (by a special process) a 0.25 um-thick layer of n-type single crystal silicon. The 0.25 um-thick silicon layer is doped with phosphorus at a concentration of 3×10^{16} cm^{-3}
2. Implant boron with dose $Q_a = 5 \times 10^{13}$ cm^{-2} and anneal so that the boron concentration is uniform through the 0.25 um-thick silicon layer.
3. Pattern the 0.25 um-thick silicon layer using the **Silicon Mask** (clear field).
4. Deposit 0.5 um of CVD SiO_2 and pattern using **Contact Mask 1** (dark field).
5. Pattern the sandwich of the 0.25 um-thick "buried oxide" and the 0.5 um-thick CVD oxide using **Contact Mask 2** (dark field). *Note*: the resulting contact hole reaches to the underlying n-type silicon substrate.
6. Deposit 0.5 um of aluminum and pattern using the **Metal Mask** (clear field).

Given: mobilities for this problem are $u_n = 1000$ $cm^2/(Vs)$ and $u_p = 400$ $cm^2/(Vs)$. Count the "dogbone" contact areas as 0.65 square each in finding the resistance. The permittivity of oxide is $e_{ox} = 3.45 \times 10^{-13}$ F/cm.

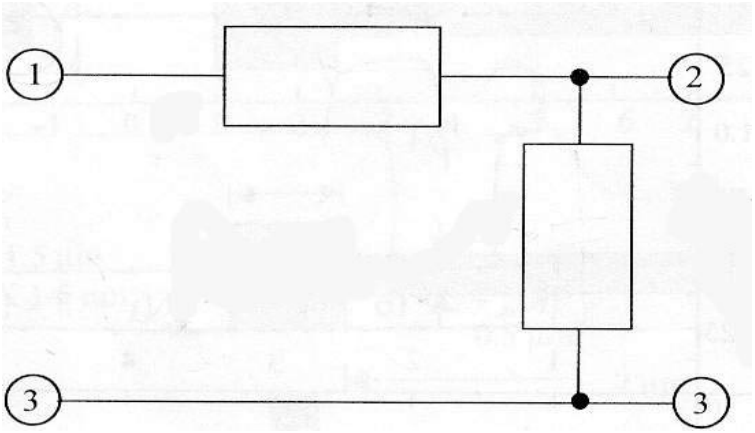
a. [5 pts.] Sketch the cross section ***A-A'*** on the graph below **after step 6.** Identify all layers clearly.



b. [3 pts.] What is the sheet resistance R-square of the 0.25 um-thick silicon layer?

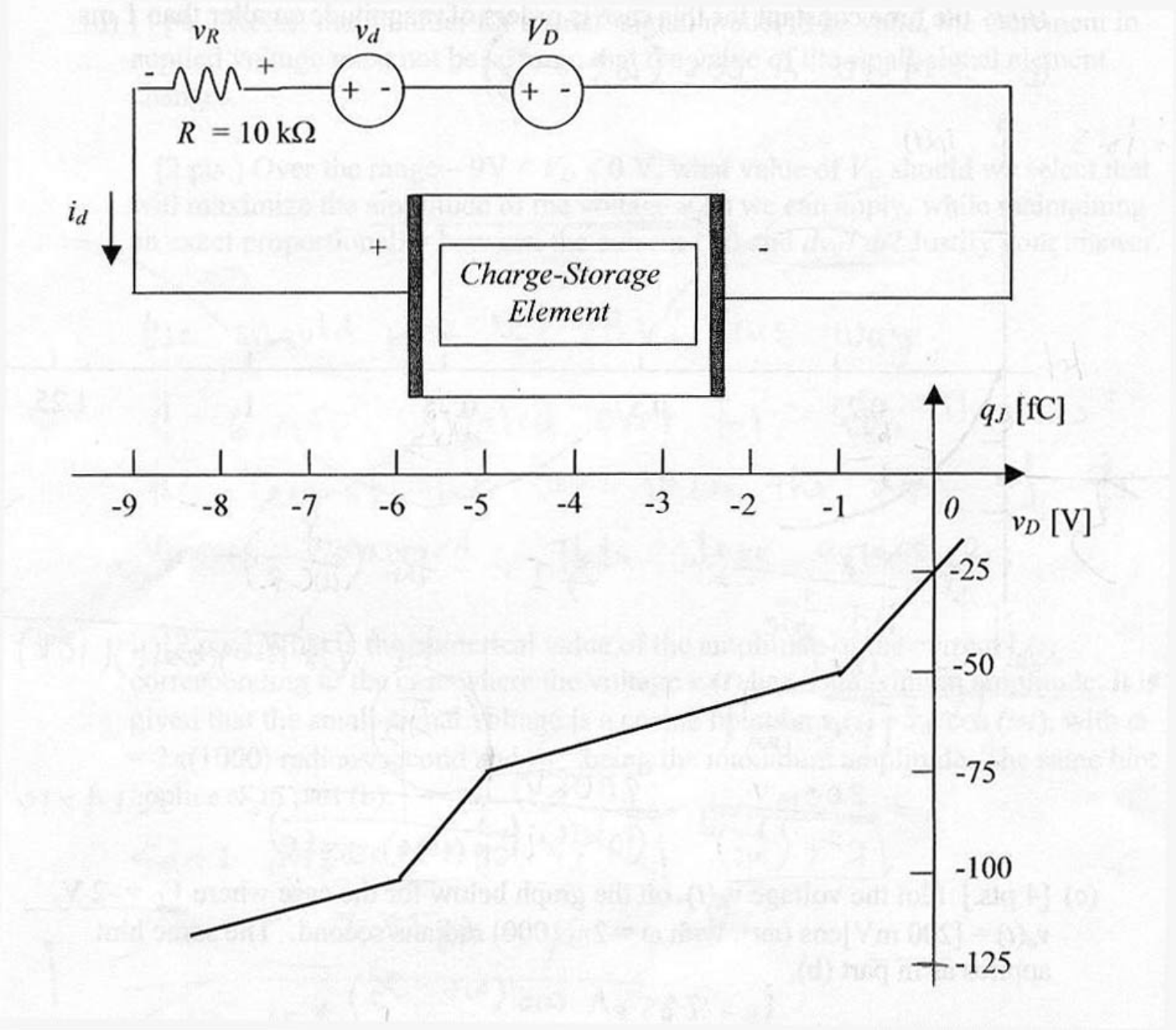
c. [3 pts.] What is the resistance $R_{1\text{-}2}$ between terminals 1 and 2 in ohms? If you couldn't solve part (a), use R-square = 200 ohms (not a correct answer to (a)).

d. [4 pts.] Fill in the boxes in the circuit model below with the correct elements *and* their values. Your answer to part (c) should be helpful. You can assume that V_1 and V_2 are each greater than 2 V and that V_3 = 0 V.



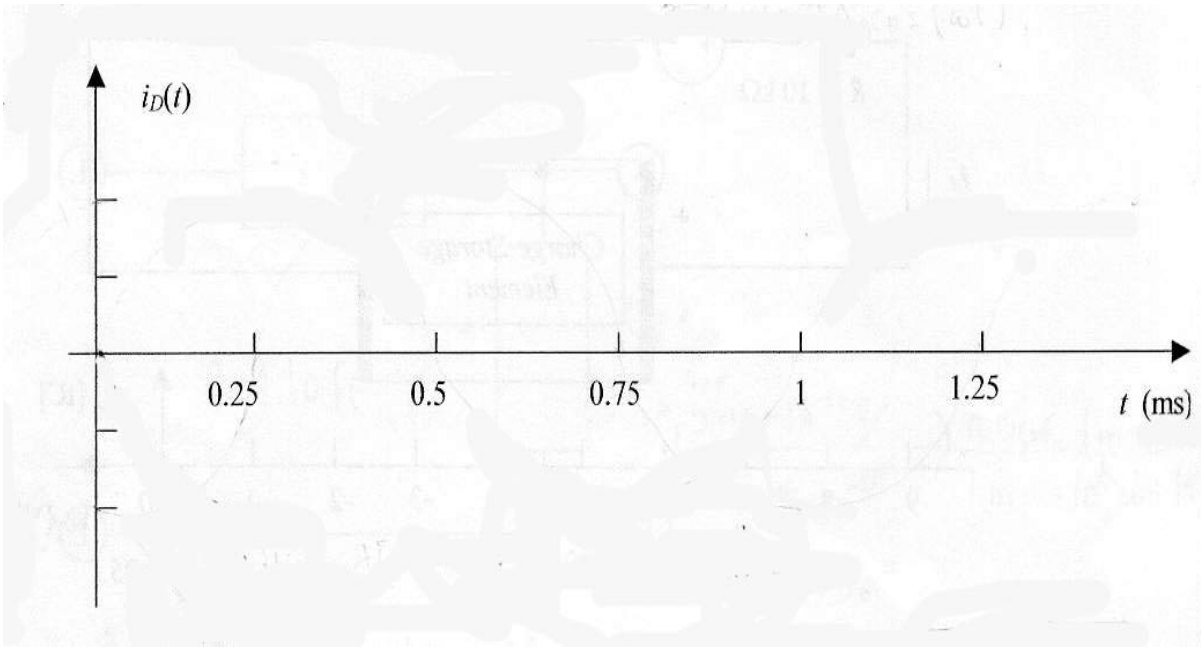
e. [2 pts.] Now if the voltages of terminals 1 and 2 are each lowered to approximately -0.25 V, with terminal 3 (the n-type substrate) being grounded, what is the effect on $R_{1\text{-}2}$ compared to the case in part (d)? Justify your answer.

2. Unusual junction charge-storage element [16 pts.]

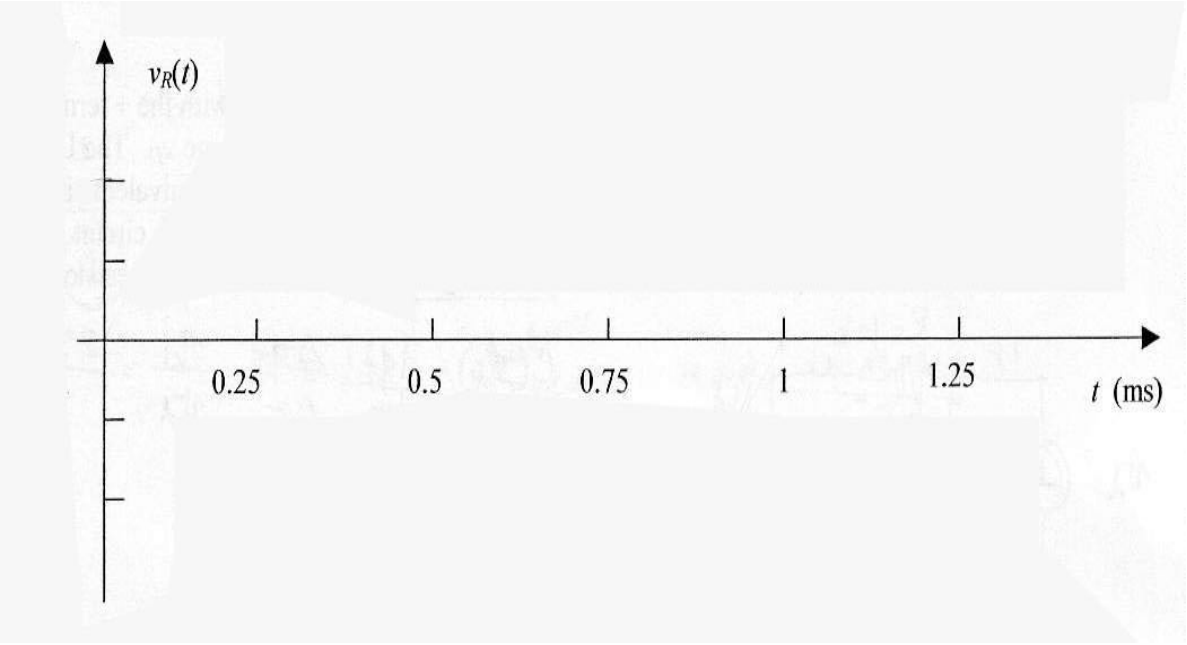


a. [4 pts.] The plot is the internal stored charge q_J associated with the + terminal of the charge-storage element, as a function of the applied voltage v_D. The DC current I_D through the device is zero. Draw the small-signal equivalent circuit for the case where V_D = -0.5 V. *Hint*: your answer should have three circuit elements, two of which are the small-signal voltage source and the resistor.

b. [4 pts.] For the case where V_D = -0.5 V and $v_d(t)$ = [200 mV]cos(omega*t), with omega = 2pi(1000) radians/second, plot the current waveform $i_D(t)$ on the graph below. *Hint*: the time constant for this case is orders of magnitude smaller than 1 ms.



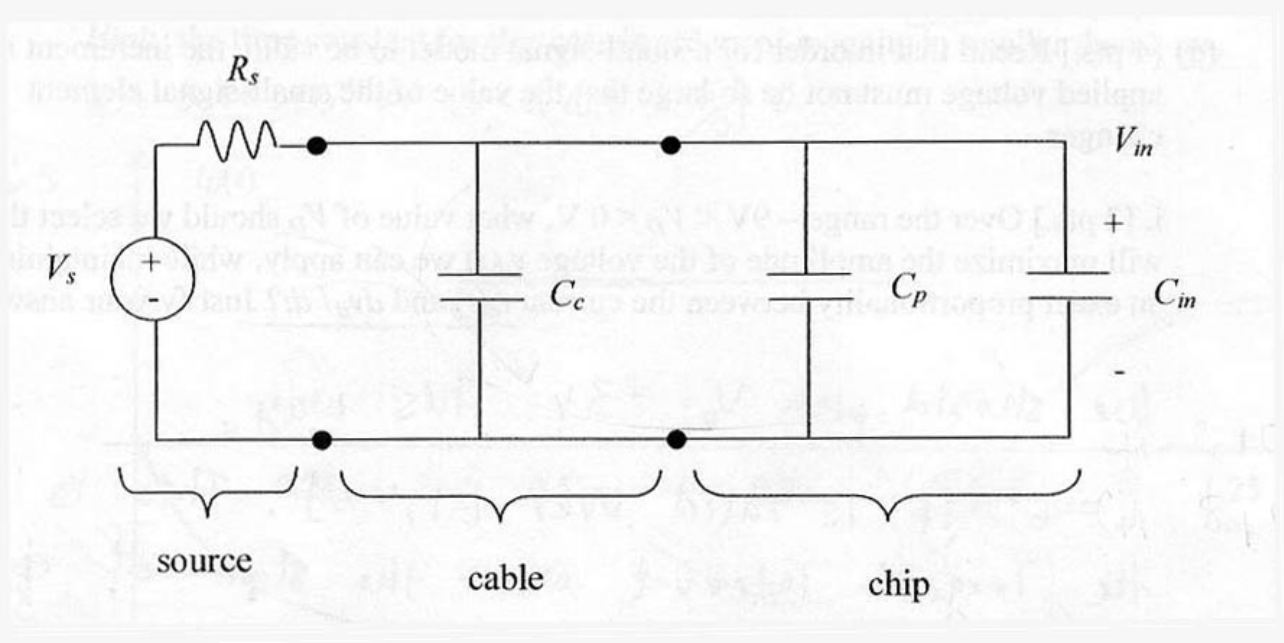
c. [4 pts.] Plot the voltage $v_R(t)$ on the graph below for the case where V_D = -2 V, $v_d(t)$ = [200 mV]cos (omega*t), with omega = 2pi(1000) radians/second. The same hint applies as in part (b).



d. [4 pts.] Recall that in order for a small-signal model to be valid, the increment in applied voltage must not be so large that the value of the small-signal element changes.
   i. [2 pts.] Over the range -9 V < V_D < 0 V, what value of V_D should we select that will maximize the amplitude of the voltage $v_d(t)$ we can apply, while maintaining an exact proportionality between the current $i_d(t)$ and dv_d/dt? Justify your answer.

ii. [2 pts.] What is the numerical value of the amplitude of the current $i_d(t)$ corresponding to the case where the voltage $v_d(t)$ has its maximum amplitude. It is given that the small-signal voltage is a cosine function $v_d(t) = v_d*\cos(\omega*t)$, with $\omega = 2\pi(1000)$ radians/second and v_d* being the maximum amplitude. The same hint applies as in part (b).

3. Frequency response measurements [17 pts.]

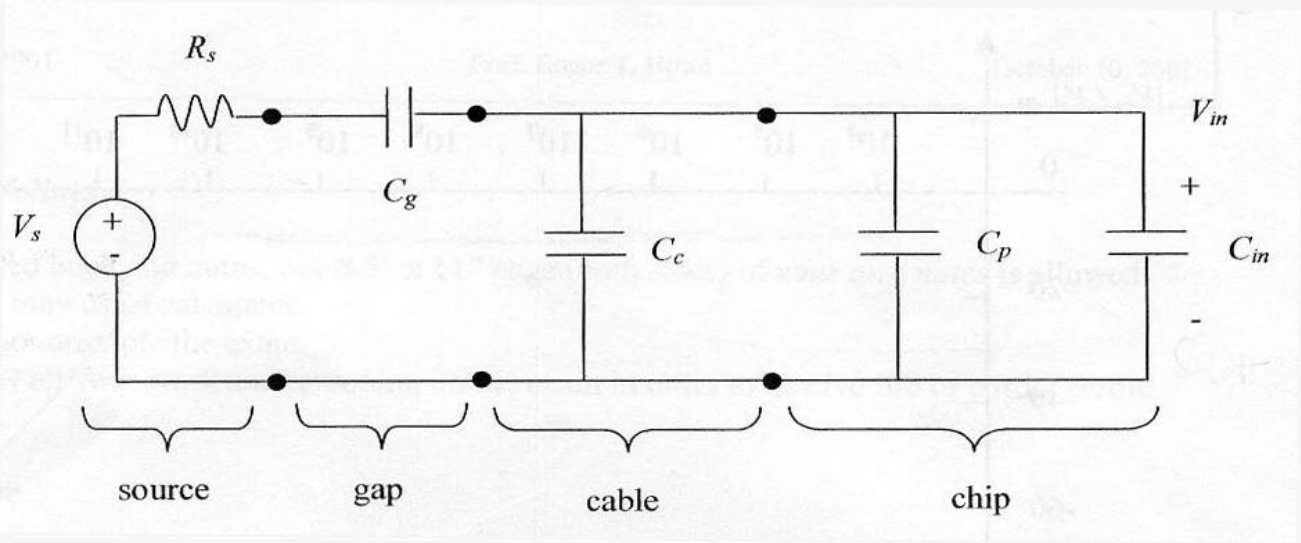


The above circuit models a test set-up to measure the input impedance of an IC amplifier. The cable has a capacitance C_c = 5 pF, the chip has a pad and interconnect apacitnce C_p = 2 pF, and the amplifier's input capacitance is C_{in} = 1 pF. The sinusoidal source has an amplitude of 100 mV and a source resistance R_s = 50 ohms.

a. [3 pts.] Find the transfer function V_{in} / V_s in the standard form of a low-pass filter.

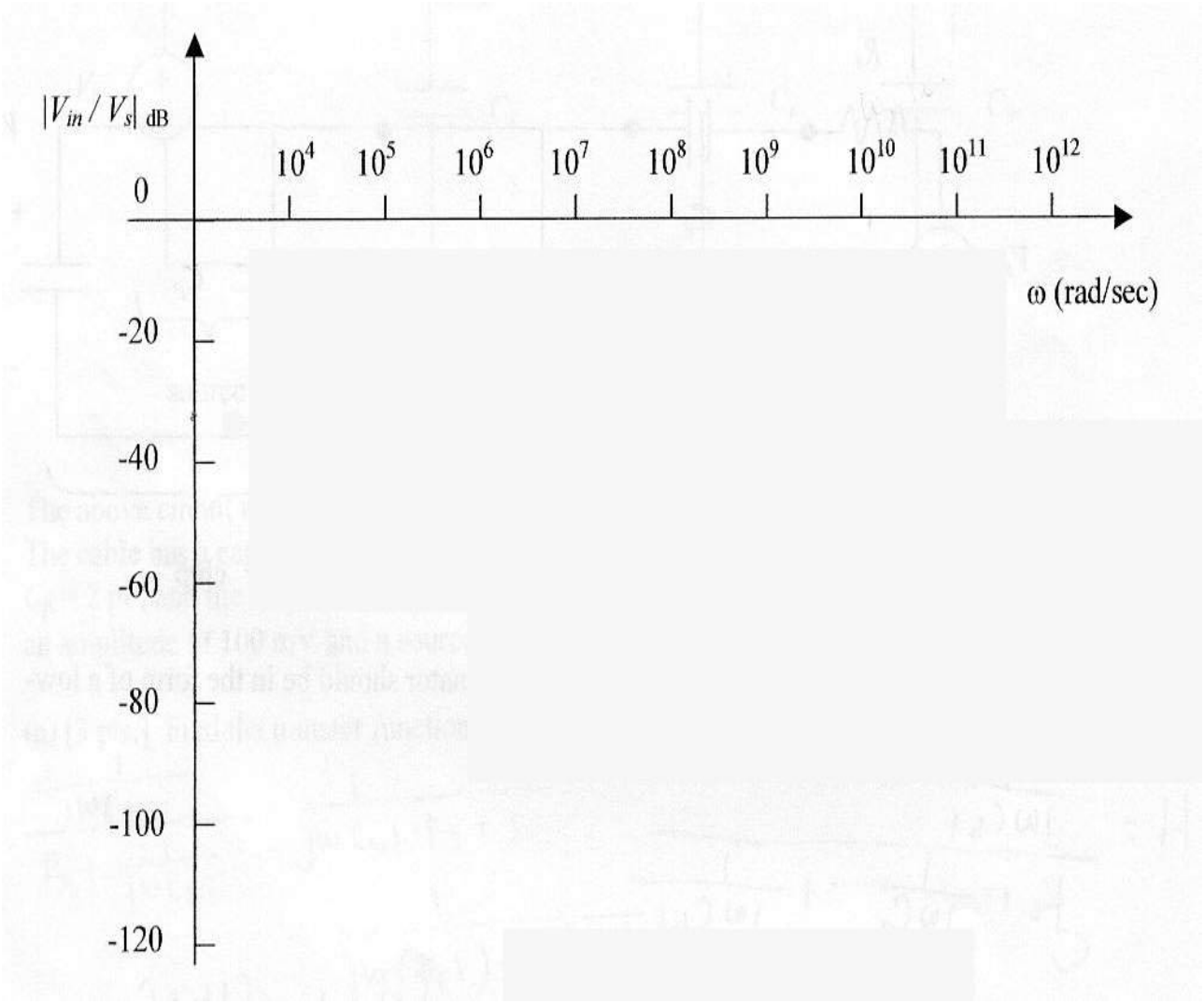
b. [3 pts.] Find the amplitude of $v_{in}(t)$ when the source has a frequency omega = 2.5 Grad/s.

c. [4 pts.] You notice that your measurements don't agree with the prediction from part (b), so you inspect your test setup. You discover that the cable connector wasn't fully inserted, so there's a small gap between it and the output of the source. This gap is modeled by a capacitor of value C_g = 2 pF, as shown in the schematic below.



Find the transfer function V_{in} / V_s. Hint: the denominator should be in the form of a low-pass fitler.

d. [4 pts.] Sketch the magnitude of V_{in} / V_s in dB versus frequency on the plot below. Note that your low and high-frequency asymptotes should be accurate - use the "straight-line" approximation. If you couldn't solve part (c), you can assume that the low frequency magnitude is -20 dB (not the correct answer, of course).



e. [3 pts.] For the circuit in part (c), find the phase of V_{in} for the case where the source frequency is omega = 2.5 Grad/s. *Hint*: your result in part (d) may be helpful.