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EECS 141: SPRING 94 - FINAL

For all problems, you can assume the following transistor parameters:

NMOS:

V_{Tn}=0.75V, k'_n=20μAV^2, λ=0.05, γ=0.5V$^{1/2}$, $2\Phi_F$=-0.6V

PMOS:

V_{Tp}=0.75V, k'_n=7μAV^2, λ=0.1, γ=0.5V$^{1/2}$, $2\Phi_F$=-0.6V

Bipolar NPN:

β_F=100, $V_{BE(on)}$=0.7V, $V_{BE(sat)}$=0.8V, $V_{CE(sat)}$=0.1V

Wiring:

Aluminum: $C_{parallel\text{-}plate}$=0.03 fF/$\mu$m^2; C_{fringe}=0.045 fF/μm, R_{sheet}=0Ω

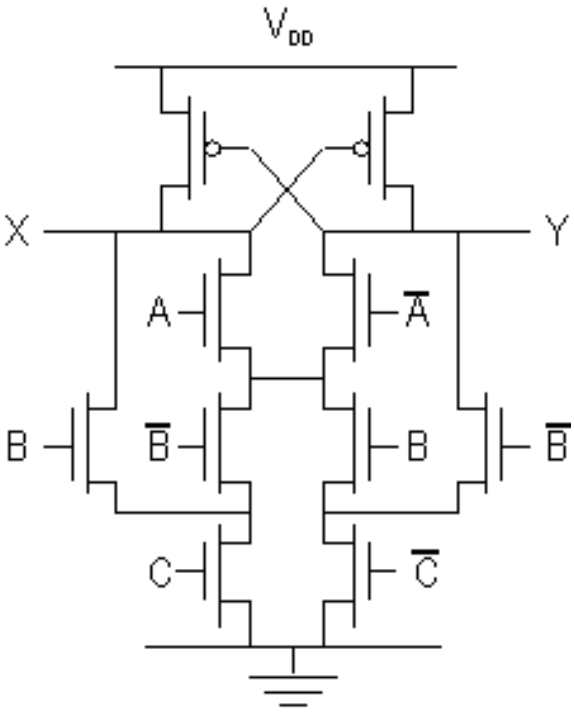
Polysilicon: $C_{parallel\text{-}plate}$=0.06 fF/$\mu$m^2; C_{fringe}=0.045 fF/μm, R_{sheet}=10Ω

For all problems, you may assume that the transistor lengths indicated are the effective lengths(L_{eff}) or, equivalently, that LD=0.

All questions are worth 15 points, except problem 1 which is graded on 10 points.

PROBLEM 1: Logic

a) Derive the logic functions of the following gate (make sure to minimize the resulting boolean expressions).



X =

Y =

b) Mark the statements, which you believe **ALWAYS** to be true.

- ☐ Differential logic uses more transistors and, hence, is slower.
- ☐ The above circuit does not consume static power.
- ☐ The above circuit can suffer from charge redistribution.
- ☐ Adder cells with less transistors consume less dynamic power, since the overall capacitance is smaller.
- ☐ Dynamic logic consumes more dynamic power than static since the number of transistors is higher.

PROBLEM 2: Memory(1)

A smart designer in a famous semiconductor company has finally conceived what he believes is the ultimate SRAM memory cell. He calls it the 5 transistor cell, show in FIG. 1 The bitline is normally precharged to V_{DD}.

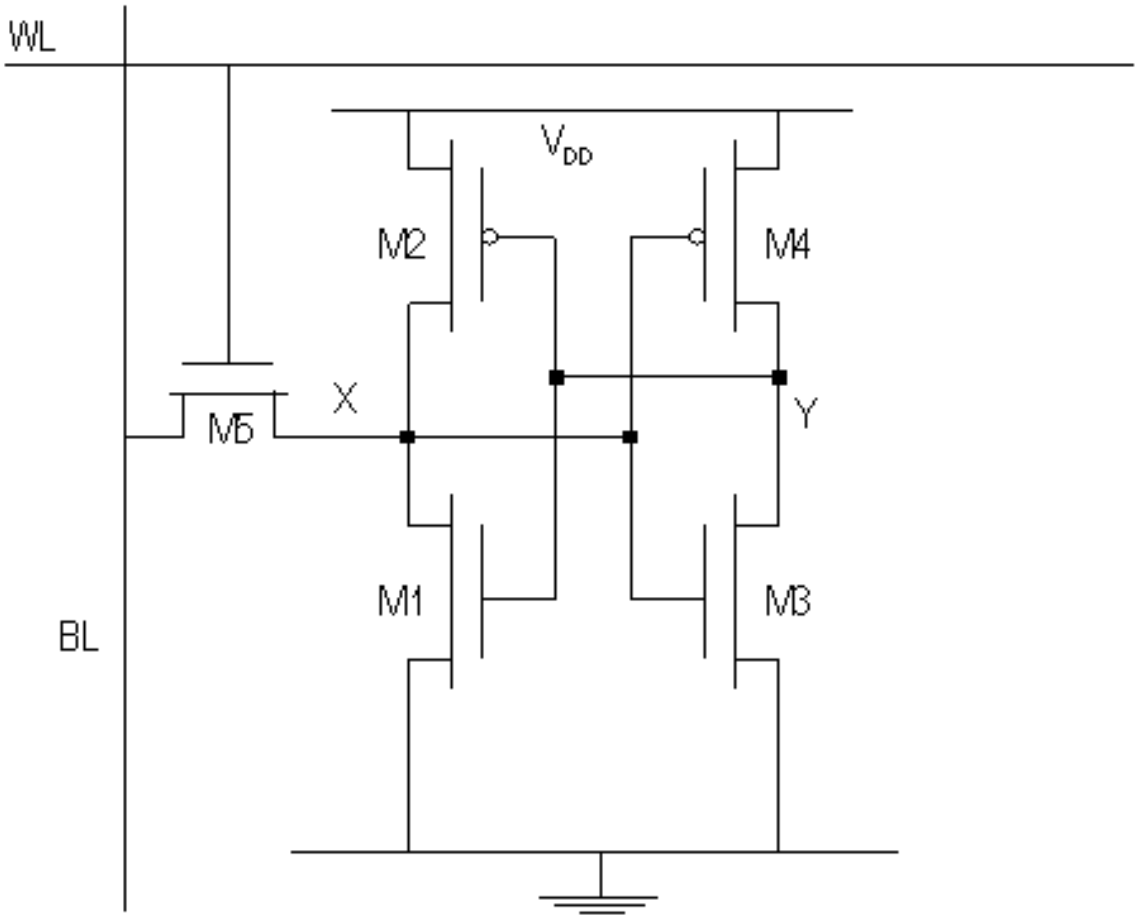


FIG. 1 5 transistor SRAM cell.

a) The designer figures out real fast that the transistor sizing of this cell is non-trivial, however, describe **ALL the constraints** which should be imposed on the devices for guaranteeing save, read and write operations. Write down the equations, which would help you to size the transistors. DO NOT SOLVE THE EQUATIONS NOR PLUG IN NUMBERS: Using the following variables: V_{DD}, V_T (same for N and PMOS), k_{Mx}, and V_M (of an inverter).

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b) Based on the above equations, discuss (quantitatively) the required relative sizing of the transistors in the cell. (for instance, transistor M_x has to be wider than transistor M_y).

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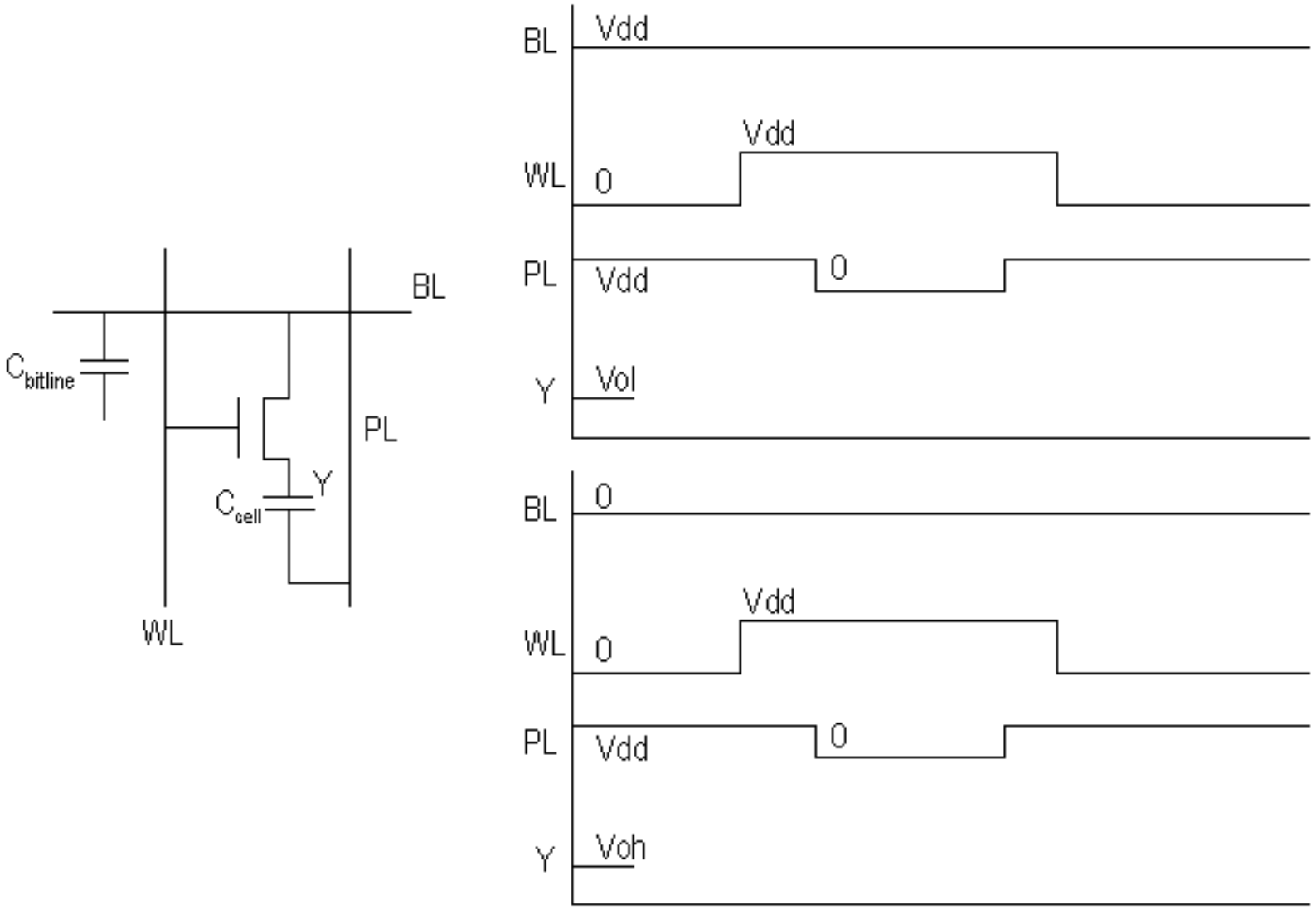
PROBLEM 3: Memory(2)
Shown below is a variant of the IT-DRAM cell.

a) Fill in the iming diagrams for the write operation. Denote the voltage levels in terms of V_{DD} and V_T (ignore body effect, IGNORE TRANSIENT EFFECTS.



b) Describe briefly why this is an attractive approach

c) Assume that the bitline capacitance equals 500fF. The transistor threshold equals 0.75V (ignore body effect). The supply voltage equals 5V and the bitline is pre(dis)charged to 0V. Derive the symbolic equations needed to derive the bitline voltages after reading a "0" and a "1". IGNORE TRANSIENT EFFECTS.

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d) Using the results from c), derive the minimum cell capacitance such that the voltage difference on the bitline between reading a "0" and a "1" is larger than 250mV.

$C_{cell.min}$ =

PROBLEM 4: Interconnect (1)

While designer Jim Jones is developing a new microprocessor, he suddenly gets confronted with the fact that driving the bus network is the speed limiting factor. The diagram of the network is shown in FIG 2. The total wire-length of the bus, implemented as a 3 μm wide aluminum wire, equals 1.5cm and it connects to a fanout of 20 gates, each representing a load of 100fF. The input capacitance of the driver equals 30fF. Use the technology data given on the first page.

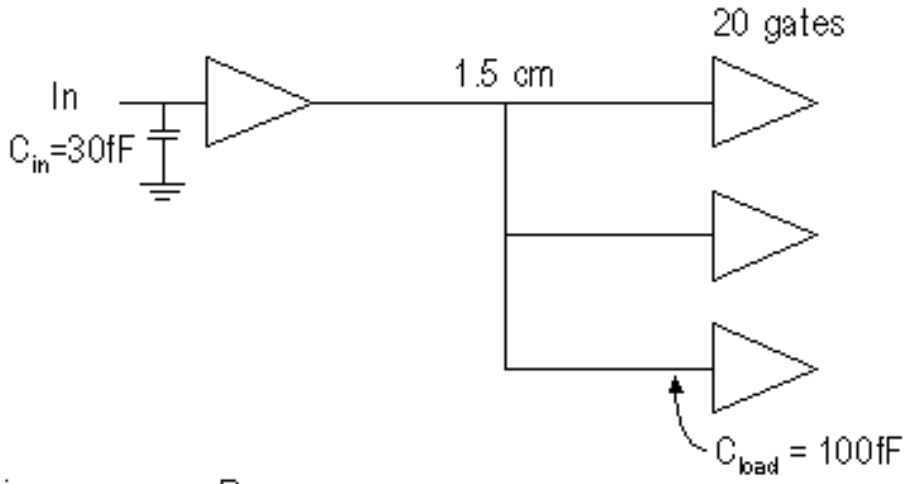

FIG. 2 Microprocessor Bus

a) Determine the total load capacitance on the bus.

C_{load} =

b) Determine the minimum time it would take to drive this capacitance, if Jones can spend as much area as he wants on the driver (without increasing the input capacitance). You may assume that the propagation delay of the minimum sized buffer equals 200psec.

t_{min} =

c) In a microprocessor design, area is an important consideration. Jones has figured out tat if he can drive the bus in 5 nsec, he should have no problem in meeting the overall system design constraints. Derive the composition of a buffer which can achieve this goal in a minimum area. Determine the number of stages required.

#stages =

d) It turns out that the process Jones is using is a BiCMOS process. Instead of using a CMOS driver, Jones

could just as well have used an emitter-follower, as shown in FIG. 3, to drive the load. Determine the time it would take to charge the bus capacitance from 0V to the 50% point (t_{pLH}) using this structure.

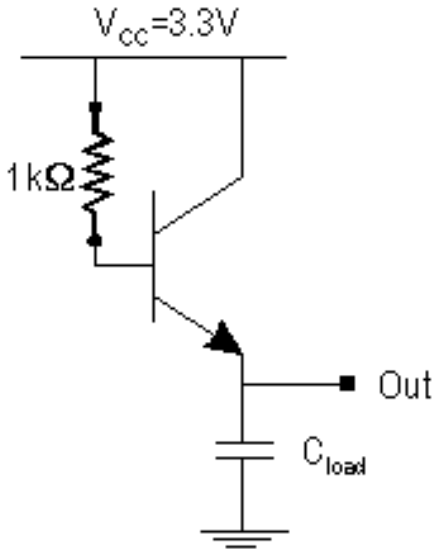

FIG. 3 Emitter-follower

t_{pLH} =

PROBLEM 5: Interconnect (2)

Still working on his microprocessor, Jones discovers a second interconnect problem. To send data to the external memory, he has to go off chip, as shown in FIG. 3. The copper wire on the board, which is 15 cm long, acts as a transmission line with a characteristic impedance of 100 Ω. You may assume that the memory input pins represent a very high impedance, which for all practical purposes can be considered as infinite. The bus driver is a CMOS inverter, consisting of very large devices of (120/1.2) for the NMOS and (360/1.2) for the PMOS. You may also assume that the on-resistance of the minimum size devices (1.8/1.2 and 5.4/1.2, for NMOS and PMOS, respectively) equals 10k Ω and scales proportionally with the size of the transistors.

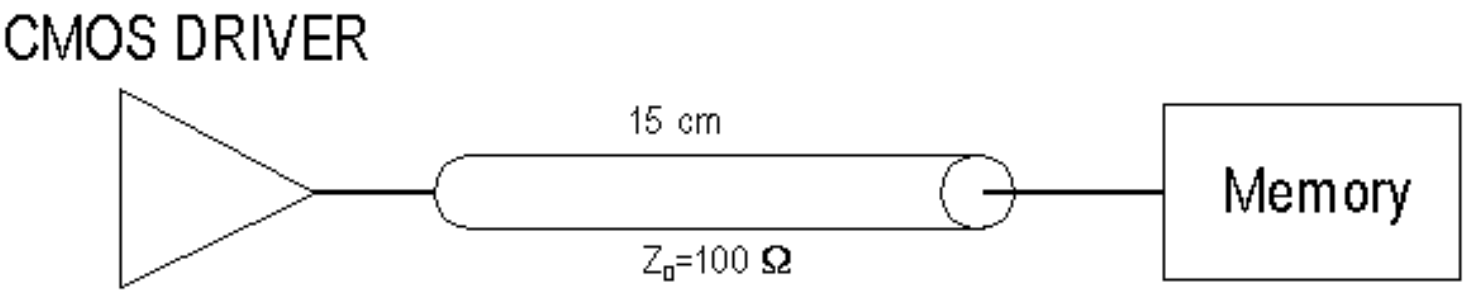

FIG. 4 Driving the memory through a transmission line

a) Determine the time it takes for a change in signal to propagate from the source to the destination (or, in

other words, what is the time of flight). You may assume that the wire inductance per unit length equals 75 × 10E-8 H/m.

time of flight =

b) Given the driver device sizes defined above, determine how long it will take the output signal to stay within 10% of its final value. You can model the driver as a voltage source with the driving device acting as series source resistance. Determine the reflection coefficients on both source and destination ends and draw the lattice diagram for the transmission line. Assume a supply and step voltage of 5V.

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ρ_{source} = ρ_{dest} =

$t_{90\%}$ =

c) Jones, being an educated designer, knows how to tackle that problem. He resizes the device dimensions of his driver to minimize the transmission line delay. Determine that minimum time and derive the corresponding sizes for the NMOS and PMOS transistors.

t_{min} =

$(W/L)_N$ =	$(W/L)_p$ =

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PROBLEM 6: Timing

Consider the register shown below and address the questions raised below. Assume that the delay through an inverter equals t_i, which is also the delay through a pass transistor (with the appropriate load).

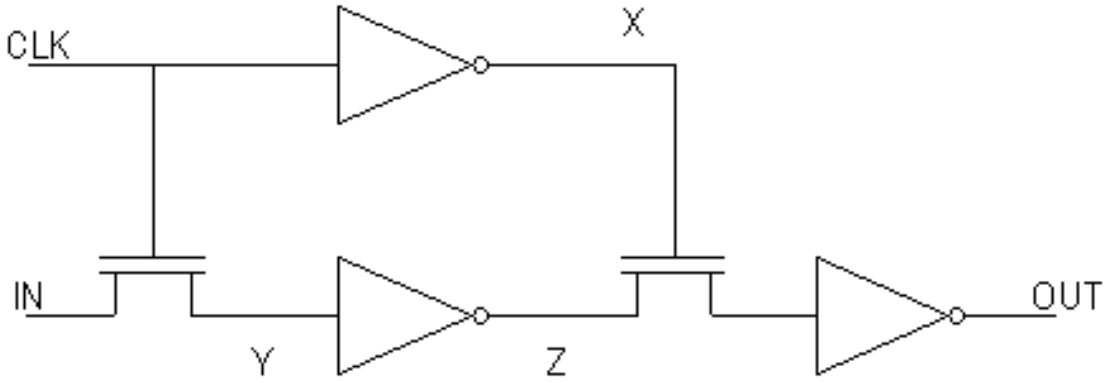
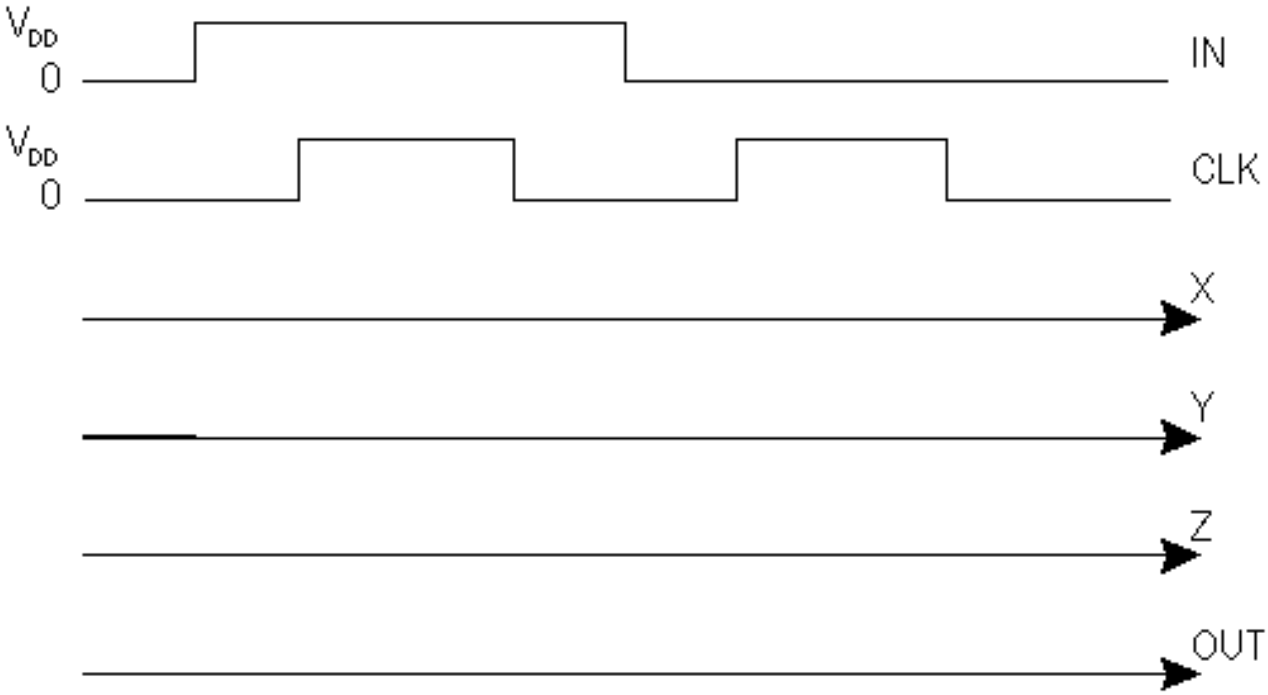


FIG. 5 Single clock register

a) Draw the signal waveform for the X, Y, Z and OUT signals given the IN and CLK signals (the supply voltage equals V_{DD}).



b) Does this circuit show a race problem? If yes, say why. If no, determine under what conditions a race would occur.

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c) Derive a simple way of making this circuit ABSOLUTELY insensitive to the race problem. DON'T ADD or REMOVE transistors, just reorganize.

d) Determine the maximum clock frequency of the circuit.

f_{max} =

e) Is there a minimum clock frequency? If so, why.

f_{min}? ☐ yes ☐ no

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PROBLEM 7: Sequential Circuits

a) For the design of the voltage controlled oscillator, engineer Amanda Lee initially decides she will use a ring oscillator. After quite a number of hours, she decides that 5 stages is the right number for her. The oscillation frequency should be 5 MHz for a supply voltage fo 3.3V. The basic inverter circuit in the oscillator is shown in FIG. 6. Due to their large sizes, you may consider transistors M2 and M3 to be ideal switches (with **zero resistance**). Determine the DC voltages needed at nodes H and L needed to get the required oscillation frequency. Consider only the capacitance shown in the figure. Ignore the channel length modulation factor. Also make sure that rise and fall times are identical.

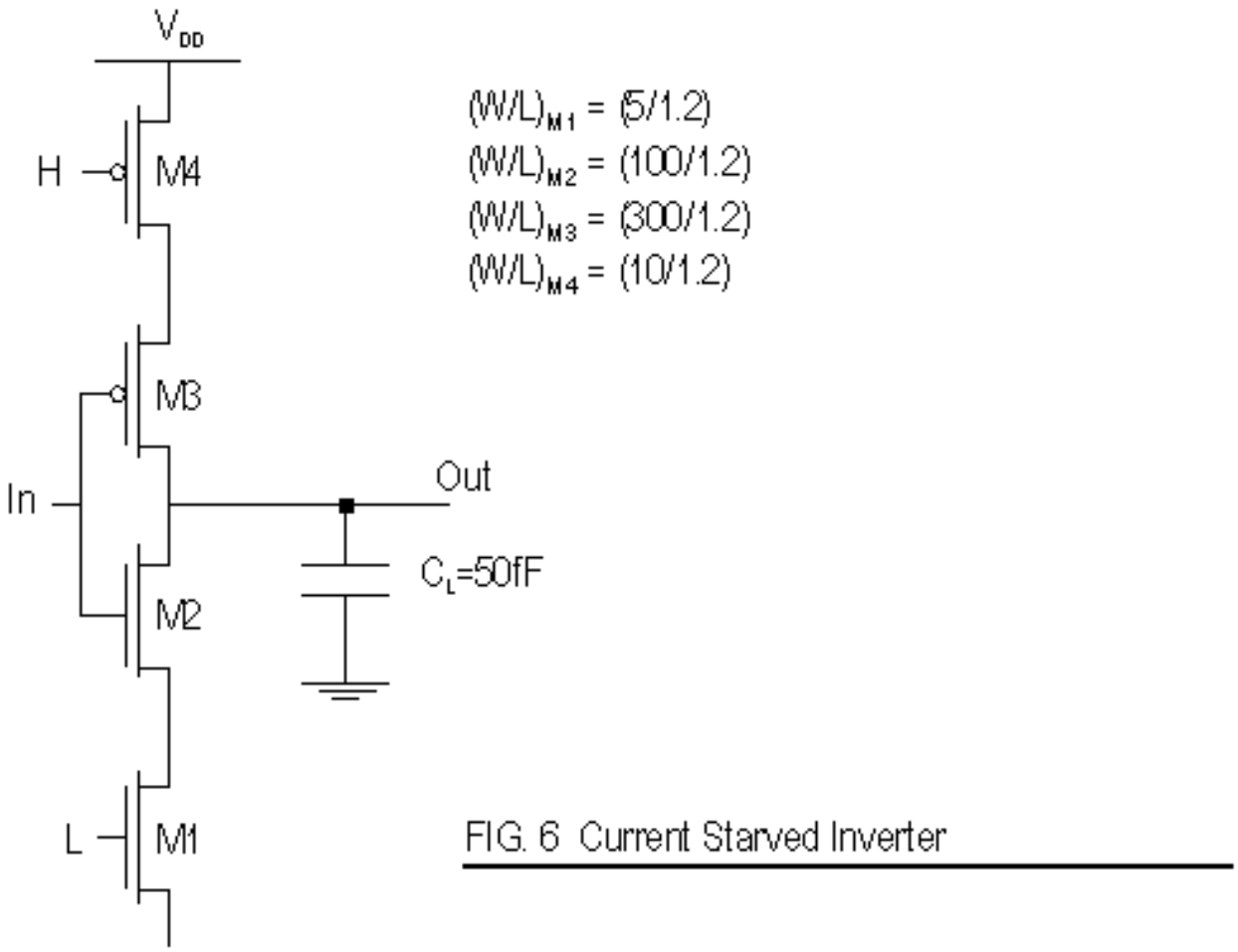
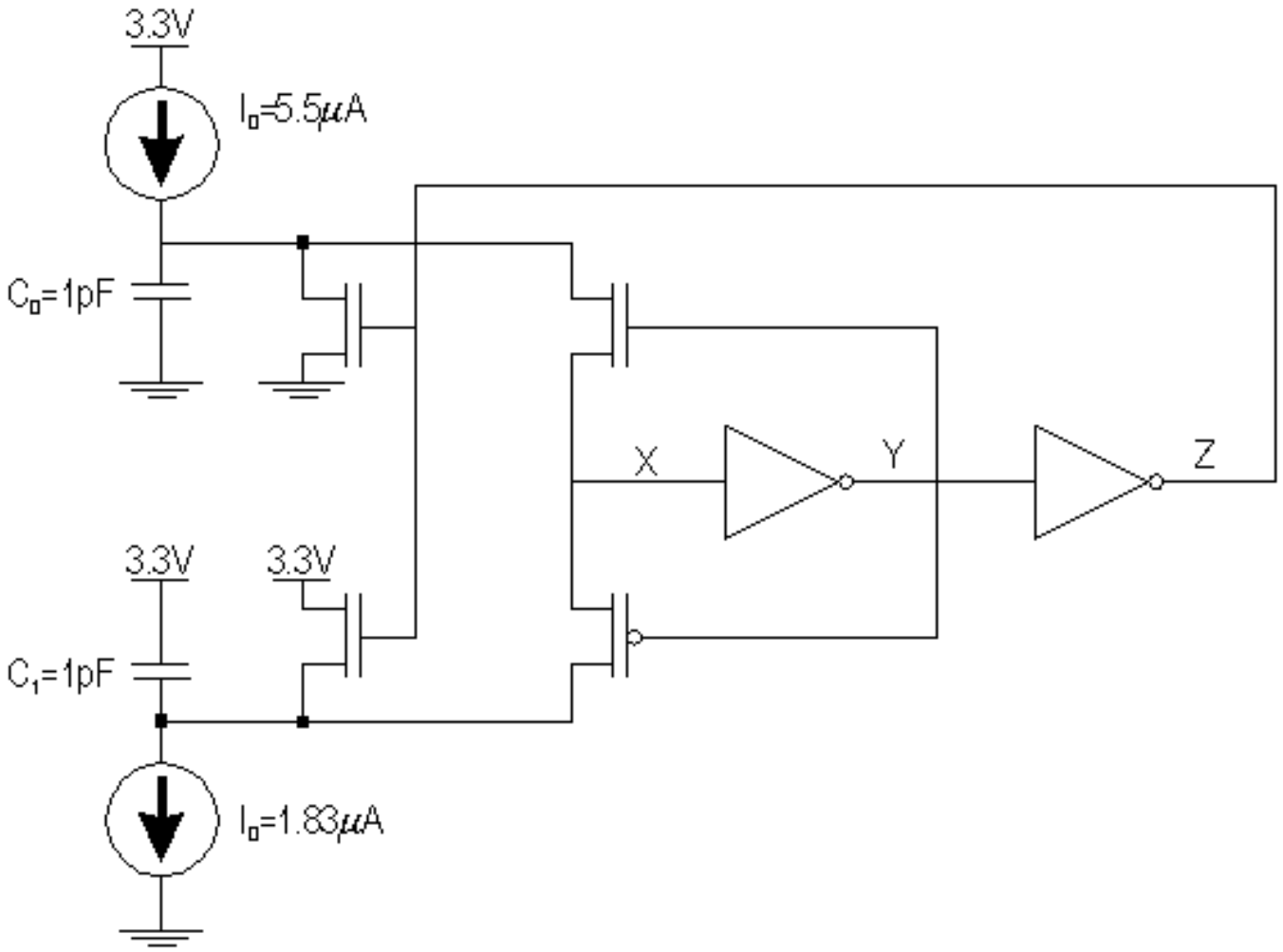


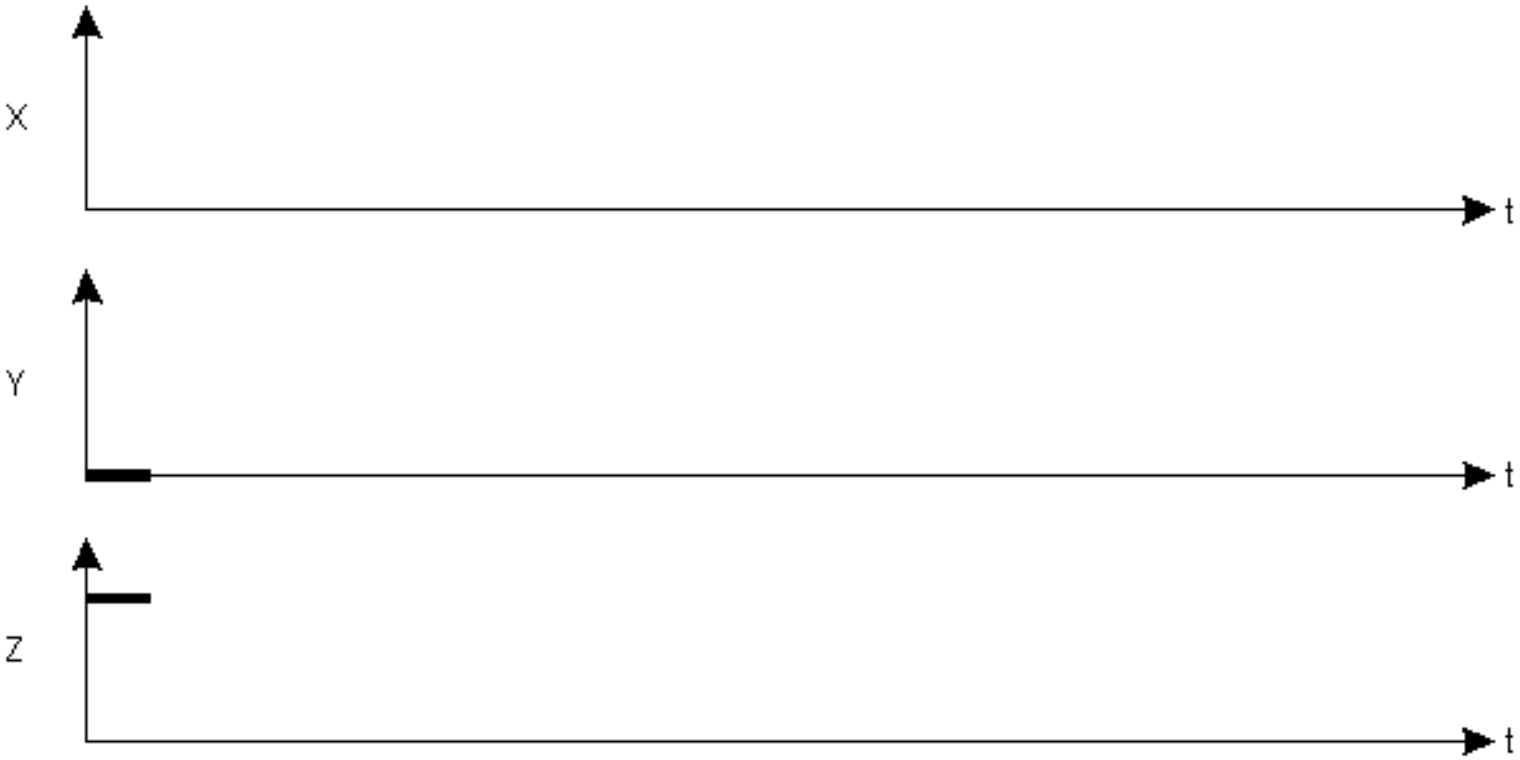
FIG. 6 Current Starved Inverter

H =	L =

b) The output waveforms of the shown inverter will have very slow rise and fall times (which will lead to high short circuit currents and power consumption). Discuss briefly how you would modify the circuit to eliminate this problem (while maintaining the oscillation frequency).

c) Not very happy with the obtained circuit, Amanda invents a new oscillator, shown below. Draw the signal waveforms for this innovative network. Determine the **oscillation frequency**. You may assume that the delay of the inverters, the resistances of the MOS transistors, and all internal capacitors can be ignored. The inverter switch point is set at 1.65 V.


3.3V
I_0=5.5μA
C_0=1pF
X
Y
Z
3.3V
3.3V
C_1=1pF
I_0=1.83μA


X
t
Y
t
Z
t

f_{osc} =