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EECS 141: SPRING 98 —MIDTERM 1

For all problems, you can assume the following transistor parameters:

NMOS:

$V_{Tn} = 0.75V$, $k'_n = 20\ \mu A/V^2$, $\lambda = 0$, $\gamma = 0.5\ V^{1/2}$, $2\Phi_F = -0.6V$

PMOS:

$V_{Tp} = -0.75V$, $k'_p = 7\ \mu A/V^2$, $\lambda = 0$, $\gamma = 0.5\ V^{1/2}$, $2\Phi_F = -0.6V$

NAME	Last First

GRAD/UNDERGRAD	

Problem 1:

Problem 2:

Problem 3:

Total	

Problem 1: Device Operation and DC characteristics

Consider the following simple logic gate:

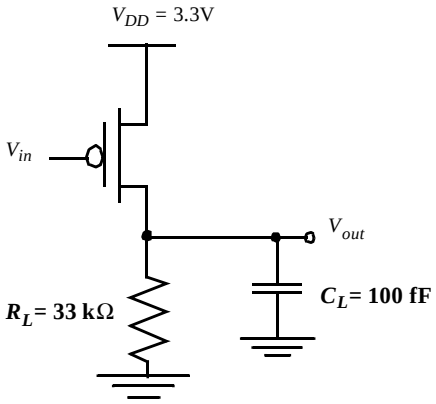
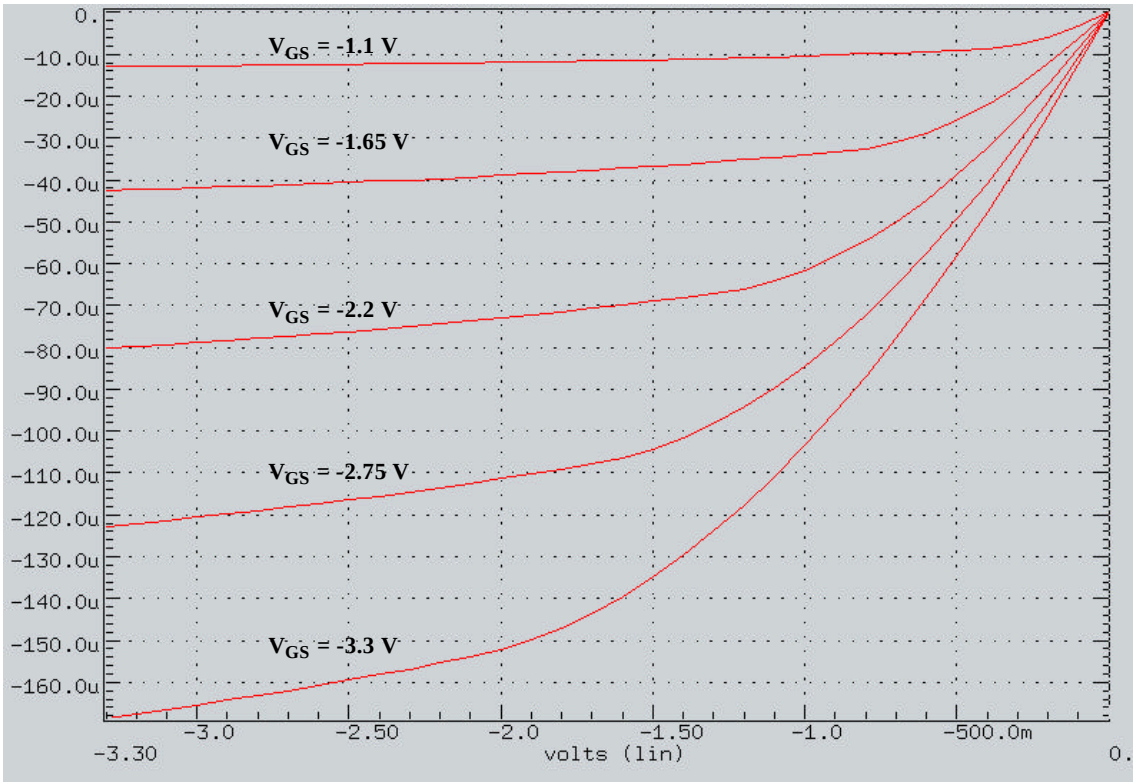


FIG. 1 : Simple Gate

The PMOS is implemented in a 0.35 µm CMOS process, and its I-V characteristics are plotted on the chart below.



Calculate answers to the following questions based only upon data points read from this plot. That is, do NOT attempt to solve by fitting analytical equations in Vgs and Vds to this data.

a. Determine approximate values of V_{OH}, V_{OL}, and V_M of the gate.

V_{OH}:
V_{OL}:
V_M:

b. Determine t_{pLH} and t_{pLH}. Assume an ideal step at the input.

***t_{pLH}*:**

***t_{pHL}*:**

c. Determine the static power dissipation of the gate in both the high and low output states.

***Pstat (Out = high)*:**

***Pstat (Out =low)*:**

d. Suppose that the bulk voltage of the PMOS is raised above VDD. Determine the impact on the following parameters and explain your answer in a couple of words:

Why?

VOH: Increase ☐ Decrease ☐ Unchanged ☐

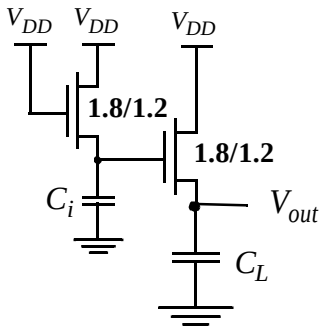
VOL: Increase ☐ Decrease ☐ Unchanged ☐

tpLH: Increase ☐ Decrease ☐ Unchanged ☐

tpHL: Increase ☐ Decrease ☐ Unchanged ☐

Pstat: Increase ☐ Decrease ☐ Unchanged ☐

PROBLEM 2: MOS Devices



Consider the following simple circuit (implemented in the 1.2 µm CMOS technology). Assume V_{DD} = 3 V. Assume that V_{out} is initially set at 0 V.

a. Determine the final value of V_{out} after the transients have subsided.

Vout (end of transient) =

b. Determine the energy taken from the supply during the transient. How much energy is dissipated in the two transistors?

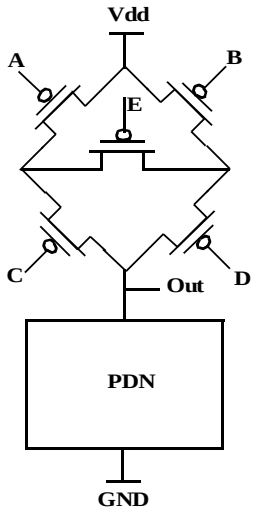
E(supply) =

E(transistors) =

c Assume that the NMOS devices represent real deep-submicron transistors. Discuss the voltage that the output will reach after we wait **for an infinite amount of time** after the initiation of the transient. Explain your answer.

Vout (t = ∞)

PROBLEM 3: Logic



Consider the logic gate given above.

a. Determine the logic function of the gate.

Out =

b. Draw the pull-down network (ensure that you use a minimum number of transistors.

c. Determine an ordering of the input signals, such that the PMOS network can be layed out a contiguous diffusion strip.

d. Size the PMOS transistors such that the resistance of the PMOS network is always equal or smaller then a single minimum-size PMOS device, yet is minimal in area.