University of California at Berkeley
Department of Electrical Engineering and Computer Science

EECS 141: Second Midterm Exam, Fall '96

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Please PRINT your name on each sheet. Write clearly.

Use the space provided to answer all questions. Use the back side if needed.

Name: _____
(last) (first)

SID: _____ Signature: _____

Transistor parameters:

	NMOS	PMOS
V_{T0}	0.75	-1.0
k'_n, k'_p	60 μA/V^2	20 μA/V^2
L_d	0 μm	0 μm

Neglect body effect and channel-length modulation.

Grades

Problem #1 (20 points)	
Problem #2 (20 points)	
Problem #3 (20 points)	
Total (60 points)	

Name:

Billbert and Filbert are designing circuits for a low-power application.

Problem 1. To prevent RACE conditions, Billbert uses NORA pipelined structures with C^2MOS latches.

1(a) Give one reason why each circuit might not work. (3+ 3points)

1(b) For each circuit specify one set of values for A, B, Φ, and $\overline{\Phi}$ that will result in a problem and highlight the corresponding logic path. (7+7 points)

Figure 1(a)

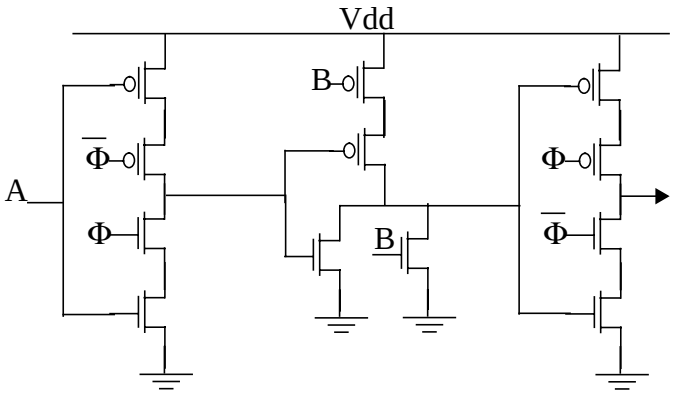
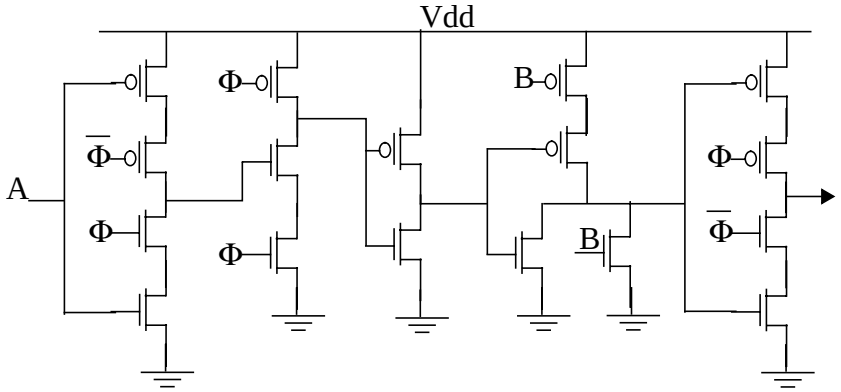


Figure 1(b)



Name:

Problem 2. Filbert generates the inverse clock using an inverter and finds that clock and clock-inverse are skewed by 0.6 ns (δ) as shown in Figure 2(a). All circuits in this problem use these clocks.

Consider the circuit in Figure 2(b). The minimum and maximum propogation delays of the inverters, logic and pass gates are — 0.1ns and 0.4ns (inverters); 0.8ns and 2ns (logic); 0.2ns and 0.4ns (pass gates). The duty cycle of the clocks is 50%.

Figure 2(a)

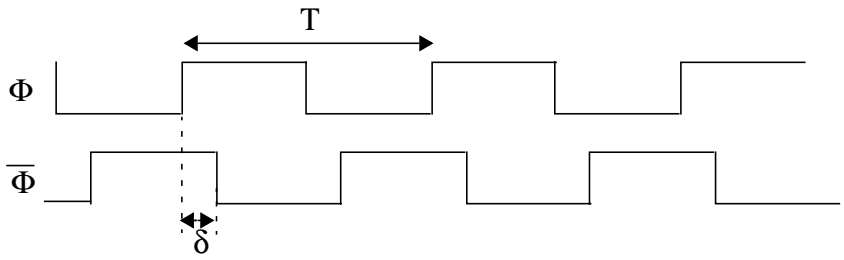
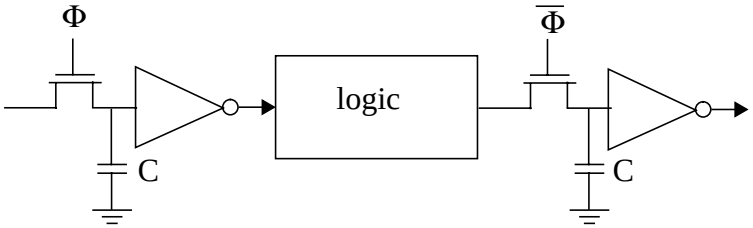


Figure 2(b)



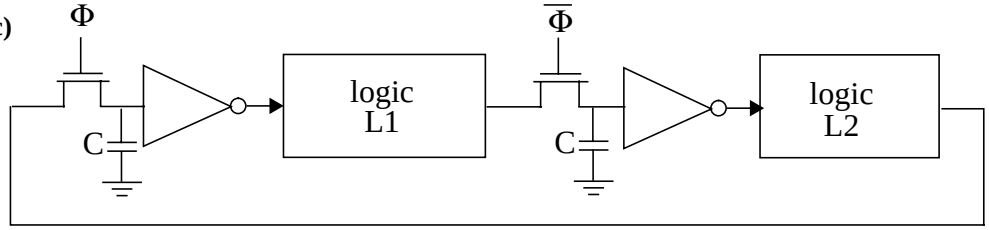
2(a) What is the minimum allowed clock period (T)? (6 points)

T_{min}:

Name:

2(b) Consider the circuit configuration in Figure 2(c). Given a 5ns clock period, what is the maximum allowed propogation delay of the logic block (L2)? Assume that the delay through L1 is unknown and the inverter delays are the same as in part (a). (6 points)

Figure 2(c)



T_{pL2}:

2(c) In order to avoid static power consumption in the inverter, Filbert uses zero V_T devices for the pass transistors. The problem with $0V_T$ transistors is the high subthreshold leakage. Assume that the subthreshold leakage through the $0V_T$ devices is 10 nA and ignore leakage in other devices. If the capacitance, C, is 50fF (Figure 2(b)), what is the maximum clock period at which there is no static power consumption in the inverter? (8 points)

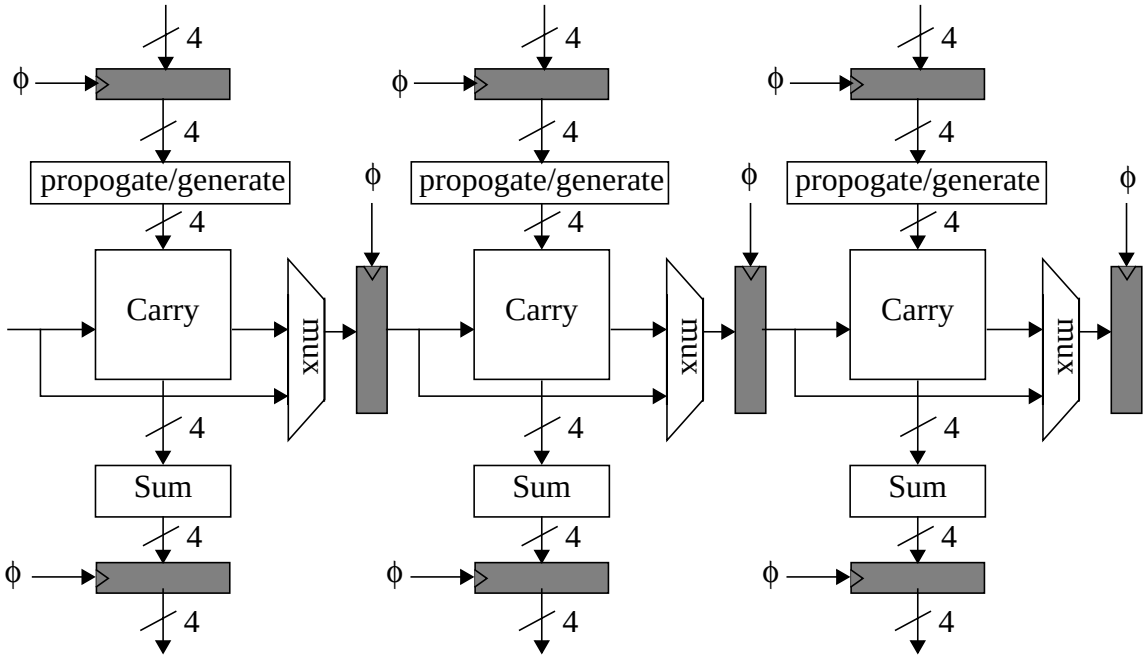
T_{max}:

Name:

Problem 3. Billbert designs a carry-bypass adder with 4 bits per stage but finds that it is too slow for large total number of bits. Being too lazy to go for a different design, he pipelines the adder using positive edge-triggered latches. A section of his circuit is shown below. Answer the questions (a) to (d) in terms of the total number of bits, N, and the following one-bit delays.

tp_{pg}	:delay though the propogate/generate block = 0.6ns
tp_{carry}	:delay of a single carry bit = 1ns
tp_{sum}	:delay of a single sum bit = 2ns
tp_{mux}	:delay of the multiplexor = 0.4ns
tp_{latch}	:delay of the latch = 0.5ns
tp_{latch_setup}	:setup time of the latch = 0.5ns

Figure 3(a)



3(a) What is the minimum clock period that Billbert can use for his N-bit adder? (i.e. throughput time). Give your reasoning for full credit. (7 points)

Is the clock period linearly dependent on the total number of bits, N? (3 points)

Name:

Clock Period:

3(b) How many clock cycles does it take for the first N-bit addition to complete? (i.e latency) (7 points)

Is the latency linearly dependent on the number of bits, N? (3 points)

Latency: