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EECS 141: Fall 95 – Midterm 2

For all problems, you can assume the following transistor parameters:

NMOS:

V_{Tn} = .75 V, $k'_n=\mu A/V^2$, $\lambda = 0$, $\gamma = .5\ V^{1/2}$, $2\Phi_F = -0.6V$

PMOS:

V_{Tp} = .75 V, $k'_p=\mu A/V^2$, $\lambda = 0$, $\gamma = .5\ V^{1/2}$, $2\Phi_F = -0.6V$

Bipolar NPN:

$\beta_F = 100$, I_S = 1.E-17 A, ϕ_T = 26mV, $V_{BE(on)}$ = 0.7 V, $V_{BE(sat)}$ = 0.8 V, $V_{CE(sat)}$ = 0.1V

For all problems, you may assume that the transistor lengths indicated are the effective lengths (L_{eff}) or, equivalently, that LD = 0.

Problem 1: Dynamic CMOS

In a recent ee141 project, I encountered the following ingenious dynamic circuit. It claimed to be solving the dynamic cascading problem without needing extra clocks or inverters. For your analysis you may assume that every node in the network represents a 10 fF capacitance, Each output signal (*Out1* and *Out2*) is loaded with an extra 10 fF wiring capacitance. All transistors are minimum size (3/2 for NMOS and 9/2 for PMOS).

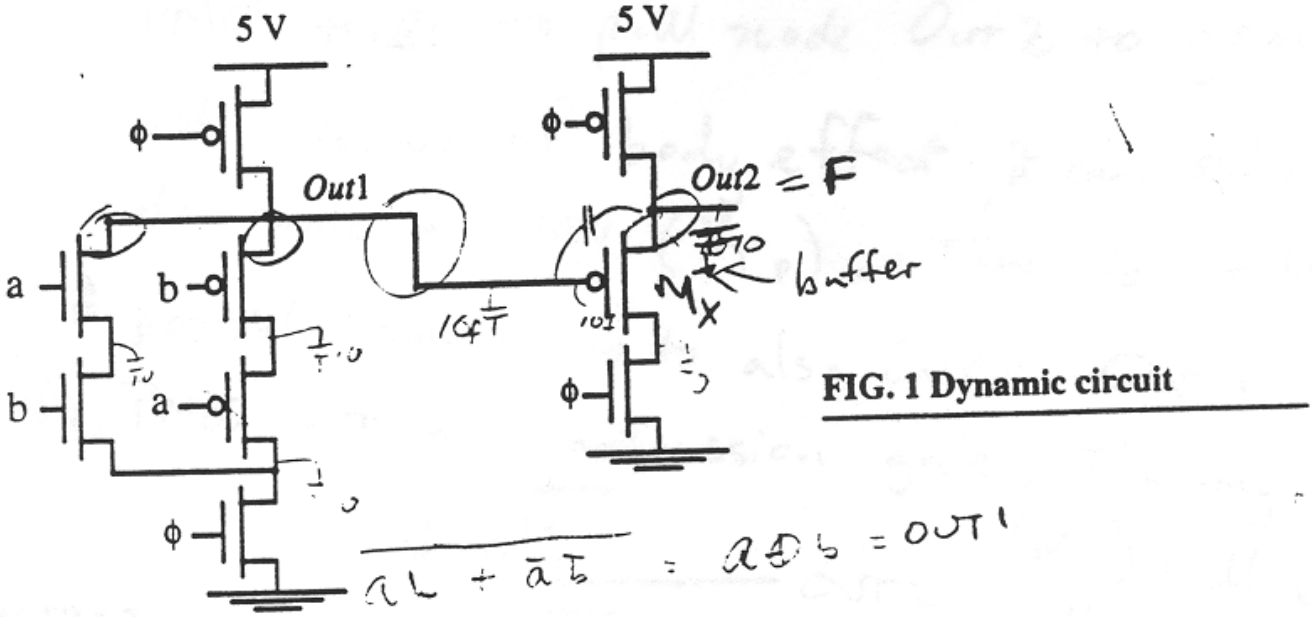


FIG. 1 Dynamic circuit

a. Determine the intended logic function of the gate.

F = **?**

b. Does this approach indeed solve the cascading problem? Explain your answer.

c. The circuit has two very important problems (besides the potential problem discussed in part b.). Define each problem, quantify it precisely (e.g., if you determine that the power consumption is too high, determine the value of the consumption), and propose a solution for the problem.

Problem 2: BiCMOS

The gate below has the advantage of being simple and reduces the number of bipolar transistors needed.

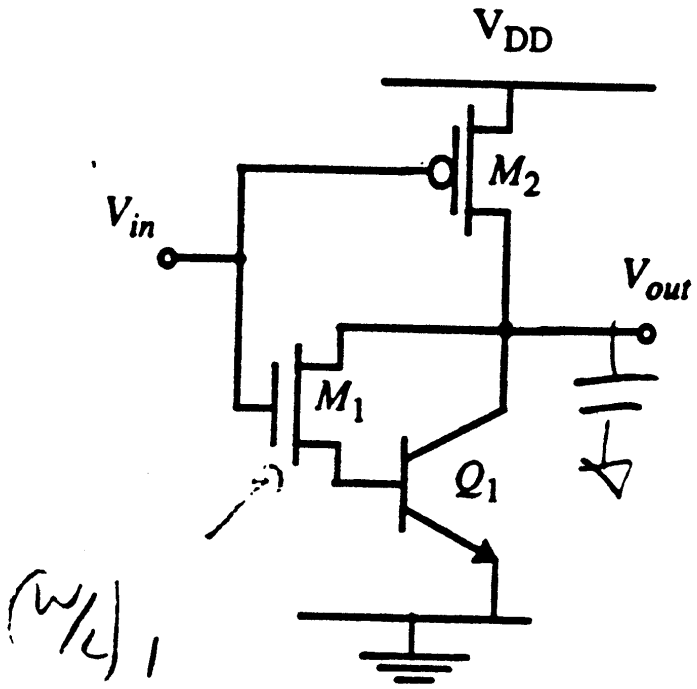


FIG. 2 : BiCMOS Gate

Determine the size of transistor M_2 such that the gate displays similar values for t_{pLH} and t_{pLH}. You may assume that the load capacitance is huge and dominates the performance. The bipolar transistor is minimum size, while the size of M_1 equals $(W/L)_1$. You may assume that the output swings from rail to rail. You may also assume that the MOS transistors stay in saturation during the transients. **Solve symbolically – and do NOT fill in any numbers.**

$(W/L)_{M2}$ = **?**

Problem 3: Merged CMOS/Bipolar current switch logic

Consider the following circuit.

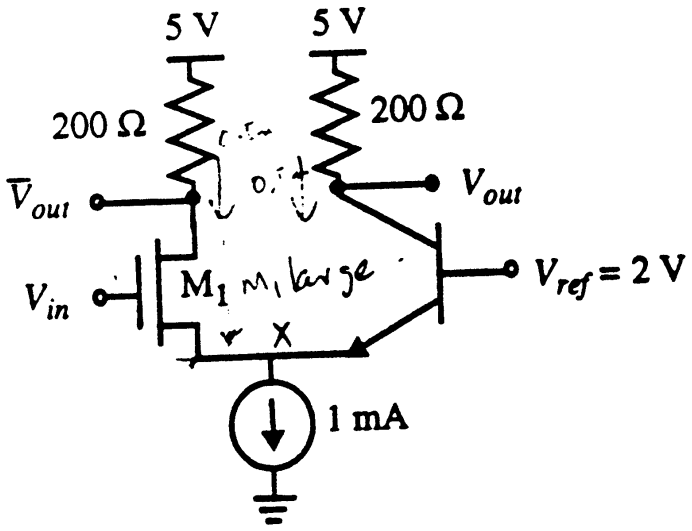


FIG. 3 : BiCMOS Gate

a. Determine V_{OH} (V_{in} = 5V) and V_{OL}(V_{in} = 0V).

V_{OH} = **?**

V_{OL} = **?**

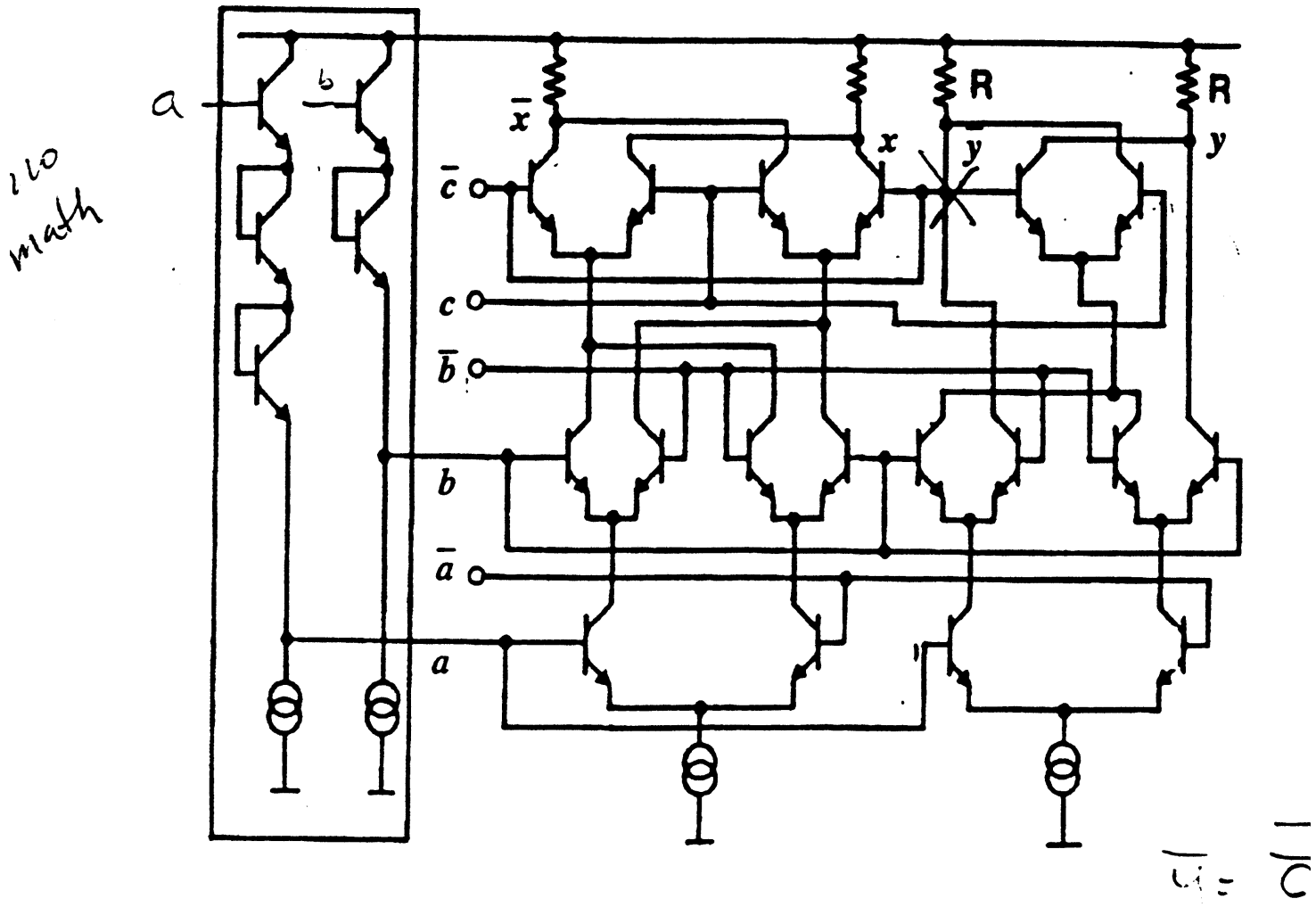
b. Determine the (W/L) of M_1 so that the output is precisely centered in the middle [V_{out} = (inverse of V_{out})] for V_{in} = 3V. BE PRECISE.

V_{in} = **?**

c. Give one example to illustrate why or where this gate could be useful.

Problem 4: Logic functionality

Determine the logic functions x and y, implemented by the circuit below. Explain the function of the circuitry in the box on the left.



x = **?**

y = **?**

Circuit in box on the left is needed for (pick one):

___ providing reference voltages

___ temperature compensation

___ level shifting

___ noise suppression
