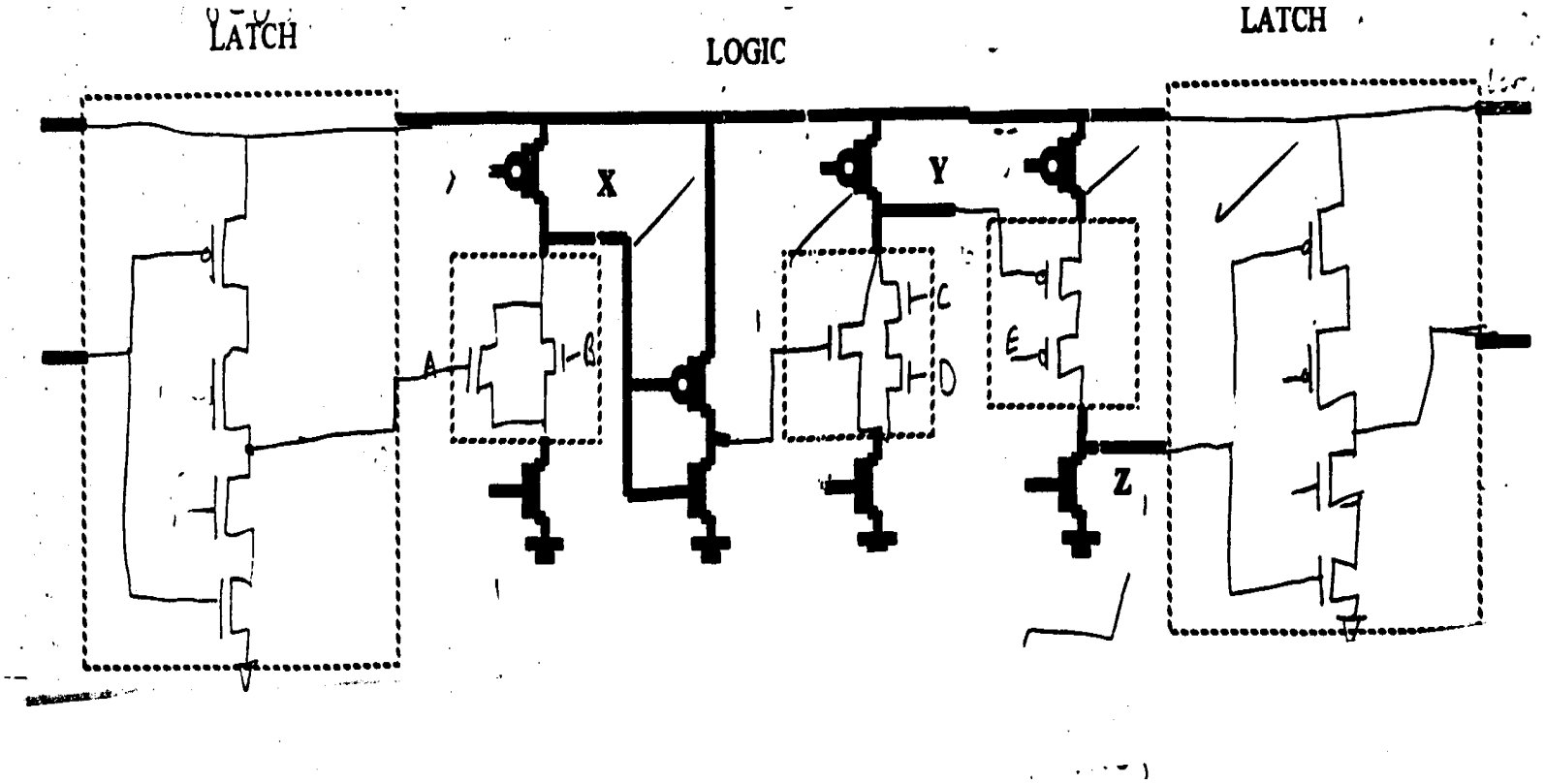
I. Dynamic Circuits and Latches

1a) For inputs, A, B, C, D, and E implement the following functions for the X, Y, and Z nodes by drawing the transistor circuits and specifying the inputs to the clock transistors (as phi or phi bar) in the dynamic logic circuit below. Use the convention that phi is high for evaluation. Do not consider the latches for part a).

X(bar) = A + B
Y(bar) = CD + X(bar)
Z(bar) = Y + E

1b) Provide latching for the dynamic logic below by placing the minimum number of latch circuits around the logic in the boxes provided and specifying inputs to the clock transistors. Assume only input A arrives through the latch on the input side.

1c) Consider the operation of this circuit, which among its four gates, includes a single static inverter stage. In the presence of clock overlap will this circuit operate correctly? Explain using the sequence of events which occurs for the case of phi going low before phi bar goes high.



II. Adders

IIa. Find carry input C_{ij}, output C_{oj}, the propogate P and generate G logic values associated with each bit in adding the following two 16 bit words. Assume the least significant bit is on the left as indicated by the bit number.

Bit= 0 1 2 3 4 5 6 7 8 9 ...

A = 1 0 1 0 0 1 0 1 1 1 1 1 1 0 0 0

B = 0 0 0 1 1 0 1 1 0 0 0 0 0 0 0 0

C_i = 0

Co =

P =

G =

Menu of Delays

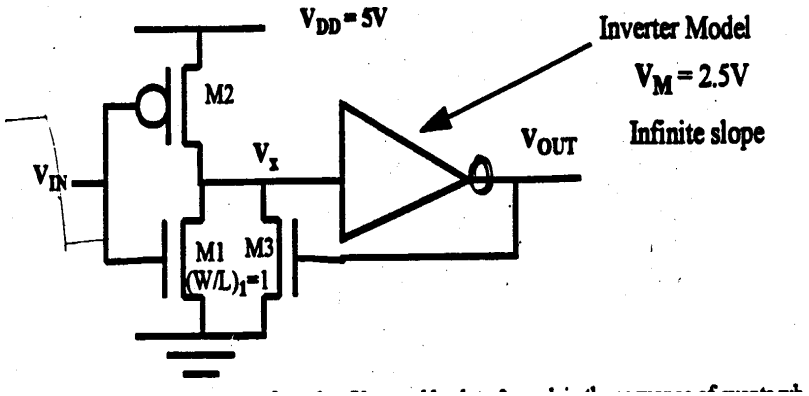
t_{setup}	$t_{propagate}$
t_{carry}	$t_{invert\text{-}carry}$
t_{sum}	$t_{invert\text{-}sum}$
t_{bypass}	$t_{invert\text{-}minimum}$
t_{mux}	$t_{project}$
$t_{generate}$	t_{degree}

IIb. For the above two code words find an algebraic expression for the delay in computing the output sum S_4 (really output of fifth bit) for a complementary CMOS ripple-carry adder. Use the menu of delays given above and assume the circuit of Figure 7.5 pp 389. Divide t_{carry} into $t_{carry\ bar}$ and $t_{invert\text{-}minimum}$ and t_{sum} into $t_{sum\ bar}$ and $t_{invert\text{-}minimum}$.

IIc. For these two code words find an algebraic expression for the delay in computing the output sum for the right most bit using a complementary CMOS carry-bypass adder with bypass length of 4 bits. Use the menu of delays given above and assume the circuit of Figure 7.5 pp 389. Divide $t_{carry\ bar}$ into t_{carry} and $t_{invert\text{-}minimum}$ and $t_{sum\ bar}$ into t_{sum} and $t_{invert\text{-}minimum}$.

IId. The complementary CMOS adder circuit in Figure 7.5 pp 389 has a worst case $t_{carry\ bar}$ which is probably about ten times larger than the delay $t_{invert\text{-}minimum}$ for a minimum sized inverter. Name two dominant physical effects which account for this slowdown and give a ball park estimate for the factor they individualy contribute.

III. Schmitt Trigger and Circuit Analysis



IIIa. As V_{IN} goes from 0 to V_{DD} and back to 0, explain the sequence of events which makes this circuit operate as a Schmitt trigger.

IIIb. Assume M3 is removed and find the minimum value of $(W/L)_2$ such that V_x is at 2.5V when V_{IN} = 3V.

IIIc. Now include M3 with $(W/L)_3$ = 5 if you do not trust your value from part b) and find the minimum value of $(W/L)_3$ such that when V_{IN} decreases from V_{DD} the output will switch at V_{IN} = 2.0V. Be sure to base your analysis on the model for the output inverter.