EE 141, Spring 1994
Midterm 2
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For all problems, you can assume the following transistor parameters:

NMOS:

V_{Tn} = 0.75V, k'n = 20μA/V^2, λ = 0.05, γ = 0.5 V$^{1/2}$, $2\Phi_F$ = -0.6V

PMOS:

V_{Tp} = -0.75V, k'p = 7μA/V^2, λ = 0.1, γ = 0.5 V$^{1/2}$, $2\Phi_F$ = -0.6V

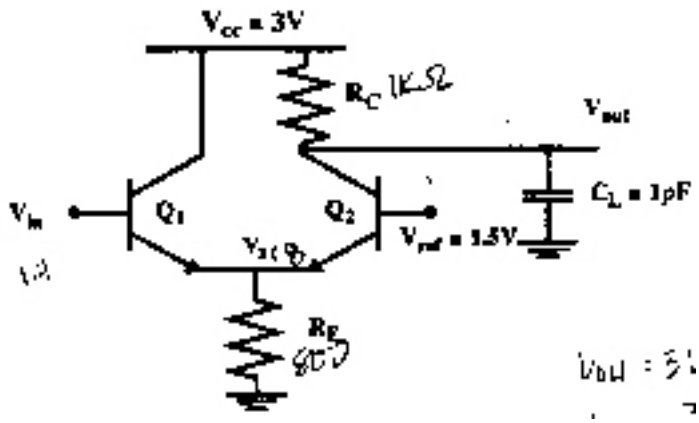
Bipolar NPN:

β_F = 100, $V_{BE(on)}$ = 0.7V, $V_{BE(sat)}$ = 0.8V, $V_{CE(sat)}$ = 0.1V

For all problems, you may assume that the transistor lengths indicated are the effective lengths (L_{eff}) or, equivalently, that LD = 0.

Problem 1: Bipolar Gate

A variant of an ECL gate is shown in FIG. 1.



a. Determine R_E and R_C such that the logic swing at the output equals 0.8V, while the maximum static power consumption of the gate equals 50mW. You may assume that the input swings between 1.1V and 1.9V.

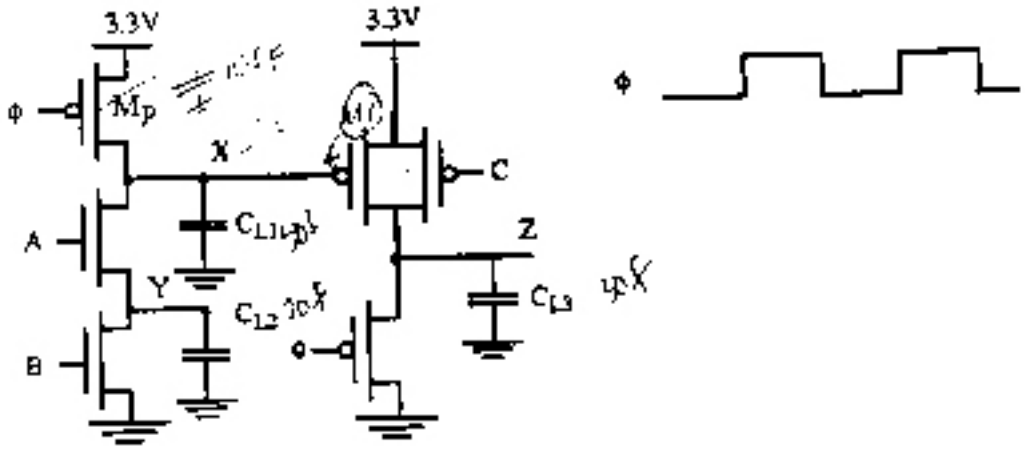
b. Determine t_{pLH}. You may assume that **all internal capacitances can be ignored (including diffusion and junction capacitors)** and that C_L is the only capacitance of interest. Assume the following values: V_{swing} = 1V, $V_{in(low)}$ = 1V, $V_{in(high)}$ = 2V, R_E = 800Ω, $R_{C = 1k\Omega}$.

c. Determine t_{pHL}. Use the parameter values of part b.

d. Will any of the two bipolar transistors ever saturate (for V_{in} between 0 and 3V)? Explain your answer.

Problem 2: Dynamic Circuits

In an attempt to save clock signals, student Jansen came up with a new logic style in his ee141 project, as shown in FIG. 2.



a. Derive the logic function implemented (at node Z).

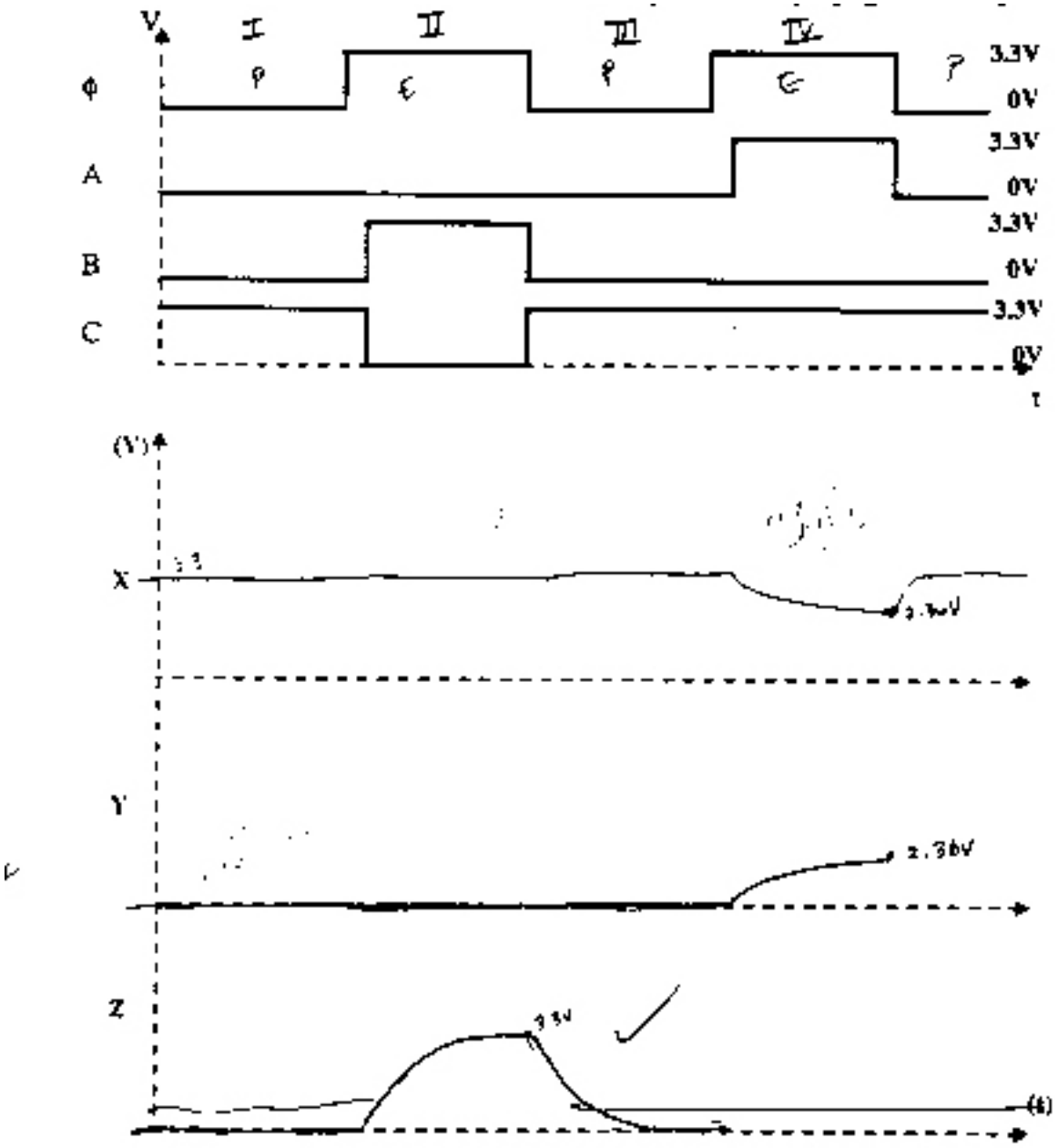
b. The precharge transistor M_p has a (fixed) gate-drain capacitance of 10fF. Draw the voltage waveform at nod X for A=B=0 and annotate the voltage levels (draw at least 2 periods and show the clock signal ϕ as well).

c. Assume that C_{L1}, C_{L2}, and C_{L3} equal 50fF, 20fF, and 50fF, respectively. The following waveforms are applied to thie inputs A, B, and C. Sketch the waveforms for nodes X, Y, and Z. Annotate the correct voltage levels. Do not worry about the propagation delays.

d. Although fast and simple, this circuit has some important problems. Describe under what circumstances the shown gate will not operate correctly (describe only the MOST IMPORTANT failure condition).

Problem 3: Transistor Sizing

FIG. 3 shows the NMOS pull-down network of a gate implemented in complimentary CMOS.



a. Derive the logic function Z. NO NEED TO SIMPLIFY THE RESULT.

b. Draw the schematics of the PMOS pull-up network. Hint: Use the Logic Graph approach introduced in Chapter 4.

c. Determine the transistor sizes such that the identical worst case rise and fall times are obtained, while minimizing the area. The minimum size NMOS device which can be used equals (1.8/1.2) and is denoted with a ratio "1".

d. Assume that all internal capacitors can be lumped into a single load capacitance $\mathbf{C_i}$ and that this load capacitance is proportional to the transistor sizes. Assume that the available (dis)charge current for the minimum area solution derived above equals $\mathbf{I_0}$. An external load capacitance $\mathbf{C_L}$ is connected to the output node. The input sources V_i can be assumed to be ideal voltage sources applying ideal step waveforms (between GND and V_{DD}).

-> Derive a symbolic expression for the propagation delay of the gate.

-> Assume now that all transistors are scaled upwards with a factor S. Derive the minimum possible value of the propagation delay and the corresponding value of S.
