EECS 141: SPRING 01 --MIDTERM 2

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The transistors in the following problems are minimum-length (0.25 um) devices fabricated in a 0.25 um process; the only model parameters you need are the zero-bias Vto and back-gate bias modified Vt threshold voltages:
NMOS: Vtno = 0.4 V, Vtn = 0.7 V;
PMOS: Vtpo = -0.4 V, Vtp = -0.7 V.
The supply voltage is Vdd = 2.5 V.

Problem 1. Static CMOS Logic

Consider the two complementary static CMOS gates shown below.

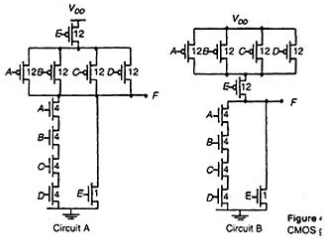


Figure 1

a) Do they implement the same logic function? What logic function(s) do they implement?

Yes ☐ No ☐

F1 =	F2 =

b) Considering the transistor sizes shown what is the worst-case input pattern (A-E) from a delay perspective for Circuit A, and, for Circuit B? Explain. Assume that an NMOS transistor has the same ON-resistance as a three times wider PMOS.

Circuit A

A=	B=	C=	D=	E=

Circuit B

A=	B=	C=	D=	E=

c) What are the worst-case popagation delays Tphl and Tplh? For which Circuit, A or B, and which input patterns do they correspond? Consider Reqn = 40k, Repq = 120k, Cdbn = Cdbp = Csbn = Csbp = 1fF for a unit transistor (W=L) and neglect the gate-overlap capacitance. Hint: draw in each case the equivalent RC network.

t_{pLH}=	Ckt	ABCDE=	t_{pHL}=	Ckt	ABCDE=

d) Consider that the inputs change in the following order: A, B, C, D, E. Which circuit performs better and why?

Ckt A ☐ Ckt B ☐

e) Give a more appropriate sizing of the transistors (in integer multiples) of Circuit A and B which improves the propagation delay.

PROBLEM 2: Dynamic Logic

For the dynamic CMOS gate shown in Fig. 2 and considering the waveforms specified (0-2.5V).

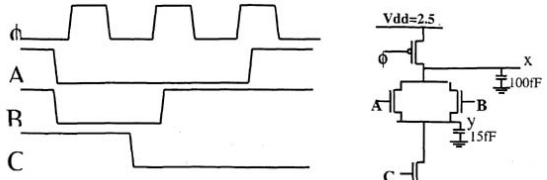
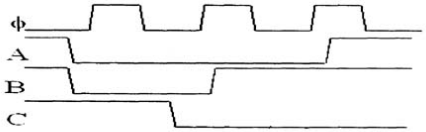


Figure 2

a) What is the logic function?

Fx =

b) Sketch the waveforms considering just the diffusion capacitances at nodes x, y, z; indicate the voltage levels for each waveform paying attention to back-gate bias when necessary.

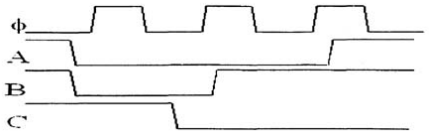


V_x

V_y

V_z

c) Now consider that Cgdo = 10fF of the clocking transistors cannot be neglected; draw the waveforms in this situation. You can neglect Cgdo for all other transistors.



V_x

V_y

V_z

d) For each of the three clock periods shown estimate the delta V on the rising (1+, 2+, 3+) and the falling edge (1-, 2-, 3-) at x and z taking into account Cgdo of the clocking transistors.

ϕ	1+	1-	2+	2-	3+	3-
ΔV_x						
ΔV_z						

e) Is there an upper limit for |delta V|? Explain.

|ΔV| =

f) What is the average power dissipation of this circuit if it is clocked at f=500MHz? Consider the switching probability. Assume all inputs have equal probability of 0 or 1.

P_{av} =

Problem 3. Pass transistor logic.

A CPL implementation of a circuit for a very common arithmetic block is shown in Figure 3.

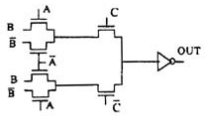


Figure 3

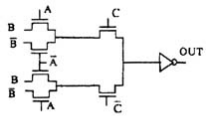
a) What is the logic function implemented and for what arithmetic block can it be used?

F_{OUT} =

b) All input signals are 0-2.5V and Vdd = 2.5V; show the voltage levels for a logic "0" and "1" at nodes x, y, and OUT;

Input	Vx	Vy	Vout
Logic 0			
Logic 1			

c) Suggest a circuit change to improve the noise margins of this circuit; draw your solution on the circuit diagram below.



d) Draw a pass-transistor circuit implementation of this function using both N- and PMOS transistors; does the solution in c) above apply to this new implementation?

e) Which solution, c) or d) is preferable and why?
