EECS 141: Fall 1992 - MIDTERM 2

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For all the problems, you can assume the following transistor parameters:

NMOS:

V_{Tn} = 0.75V, Kn = 20 uA/V^2 , LAMBDA = 0.05, GAMMA = 0.5 $V^{1/2}$, $2PHI_F$ = -0.6V

PMOS:

V_{Tp} = -0.75V, Kp = 7 uA/V^2 , LAMBDA = 0.1, GAMMA = 0.5 $V^{1/2}$, $2PHI_F$ = -0.6V

NPN:

B_F = 100, $V_{BE(on)}$ = 0.7V, $V_{BE(sat)}$ = 0.8V, $V_{CE(sat)}$ = 0.1V, $I_S = 10^{-17}$A

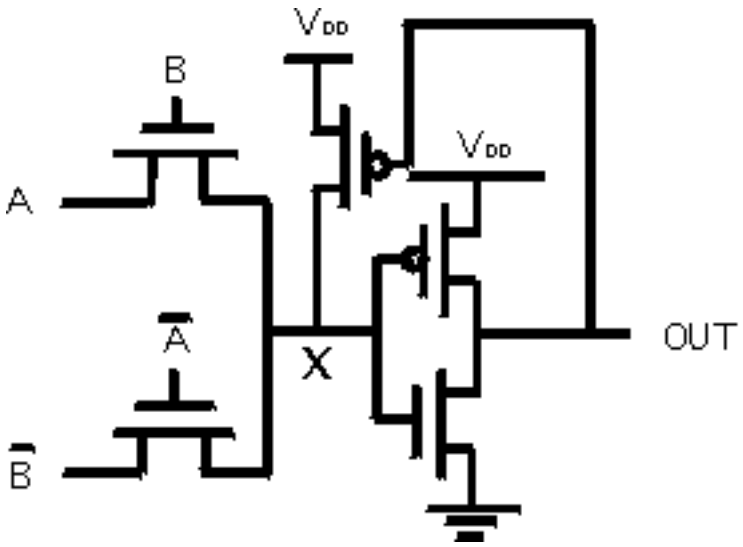
For all problems, you may assume that the MOS transistor lengths indicated are the effective lengths (L_{eff}) or, equivalently, that LD = 0.

Problem 1: Logic Gates

The circuits shown below have a major problem. For each of those circuits,

a). Determine its logic function.
b). Explain the problem.
c). Redraw the circuit such that the problem is solved. Try to keep the number of changes minimal (e.g. if a circuit is dynamic, keep it such). Also, stick to the available input signals.

Circuit 1:



a). Logic function:

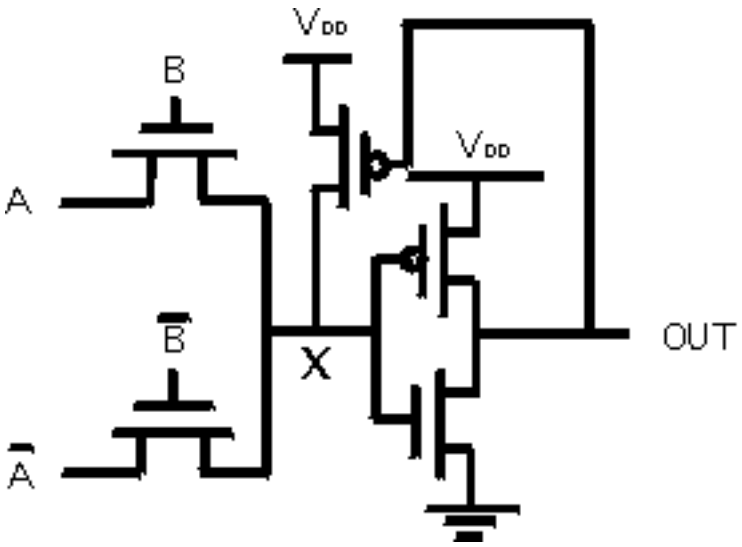
A	B	X	OUT
0	0	1	0
0	1	0	1
1	0	?	?
1	1	1	0

OUT = $A \oplus B$ or OUT = $A\bar{B}$ (depending on what you want "?" to be)

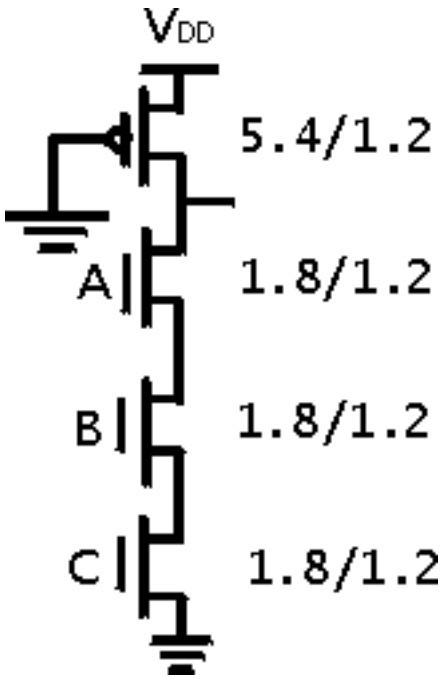
b). The problem:

Node X is not driven by input when B=0 A=1, so X will keep its previous value.
Need to make sure X is driven by one and only one input at all times.

c). Redrawn Circuit:



Circuit 2:



a). Logic Function:

$$OUT = \overline{ABC}$$

b). The problem:

PMOS W/L too large compared to 1/3 NMOS W/L.
So V_{OL} will be very high.

Want $R_{PMOS} >> R_{NMOS} + R_{NMOSB} + R_{NMOSC}$

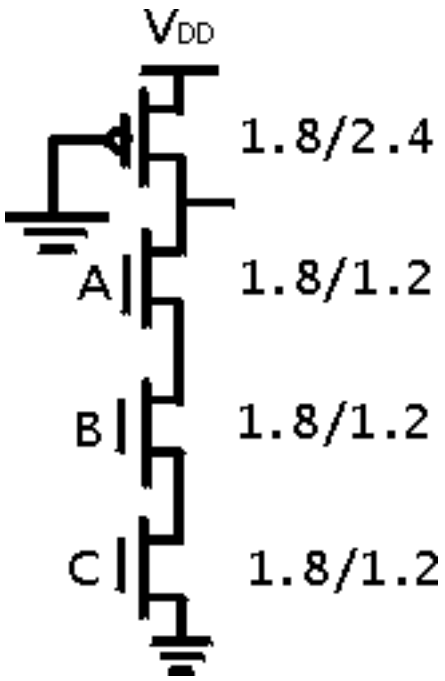
--> $1/(u_p) \times 1/(W/L|_p) >> 3/(u_n \times W/L|_n)$ $u_n/u_p \sim 1.8/2.4$

--> $W/L|_p << W/L|_n$ so say $W/L|_p = 1.8/2.4$

Ideally, we'll set the ratio to make $V_{OL} < V_{Tn}$

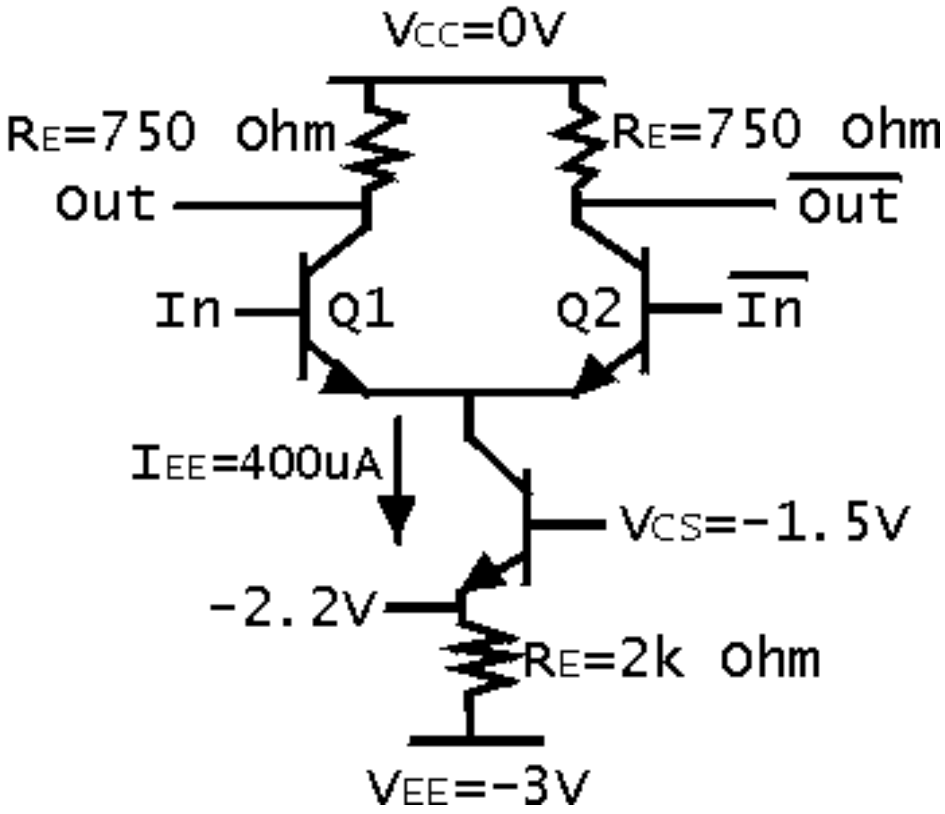
Note: It is true that t_{PHL} and t_{PLH} are asymmetric, but this is almost always true for pseudo NMOS. It is not correct to set $R_{PMOS} = R_{NMOSCHAIN}$ because then $V_{OL} = V_{DD}/2$.

c). Redrawn Circuit:



Problem 2: Differential Current Mirror Logic

A differential CML gate is shown below.



a). Determine the important points of the VTC (V_{OH}, V_{OL}, V_{IH}, V_{IL} and V_M). For the computation of V_{IH} and V_{IL}, you can use the simplified definition (V_{IL} is defined as the point where the transistor Q1 is carrying 1% of the current through the current source, while at V_{IH} transistor Q1 carries 99% of the total current).

V_{OH}, V_{OL}: Assume the current in Q1 and Q2 is I_{EE} or zero.
Current = 0 --> $V_{OH} = V_{CC} = 0$
Current = I_{EE} --> $V_{OL} = V_{CC} - I_{EE}R_C = -0.30V$

V_M: This is a symmetric differential circuit, so $V_M = (V_{OL} + V_{OH}) / 2 = -0.1V$

V_{IH}, V_{IL}: Remember, this isa differential circuit, so In and In changes.
When $V_{In} - V_{In} = 120mV$, $I_{C1} = 100\ I_{C2}$
So, $V_{IH} = V_M + 60mV = -0.09V$
$V_{IL} = V_M - 60mV = -0.21V$

b). Assume that the output **Out** connects the input terminal of 5 identical gates (or has a fanout of 5). Recompute the values of V_{OH} and V_{OL} under these conditions.

When an ouput is low base current inot load = 0.
So V_{OL} stays at -0.30V.

When output is high, each load draws base current = 400mA/B_F = 4mA

So, V_{OH} = 0 - 5 x 4mA x 750Ohm = -0.015V

c). Assume that the capacitance to the outputs of the gate equals 40fF and that there are no other capacitors in the circuit. You can ignore Q_F. Compute the power consumption of the gate. Assume that the input is high 50% of the time and makes a transition (L -> H or H -> L) every 5 nsec. Assume that the input is high for 50% of the time.

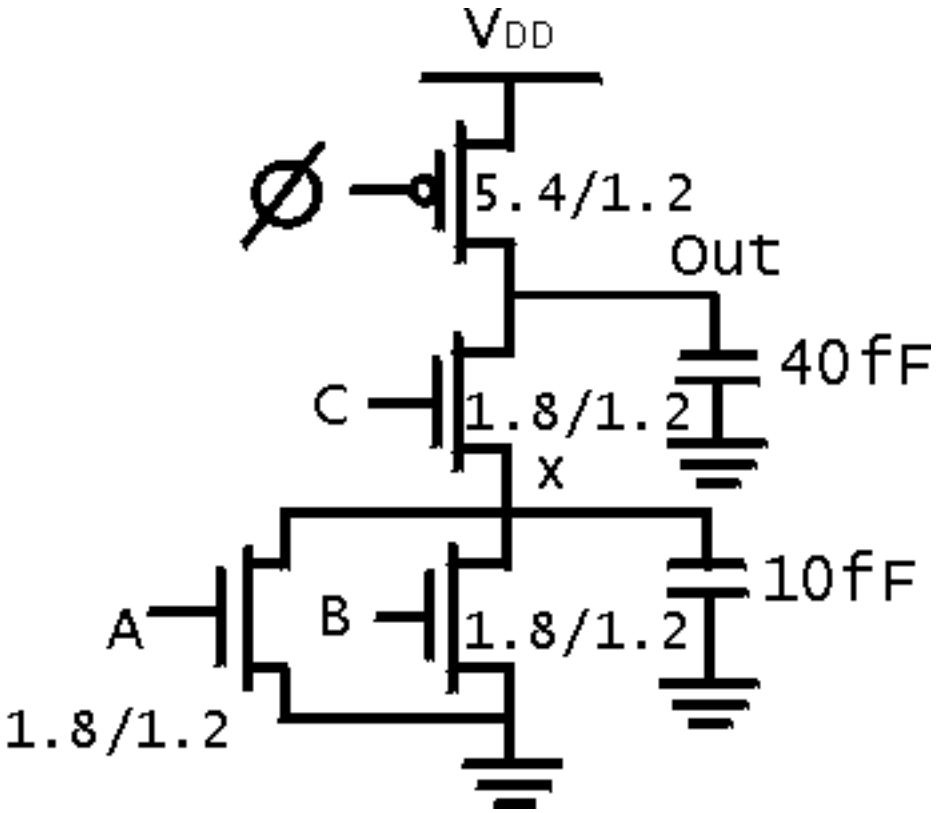
$P_{static} = I_{EE} (V_{CC} - V_{EE}) = (400uA)(3V) = 1.2mW$

$P_{dynamic}$: with each transition, one 40fF capacitor is charged.
Energy/Transition = $(V_{CC} - V_{EE})(V_{OH} - V_{OL}) C_L = (3V)(0.3V)(40fF) = 36fJ$
Hence, $P_{dynamic} = 36fJ/5nsec = 7.2uW$

$P_{total} = P_{static} + P_{dynamic} \sim P_{static} = 1.2mW$

Problem 3: Dynamic CMOS

After taking EE141, a student figured out that dynamic circuits were way too complex and came up with his "new" dynamic style called BDL (for Berkeley Dynamic Logic). A gate in this logic style is shown in the Figure below.

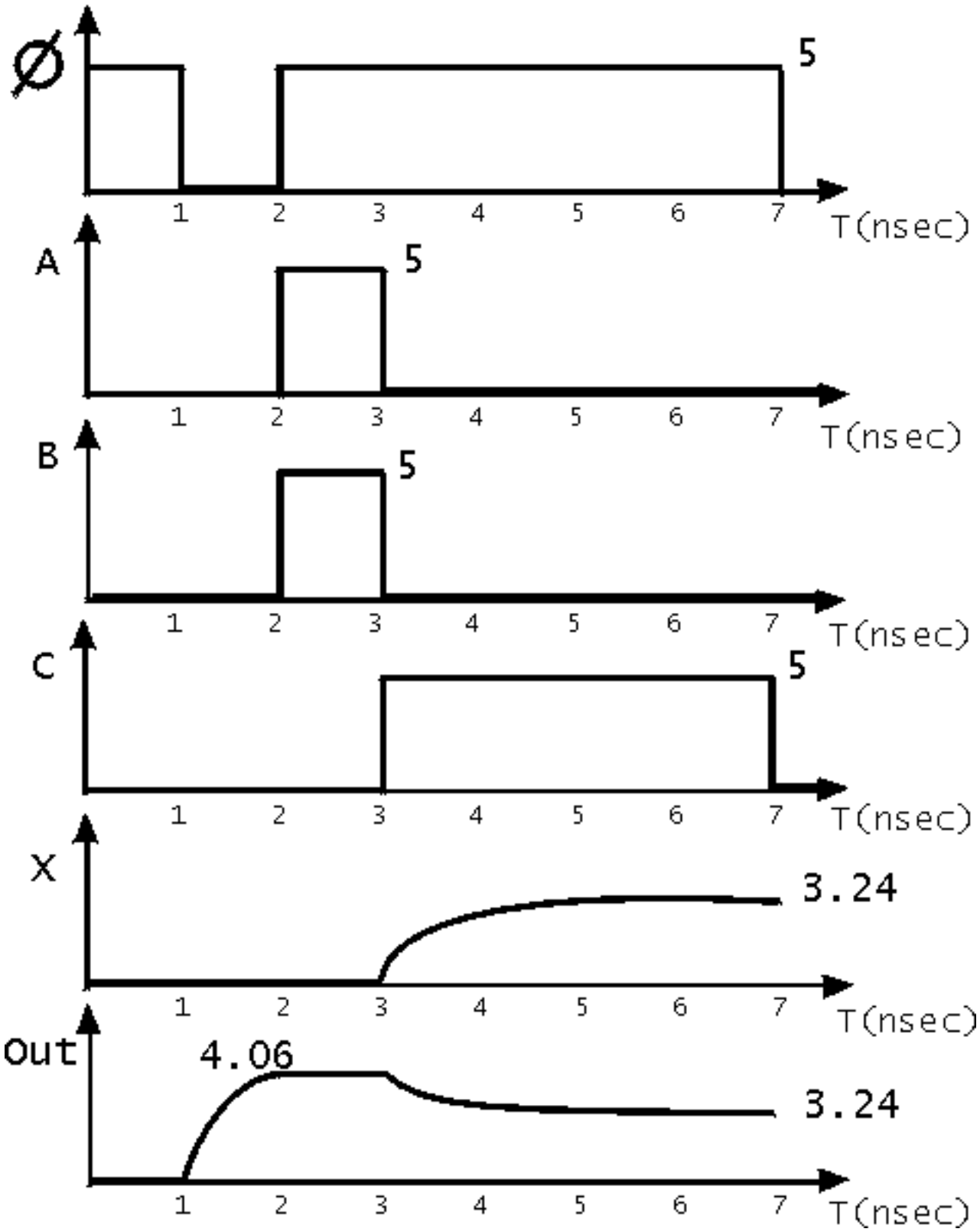


a). Is this circuit going to work under all conditions? If not, explain why and give a case when this circuit is not going to work.

> No. If inputs are high during precharge, the output will fail to precharge to V_{DD} . (Why would inputs be high during precharge? Well, if you use "BDL" in domino or np CMOS, that could happen.)

b). Given the set of input waveforms, shown on the next page, draw the voltage waveforms for both the intermediate node **X** and output **Out**. Both have an initial value of 0V. Determine the voltage levels precisely and mark them on the drawing. You may assume that all input signals change abruptly. All capacitances have been lumped and their values have been annotated on the Figure above. To compute the transient response, you may assume that all transistors (NMOS and PMOS) can be modeled as linear resistors with a value of 15kOhm. Assume that C_{GS} and C_{GD} = 0 for all transistors.

V_{out}(2nsec) = 4.06	V_{out}(3nsec) = 4.06	V_{out}(7nsec) = 3.24



t = 1ns -> 2ns: 40fF charging through PMOS at **Out;** no charge at **X** (floating)
Vout = 5(1 - exp(- (t-1ns)/(15kOhm x 40fF)))
Vout(2ns) = 5(1 - exp(-1ns/0.6ns) = 4.06

t = 2ns -> 3ns: Output floating -> no change in voltage
X tied to ground -> no change in voltage.

t = 3ns -> 7ns: Charge is shared from Out to X.
Equilibrium voltage = (40/40+10) (4.06) = 3.24V
After 4ns, should be very close to equilibrium.

c). TRIVIA: Are the Following Statements TRUE or FALSE?

T	F	
x		Clock Feedthrough Can be Reduced by Reducing the Size of precharge Transistor.
	x	NAND logic is preferred over NOR logic in dynamic Gates with NMOS PDN.
x		Implementing a NAND function is Not possible in DOMINO.
	x	Dynamic Logic is the Logic Style with the Smallest Number of Transistors
	x	The Propagation Delay of a Dynamic Gate is Linear with Respect to Fanin.
x		Clock FeedThrough Can Hurt the Power Consumption.
		Increasing the Fanout of a Dynamic Gate Does Not Affect the Noise Margins.
	x	Dynamic Logic is Often Used in Portable Cameras for Its Low Power Consumption.