EE130 Midterm #1 Fall 1998
Professor: C. Hu
Closed book; One sheet of notes allowed.

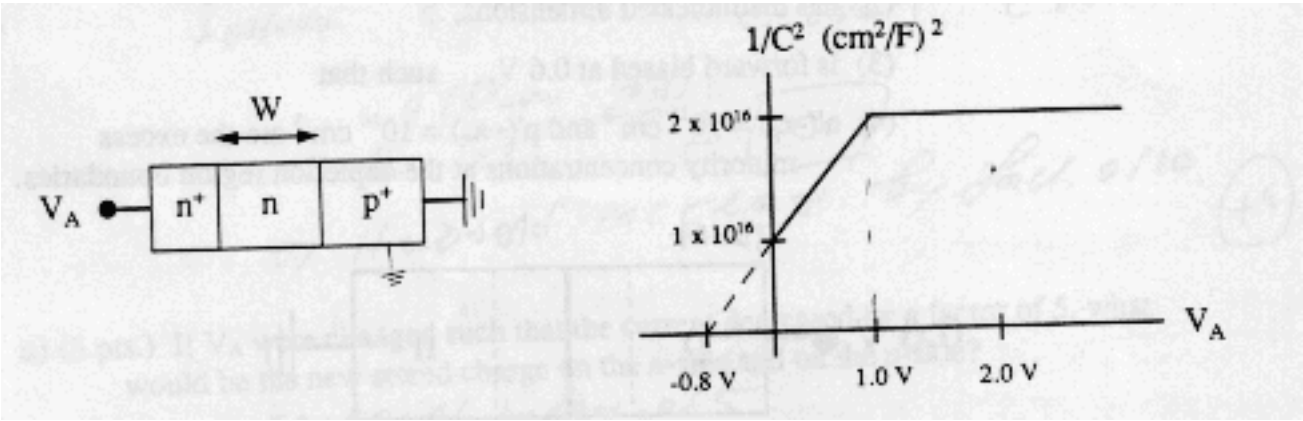
1. (16 pts) Consider a semiconductor for which:

ni = 10^13 /(cm^3)
mp = mo = 25 mn
fixed mean scattering times taucn = taucp = 10^-12 s.
Nd = 0.

a) 3pts. What is the ratio of electron and hole mobilities, mu(sub n) / mu(sub p)
b) 10pts. Determine the acceptor concentration Na that would minimize total conductivity sigma.

c) 3pts. What is the electron diffusion coefficient Dn at room temperature?

2. (18 pts) Consider the plot of 1/(C^2) vs. applied voltage Va fro the silicon n+ np+ diode pictured below. Doping concentrations are uniform throughout each of the n+, n and p+ regions.



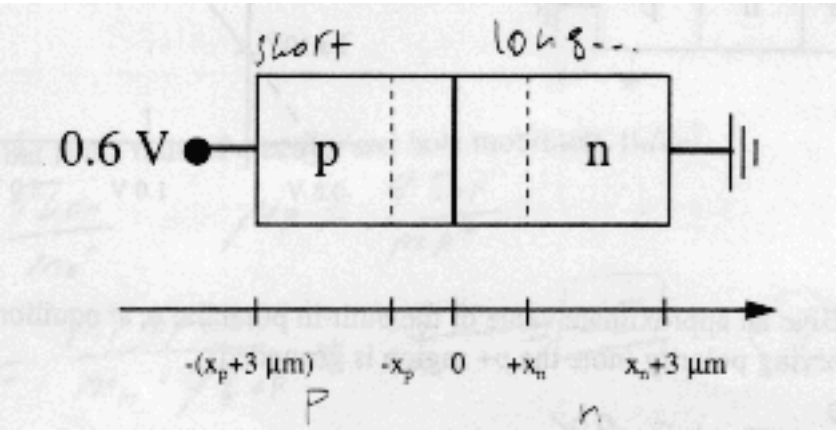
a) 2pts. Give an approximate value of the built-in potential phi sub i at equilibrium, while observing polarity. note that the p_ region is grounded.

b) 3pts. What is the depletion width xsubd at equilibrium?

c) 8pts. What is the maximum electric field in the diode at Va = 0V?
You may make appropriate approximations given the diode is a one-sided junction.

d) 5pts. Determine the width W of the sandwiched n-region.

3. (30 pts) Consider the Si pn diode illustrated below. The diode is:
1. at room temperature
2. has the indicated dimensions.
3. is forward biased at .6V, such taht
4. n'(-xp) = 10^15 cm^-3 and p'(+xn) = 10^14 cm^-3 are the excess minority concentrations at the depletion region boundaries.



a) 7pts. You are given Lp = 100 microns on the n-side and Ln = .1 microns on the p-side. Compute the stored minority charge densities (C/cm^2) on the n-side and on the p-side

(Hint: make appropriate approximations given the sizes of Lp and Ln relative to the diode dimensions).

b) 6pts. You are asked to modify the diode design so as to improve its switching speed (i.e. reduce the stored charge for a given current).

Suggest two changes you would make. Number the changes #1 and #2 according to their effectiveness.

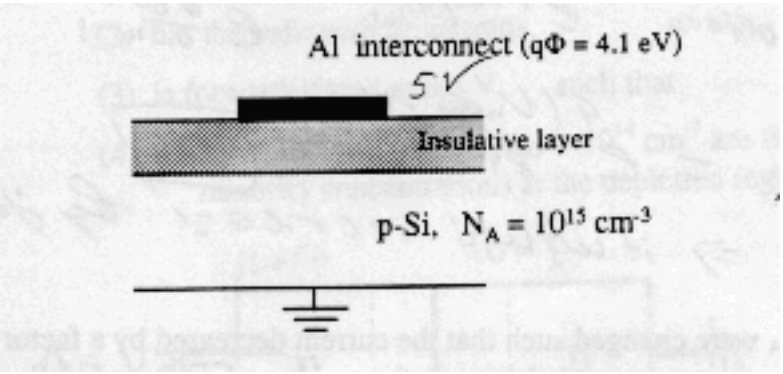
c) 5pts. If Va were increased to .66 V by what factor would the current I increase?

d) 5pts. If Va were changed such that the current decreased by a factor of 5 what would

be the new stored charge on the n-side and on the p-side.

e) 7pts. If both n and p sides of the diode were shortened by 1 micron, by what factors would abs(Jn(-xp)) and abs(Jp(xn)) change?

4. (36 pts). Metal interconnect lines in IC circuits form parasitic MOS capacitors as illustrated below. Generally one wants to prevent the underlying Si substrate from becoming inverted.



a) 6pts. Find Vfb for the parasitic MOS capacitor.

b) 8pts. If the interconnect is at 5 V, what is the minimum capacitance (F/cm^2) of the insulative layer to prevent inversion?

c) 4pts. If for fabrication considerations the insulative layer thickness must be 1 micron, what should be the dielectric constant K = epsilon/epsilon not of the insulative material to make Vt = 5V.

d) 3pts. Is the answer in (c) the minimum for maximum allowable K to prevent inversion?

e) 5pts. At Vg = Vt + 2V (Vt = 5V) what would be the area charge density (C/cm^2) of an inversion layer.

f) 6pts. At Vg = Vt = 5V what would be the high-frequency MOS capacitance (F/cm^2)?

g) 4pts. At Vg = Vt + 2V (Vt = 5V) what voltage is dropped across the insulative layer?