EECS 130, Fall 98
Final Exam
Professor C. Hu

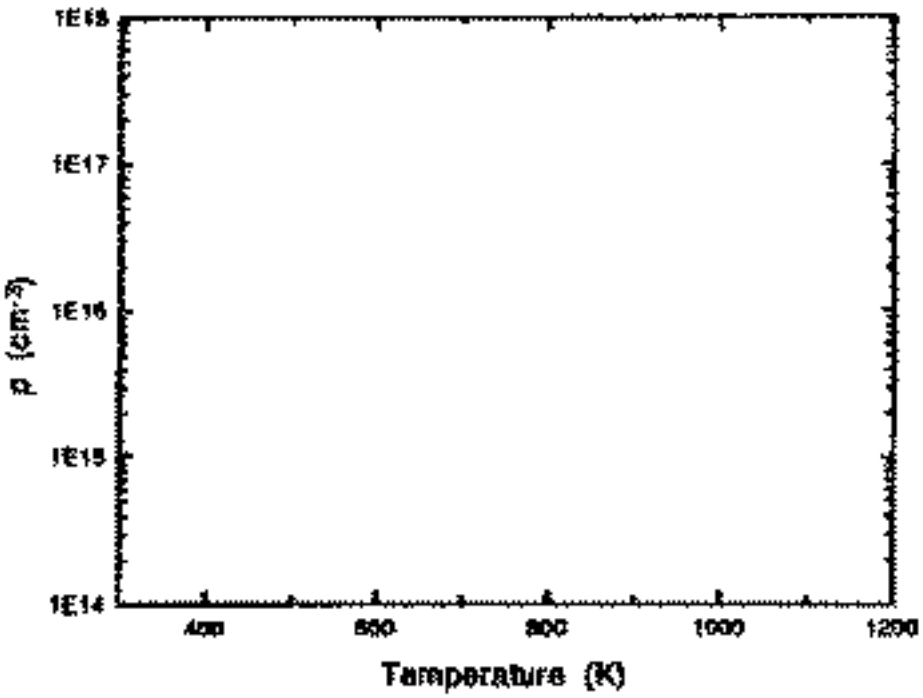
Problem #1

(25 pts.) A silicon sample is doped with boron atoms to $N_A = 10^{15}$ cm.

a) (3 pts.) What are the electron *n* and hole *p* concentrations at room temperature?

b) (4 pts.) What are *n* and *p* at *T* = 600 K to within an order of magnitude?

c) (4 pts.) Sketch $\log_{10}(p)$ versus temperature between 300K and 1200K on the axes below.



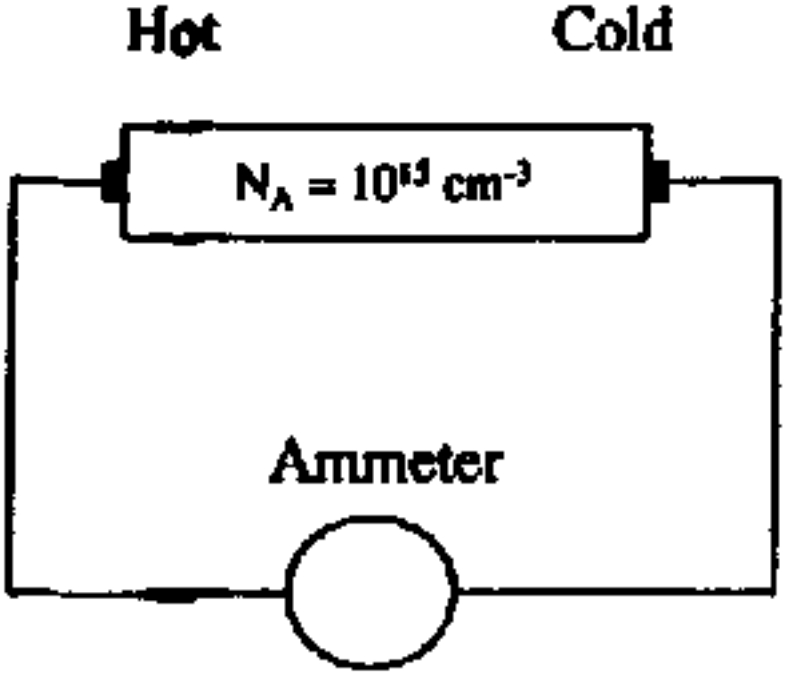
d) (4 pts.) Consider a GaAs sample (E_g = 1.4 eV) also doped with $N_A = 10^{15}$ cm^{-3}.
Using a dotted line, add a 2nd curve to the axes in part (c) showing $\log_{10}(p)$ vs. *T* for the GaAs sample.

e) (3 pts.) GaAs is preferred over Si for high-frequency transitors. What semiconductor property accounts for this?

f) (4 pts.) Is the hole mobility μ_p at 600 K larger than, smaller than, or the same as μ_p at 300 K?

What scattering mechanism is dominant in this temperature range?

g) (3 pts.) A hot-probe experiment is performed on this sample as illustrated below.
With an arrow, indicate the current flow direction



Problem #2

(20 pts.) IC Processing Questions

a) (4 pts.) Give one significant advantage of shallow trench isolation over LOCOS isolation.

b) (5 pts.) What are the two reasons for doing a high temperature anneal after source/drain implantation?

c) (5 pts.) What is the meaning of wet oxidation?

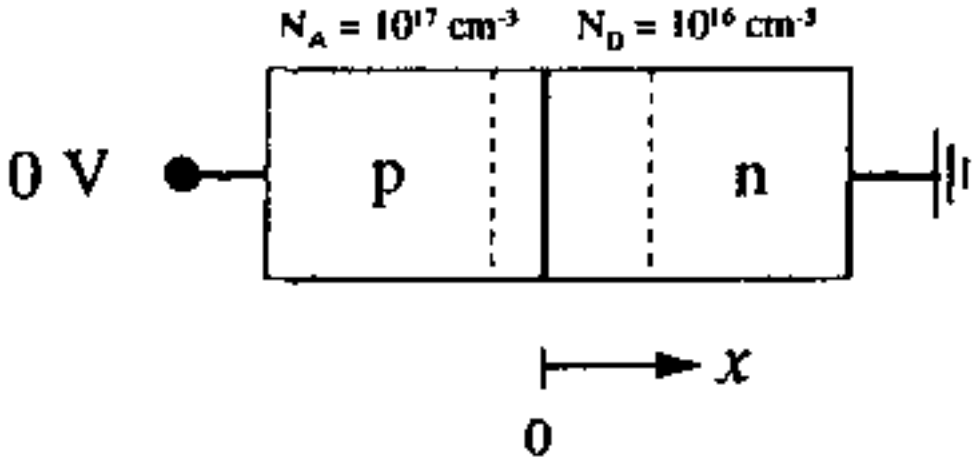
Does wet oxidation proceed at a faster, slower, or same rate compared to dry oxidation?

d) (2 pts.) What does the acronym CVD stand for?

e) (4 pts.) What is epitaxial growth used for in the fabrication of bipolar transitors?

Problem #3

(25 pts.) The pndiode illustrated below is held in euqilibrium at 300K.



Determine the electron *n* and hole *p* concentrations at the metallurgical junction x = 0.

Problem #4

(15 pts.) Indicate whether each of the following BJT performance parameters increases, decreases, or remains the same, **when the base width is decreased.**

a) (2 pts.) Emitter efficiency, *y*:

b) (2 pts.) Base transport factor, a_T:

c) (3 pts.) Early voltage, V_A:

d) (2 pts.) Current gain, B:

e) (2 pts.) Base transit time, t_BB:

f) (2 pts.) Base Gummel number, Q_B:

g) (2 pts.) Emitter Gummen number, Q_E:

Problem #5

(20 pts.) Comparison of BJT and MOSFET transconductances

a) (3 pts.) For a long-channel MOSFET biased at $V_g > V_T$, write down the expression for the transconductance g_{msat}.

b) (3 pts.) Write the expression of g_m for a bipolar junction transistor biased at collector current I_C.

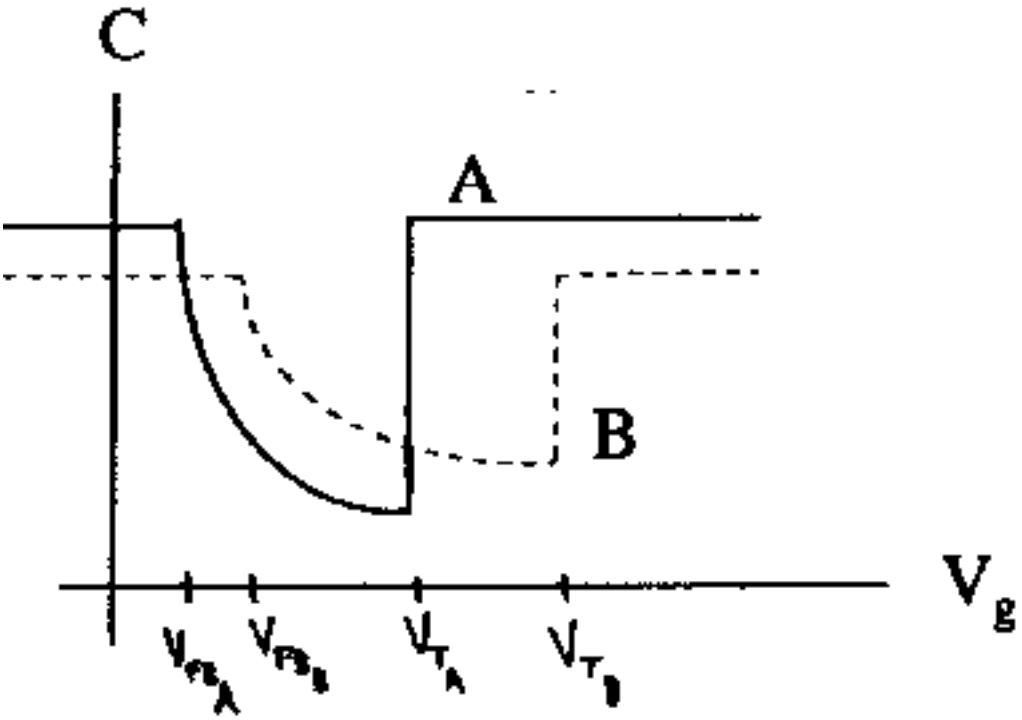
c) (6 pts.) Under the condition that $I_C^{BJT} = I_{Dsat}^{MOS}$, what is the ration g_m^{BJT}/g_m^{MOS}?

Which transistor has the larger g_m?

d) (8 pts.) Repeat (c) for the MOSFET biased in the subthreshold regime ($V_g < V_T$).

Problem #6

(10 pts.) The CV measurements for MOS capacitors A (solid line) and B (dashed line), each having the same area, are shown below.



a) (5 pts.) Are the substrates p-type of n-type?

How do you know this?

b) (5 pts.) Circle A or B to indicate the capacitor having **larger**

X_{ox}: A B

V_{FB}: A B

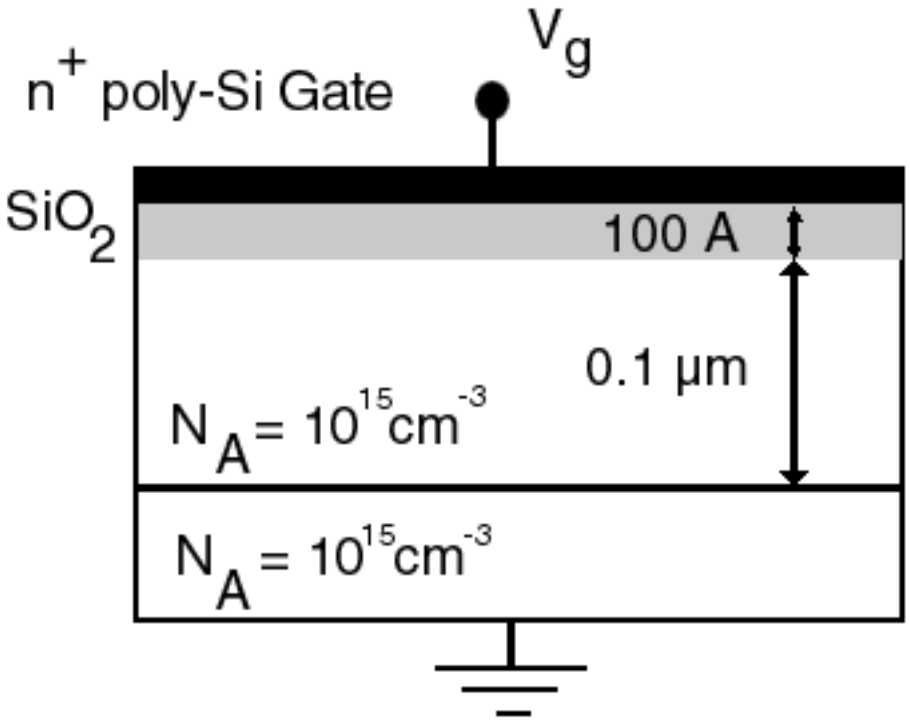
X_{dmax}: A B

N_{sub}: A B

V_T: A B

Problem #7

(30 pts.) A MOS capacitor has the following doping profile in the silicon substrate.



a) (6 pts.) Draw the energy band diagram at the flat-band condition, **i.e. when there is no band bending at the Substrate-SiO_2 interface ($E_{OX} = 0$)**.

b) (6 pts.) Calculate the flat-band voltage for part (a).

c) (6 pts.) What is the depletion region width in the substrate when $V_g > V_T$?

d) (6 pts.) Qualitatively sketch the high-frequency and low-frequenct CV curves for this MOS capacitor. Label the curves HF and LF respectively.

e) (6 pts.) What is the high-frequency capacitcance value (units of F/cm^2) at $V_g = V_T$

Problem #8

(30 pts.) Velocity saturation in an *n*-channel MOSFET may be modeled with

$$v = \frac{\mu_n \mathcal{E}}{1 + |\mathcal{E}| / \mathcal{E}_{sat}} \qquad (\mathcal{E} = \text{electric field})$$

Using this model, derive an expression for the channel potential profile $V_c(y)$ below saturation in terms of V_d, V_g, V_T, L, and E_{sat}

Problem #9

(25 pts.) MOSFET Potpourri

a) (5 pts.) Briefly describe the CMOS latch-up phenomenon in 1 to 2 sentencs.

b) (5 pts.) Briefly explain the mechanism of CMOS latch-up in 1 to 2 sentences.

c) (5 pts.) A MOSFET biased at $V_D = 2$ V has $I_D = 10^{-10}$ A at $V_g = 0$. It has a subthreshold swing S = 90 mV/decade. What is the approximate I_D at $V_g = V_T = 0.5$ V?

d) (5 pts.) List 2 things you can do to reduce subthreshold swing.

e) (5 pts.) List 2 things you can do to reduce the short-channel V_T-rolloff effect.
