Fall 1993 CS 152 Midterm II

11/23/93

You have 120 minutes to complete 125 of the 140 points. You should do 3 of te last 3 problems and indicate which. You may use a calculator or the book if you like, but you will probably do better withou it. The exam is long and hard so pace yourself and think before you write.

Show your work. Write neatly and be well-organized. Good Luck!

page	max	score
2	25	
3	15	
4	15	
5	25	
6	15	
7	15	
8	15	
9	25	
TOTAL	125	

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1.[15]Indicate which of the following are specified in the instruction set architecture (ISA) and which are determined by the machine organization (MO).

a. instruction format
b. cycle time
c. set of operations
d. data types and representations
e. power consumption
f. programmable storage
g. pipeline hazard resolution
h. CPI
i. MFLOPS

j. handling of conditions
k. number of branch delay slots
l. cache line size
m. how memory is addressed
n. number of explicit operands
o. virtual to physical address translation

2.[5]The normalized single precision IEEE floating point number of smallest magnitude is

a. 1.0*2^-127
b. 1.0*2^-126
c. -1.0*2^-127
d. 1.1*2^-126

3.[5]During the post-normalization step of an IEEE floating point addition it may be necesssary to shift the result

a. right
b. right or left
c. right by one or left by some
d. right by some or left by one
e. right by one or left by one

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4.[5]Briefly explain the difference between horizontal and vertical microcode and indicate the advantages/disadvantages of each.

5.[5]Draw the waveform for y produced by the VHDL statement

y<=a NOR b after 0.5ns

6.[5]Consider a datapath stage containing combinational logic with a critical path of 10ns between two edge-triggered flip-flops with a setup time of 1ns, propagation delay of 2ns, and a hold time of 0ns. The maximum clock skew is 1ns. What is the minimum clock period at which the datapath can be run?

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7.[7]The following diagram shows the internal structure of a register file with one read port and one

write port. Label each of the components and fill in the missing pieces of the cell detail.

diagram missing

8.[8]Compute the timing and load characteristics of the new cell C shown below from the cells A and B in the table.

	Input Load	Internal Delay	Delay per Load
A	1	5	2
B	2	3	1
Cix			
Ciy			

diagram missing

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9.[5]Briefly explain memory indirect addressing modes make it difficult to pipeline an instruction set.

10.[7]A simple code sequence and a list of potential hazards are shown below, where a12 means an occurance of location a in instruction 1 and 2. Indicate for each hazard whether it is RAW, WAW, WAR.

1. a=b+c
2. c=b+d
3. branch_zero (c) to 5
4. a=b+b
5. d=c+b

a. c12
b. b12
c. a14
d. c25
e. d25

11.[8]For the code sequence and hazards a-e in Problem 10, which hazards must be resolved by the hardware if instructions:

- are issued simultaneously to execute in parallel?
- are issued only after the previous one completes?

- complete order and perform writers in the last stage?
- issue in order and read operands in the first stage?

12.[5]In order to support virtual memory, what information must be saved by the hardware on a page fault in order for the operating system to handle the fault?

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Do three of the next four problems. Indicate which is to be graded.
13.[15]Suppose we have a machine with a 32-bit address space that is byte addressible. Bit 0 is the lsb and bit 31 is the msb of the address. It has a 64 KByte unified instruction and data cache. The cache is 2-way set associative with 32-byte blocks. Show how each field of the address is used in a cache access. Diagram the organization of the cache to make your answer clear.

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14.[15]You are given the following information about a program executing on a machine. It is a load/store architecture with a 32-bit word size and all instructions are 32-bits. The machine runs at 50 MHz. The dynamic instruction mix is a shown below. To keep things simple, the memory is word addressible and the cache line size is one word. The instruction hit rate is 90%. The data read hit rate is 50%. The data cache is write-through.

Inst Type	Freq
ALU	50%
Load	20%
Store	10%
Branch	20%

The measured bandwidth (instruction and data) at the memory is 36MB/s. What is the CPI? (Show very clearly how you calculate this! Draw yourself a picture. Make sure the units check in each step of the calculation.)

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15.[15]We have used a linear model to estimate the performance of many aspects of computer system. A model frequently applied to network is $T(n)=T0+n/BW$, where T0 is the start-up cost to send a zero length message and n is the message size. You are comparing ethernet and FDDI for a system you are

designing. A little table is shown below to help you recall the key performance parameters. Suppose that the start-up cost

	EtherNet	FDDI
Peak BW	10 Mbits/S	100 Mbits/S
Max Packet Size	1500 Bytes	4500 Bytes

to send a 1500 byte packet is 1 millisecond on either network. What is the bandwidth achieved on each network sending packets of this size (assuming no contention)?

How much additional bandwidth is achieved on FDDI if a full size packet is sent with this same start-up cost?

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16. Sketch a datapath for the following tiny instruction set and show the state diagram you would use to implement the ISA with a jump-state controller and with a time-state controller

Instruction	RTL
add rd, rs, rt	R[rd]<R[rs]+R[rt]
sub rd, rs, rt	R[rd]<R[rs]-R[rt]
lw rt, rs, im16	R[rt]<M[R[rs]+SX(im16)]
sw rt, rs, im16	M[R[rs]+SX(im16)<-R[rt]
bz rt, rs	ifR[rt]==0 then PC<-R[rs]