University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS 150 R.H.Katz
Spring 2001

SECOND MIDTERM EXAMINATION
Thursday, 22 March 2001

INSTRUCTIONS – READ THEM NOW! All work is to be done on these pages. Partial credit is given only if we can evaluate your approach: indicate your assumptions and write as neatly as possible. Points are assigned to problems based on our estimates of how long they should take – 1 point equals 1 minute. PACE YOURSELF ACCORDINGLY: it is better to get partial credit on all of the problems than to complete a handful of them. This is a closed book examination. You will not need a calculator or other information appliance. You may use a *single* 8.5" by 11" piece of paper (both sides) with prepared notes. Write your name and student ID Number at the top of each examination page.

Please refrain from discussion the examination after you have taken it. A small number of students are taking a late examination due to special circumstances.

It is a sad fact of life that cheating sometimes happens. It will not be tolerated. By signing below, you assert that all of the work included herein is your own, and that you understand the harsh penalties that will be imposed should cheating be detected – a 0 on the examination, and a letter of reprimand to your life:

_____ SID:_____
(Signature)

_____
(Name – Please Print!)

QUESTION	POINTS ASSIGNED	POINTS OBTAINED
1	5	
2	5	
3	15	
4	15	
5	20	
6	20	
TOTAL	**80**	

Student Name:_____ SID:_____

Question 1. *True/False*(5 Points)

Circle T for true and F for false below(0.5 points each):

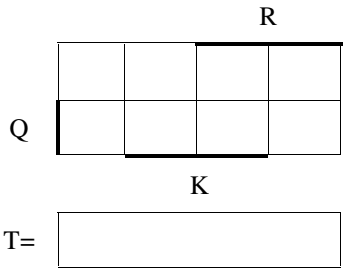
(i)	A flip-flop can enter a metastable state if its inputs change too close to the triggering clock edge.	T	F
(ii)	A synchronizer is a specialized circuit structure that guarantees that metastability will never occur.	T	F
(iii)	A Moore Machine usually has fewer states than a Mealy Machine with the same input/output behavior.	T	F
(iv)	Tri-state gates can be used to implement the same functionality as a multiplexer.	T	F
(v)	Asynchronous flip-flop inputs for reset and set should always be used to avoid outputs that cannot be interpreted as either 0 or 1.	T	F
(vi)	A 1-hot encoding uses more state flip-flops than a dense encoding.	T	F
(vii)	Two states are equivalent if they transition to the same or equivalent next states on non-identical inputs.	T	F
(viii)	To insure that flip-flops can be properly cascaded, hold times are designed to be shorter than set-up times.	T	F
(ix)	Clock-skew is a problem that arises when the clock signal is delayed in its distribution through the logic circuit.	T	F
(x)	A Moore Machine associates its outputs with the current state while a Mealy Machine's output is a function of the current state and input.	T	F

Student Name:_____ SID:_____

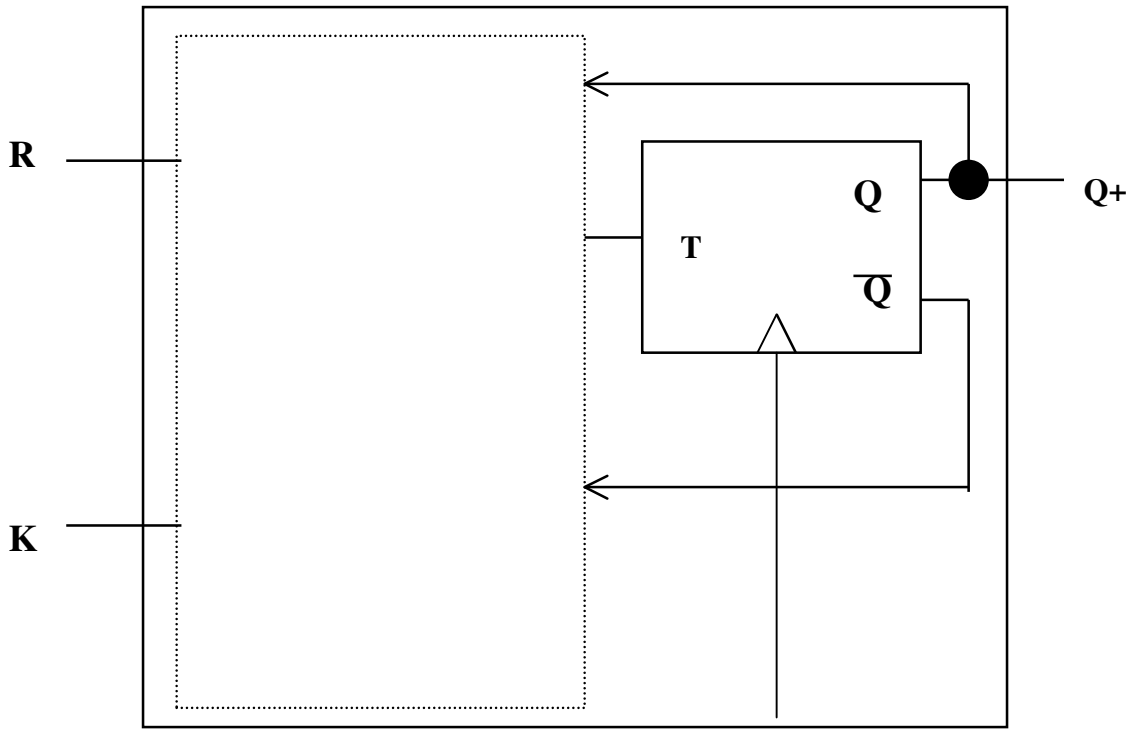
Question 2. *Flip-flop Design Using Toggle(T) Flip-flops* (5 points)
Consider a new kind of flip-flop, called the R K flip-flop, which behaves as follows. When R=K=0, the flip-flop is reset. When R=K=1, the flip-flop is set. When R=0 and K=1, the flip-flop holds its current state. When R=1 and K=0, the flip-flop complements its current state (0 becomes 1, 1 becomes 0).

Complete the State Transition Table to describe the behavior of the R K flip-flop and the necessary T input values to obtain such behavior from a Toggle flip-flop (3 points).

R	K	Q	Q+	T
0	0	0		
		1		
0	1	0		
		1		
1	0	0		
		1		
1	1	0		
		1		

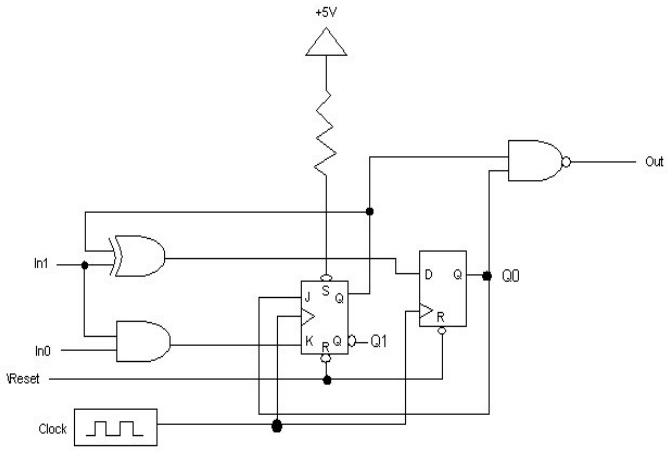


Show below the gate-level implementation of the R K FF using a Toggle FF as the basic building block (i.e. when the T input is 0, the flip-flop holds its state; when the T input is 1, the flip-flop complements its current state) (2 points).



Student Name:_____ SID:_____

Question 3. *Reverse Engineering* (15 Points)
Given the schematic below, your task is to derive a state diagram that defines the behavior of this finite state machine. The flip-flops are positive edge triggered with synchronous active low reset and set. Recall that a J K flip-flop holds its state when J=K=0, toggles its state when J=K=1, sets its state when J=1, 0, and resets its state when J=0, K=1.



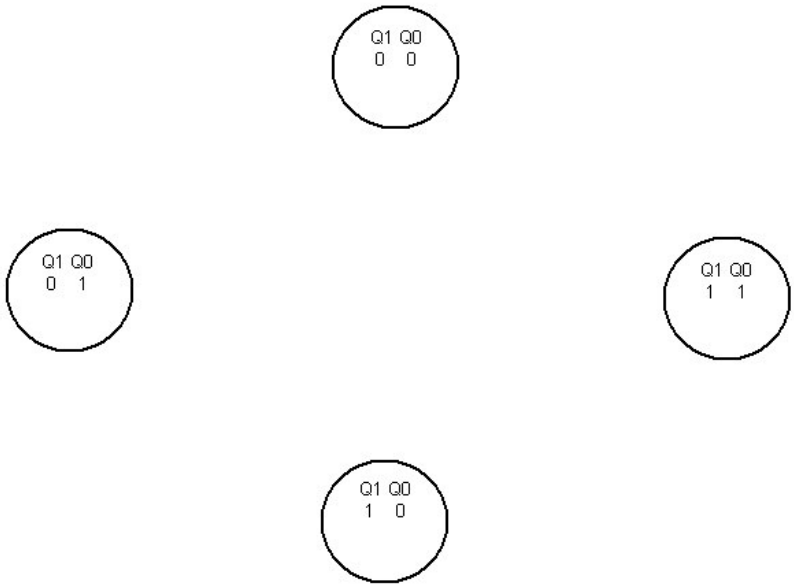
J =

K =

D =

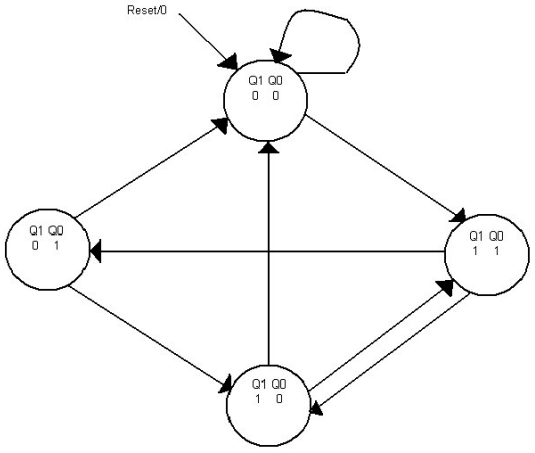
Out =

Complete the State Diagram below (15 points):



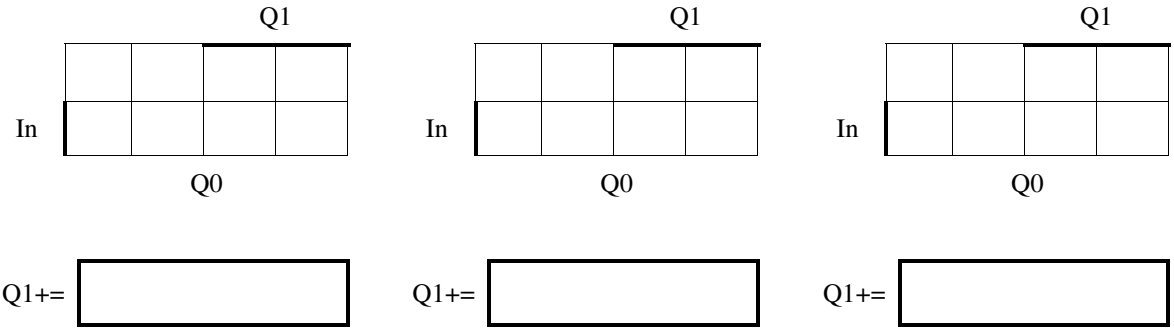
Student Name:_____ SID:_____

Question 4. *Mealy Machine Timing* (15 Points)
Consider the following Mealy Machine state diagram.

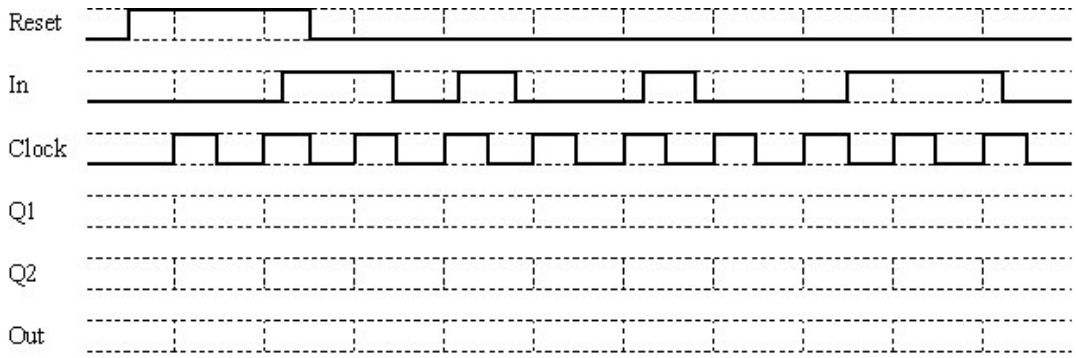


Q1	Q0	In	Q1+	Q0+	Out
0	0	0			
		1			
0	1	0			
		1			
1	0	0			
		1			
1	1	0			
		1			

Determine the next state and output logic functions for this state machine (3 points):



Complete the following timing chart. Ignore setup/hold times; assume 0 propagation delays. (12 points).



Student Name:_____ SID:_____

Question 5. *Controller Design* (20 Points)
Design an in-car "trip computer" to the following specification. Under driver control, the trip computer can display miles traveled since last reset, average speed (miles traveled/elapsed time since last reset), and miles per gallon (miles traveled/gallons consumed since last reset). The inputs to the state machine are: (1) signal to increment miles traveled (once per mile traveled), (2) increment time (once per hour), and (3) the integer number of gallons of gas consumed since the last reset. The user interface has two buttons: a *reset* and a *display* push button. By default, miles traveled since last reset is displayed. If *display* is pressed, the average speed in miles per hour is shown. If pressed again, the miles per gallon is shown. Pressed one more time, it returns to miles traveled, and the display sequence can be repeated. You may assume that display is a synchronized, debounced signal that is asserted for exactly one clock period when pressed.

(i) To make sure that you understand the specification, draw a simple block diagram that shows the controller's inputs and outputs (3 points).

(ii) Draw a simple datapath diagram for the trip computer, including any multiplexers, counters, registers, arithmetic functional units (e.g. adders, subtractors, multipliers, dividers), and display decoders and drivers you may need for its implementation. Show how they are interconnected and indicate the control signals that you need to control this datapath (10 points).

Student Name:_____ SID:_____

(iii) Draw a complete MEALY MACHINE State Diagram for your controller (7 points).

Student Name:_____ SID:_____

Question 6. *State Machine Timing* (20 Points)
PLEASE READ THE FOLLOWING SPECIFICATION VERY CAREFULLY! You are to implement a MOORE MACHINE *state diagram fragment* that does the following. It "swaps" the values in two registers inside a register file. That is, the high level operation SWAP (REG_X, REG_Y) places the contents of REG_X into REG_Y and REG_Y into REG_X where REG_X and REG_Y are two registers within a register file. It is possible to swap the contents of a register with itself.

The register file can read one register or write one register during any clock period, but not both. This is a so-called single port read/single port write register file.

This signals RD and WR control reading from and writing to the register file respectively. RED ADDRESS determines the location within the register file. The RD signal is *asynchronous.* Reading begins as soon as the signal is asserted.

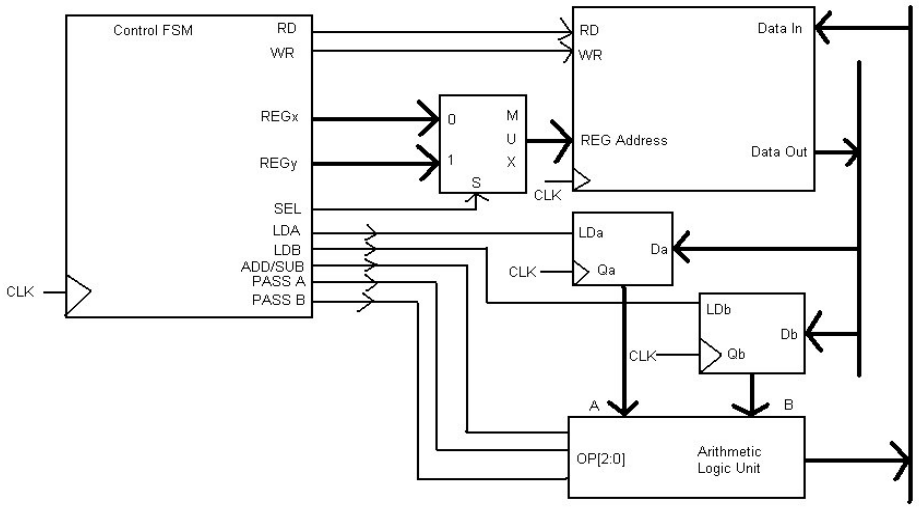
You may assume that data will be available at Data Out well before the rising edge of the clock after RD is asserted and REG ADDRESS becomes stable (i.e. propagation delay through the register file is short compared with the clock period).

The WR signal is *synchronous,* and writing takes place on the rising edge of the clock whenever WR is true. You may assume that set-up time for REG Address and Data In is much shorter than the clock period.

There are two buffer registers with synchronous LD control inputs outside the register file. They provide the A-side and B-side inputs to an arithmetic/logic unit (ALU). The ALU can perform the four operations A PLUS B (OP=100) (sum A and B inputs), A MINUS B (OP=000) (subtract B from A), PASS A (OP=010) (pass through the A input), or PASS B (OP=001) (pass through the B input).

You may assume that any of the ALU operations take place with a propagation delay much less than the clock period.

The datapath fragment is the following. Thick lines are multi-bit busses; thin lines are single bit:



(The rest of the question continues on the next page.)

Student Name:_____ SID:_____

(i) Draw a state diagram fragment below, with the fewest possible states, to implement the SWAP (REG_A, REG_B) sequence. Indicate which control signals are asserted in each state (10 points).

(ii) Complete the following timing diagram, indicating in detail when control signals are asserted and unasserted with respect to the clock (10 points).