Your Name: _____ **SID Number:** _____

UNIVERSITY OF CALIFORNIA AT BERKELEY

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Department of Electrical Engineering and Computer Sciences

CS 150 - Spring 1997
Prof. A. R. Newton

(1)	/30
(2)	/30
(3)	/30
TOTAL	**/90**

Quiz 1

Room 10 Evans Hall, 2:10pm Thursday February 20
(Open Katz only, Calculators OK, 1hr 20mins)

Include all final answers in locations indicated on these pages and in pen. Use space provided for all working. If necessary, additional sheets by staple at the end. BE SURE TO WRITE YOUR NAME ON EVERY SHEET.

1. **(a) Identify and name** the following two-input logic functions:
   (i) The output is 0 **iff** both inputs are 1.
   (ii) The output is 1 **provided the inputs are different.**
   (iii) The output is 1 **provided no more than one input variable is 1.**
   (iv) The **only time** the output is 0 is **when both inputs are 0.**

1(a) 8pts

$f_i(A,B)$ = _____ **$f_{ii}(A,B)$ = _____**

$f_i(A,B)$ is called the _____function. **$f_{ii}(A,B)$ is called the _____function.**

$f_{iii}(A,B)$ = _____ **$f_{iv}(A,B)$ = _____**

$f_{iii}(A,B)$ is called the _____function. **$f_{iv}(A,B)$ is called the _____function.**

(b) A company is controlled by a **managing director A**, **financial director B**, and **two elected members of the board, C and D**. To make a decision, **A needs the support of at least one other member of the controlling group while B needs the support of any two or more other members of the group**.
   (i) Obtain a **truth table** for the **conditions under which a decision is approved**.
   (ii) Write the **minimum Boolean sum-of-products expression** for the conditions under which the **decision goe against A.**
   (iii) Write the **minimum Boolean sum-of-products expression** for the conditions under which the **decision goe against B.**

1(b) 10pts
(i) Truth Table:

(ii) Against A = _____

(ii) Against B = _____

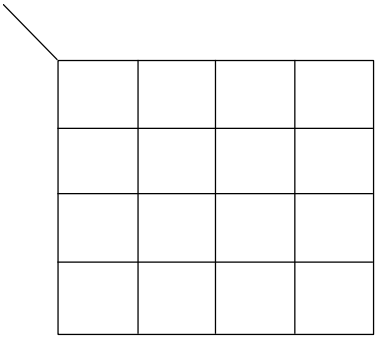
(c) You are to design a **single-output logic function, F**, for a deciding whether a four-bit binary number is **divisible by 2 or divisible by 3 (or by both).** Show the following:

(i) A **truth table for F.**
(ii) A **Karnaugh map for F**, showing a **circled set of essential prime implicants**.
(iii) A **multi-level logic expression for F** which contains the **minimum number of literals.**
(iv) A **schematic diagram which implements your logic function**. **Assume complements are available.**

1(c) 12pts

(i) Truth Table:

(ii) Karnaugh Map:



(iii) F = _____

(iv) Schematic Diagram:

Additional space for Problem 1

Your Name: _____

(2) In all parts to this question, **assume input complements are <u>not</u> available** (i.e. **an inverter or an inversion counts as a gate**.) and consider the following logic function:

F(A,B,C) = $\overline{A} \cdot \overline{B} + B \cdot C + A \cdot \overline{C}$

(a) **Hazard analysis:**

(i) If you were to **implement F directly as it is written**, as a two-level AND-OR network**, would it have the minimum number of gates+gate inputs?** Could you reduce it further as a two-level network?

(ii) If you implemented F as written, **would the circuit have any single-input static hazards**? **What type of hazard(s) are they and how would they be excited? How would you eliminate them?**

2(a) (8pts)

(i) .....

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(ii) .....

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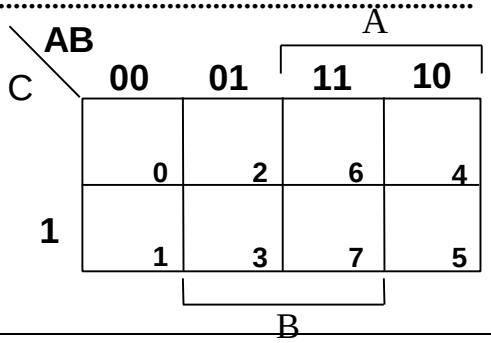


(b) **Multiplexer implementation**

(i) Implement F using **a single 8-input, 3-control-line multiplexer.**

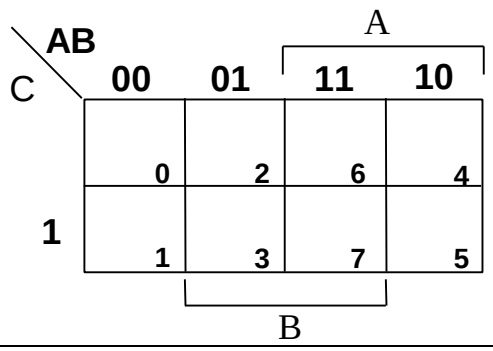
2(b) (4pts)

(i)

(ii) Implement F using **a single 4-input, 2-control-line multiplexer and a minimum number of two-input logic gates (AND, NAND, XOR, etc.) and inverters only**. **Show a Karnaugh map.**

2(b) (8pts)

(ii)



(c) **If F were to be implemented as a PLA:**

(i) Show the PLA table format for F. Indicate all **don't-cares in the product terms (rows) with an asterisk (*)** and use the **minimum number of rows.**

(ii) Would your PLA contain any **single-input static hazards,** as shown? Why?

2(c) (10pts)
(i)

(ii) .....
.....
.....
.....

Additional space for Problem 2

Your Name: _____

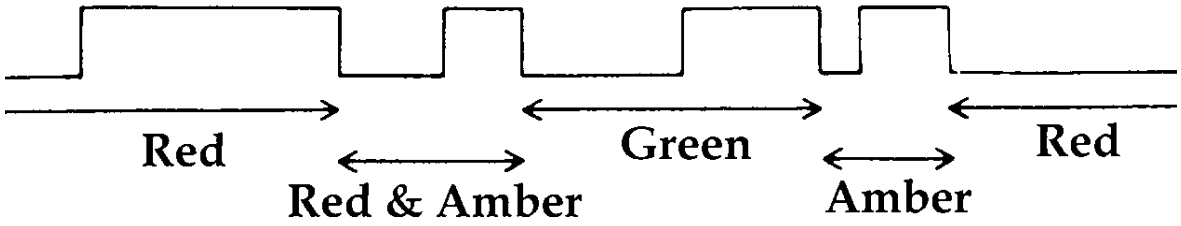
(3) (a) Design a **clocked, sequential digital machine** that will output the following sequence of 2-bit values: **00, 01, 11, 10** and then **continuously repeat the sequence from 01** (i.e. never return to 00). **Show a state transition graph.**

(i) **Implement** the machine using **D flip-flops**.

3(a) (i) (10pts)

(ii) **Implement** the machine using **T flip-flops**.

3(a) (ii) (10pts)



(b) Design a logic system to operate a set of traffic. The individual lights must be on in the following sequence: red, red & amber together, green, amber, red, etc. The lights change from one color (or color combination) whenever a 1→0 transition occurs in the input control signal, as shown above.

3(b) (10pts)

Additional space for Problem 3