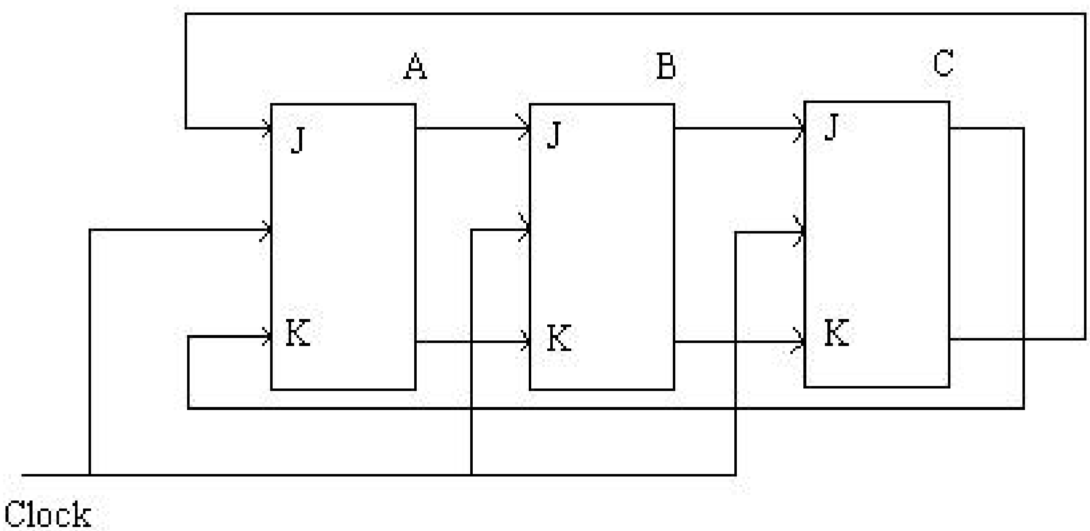
CS150, Fall 1995
Quiz #2
Professor I. Koren

Problem #1

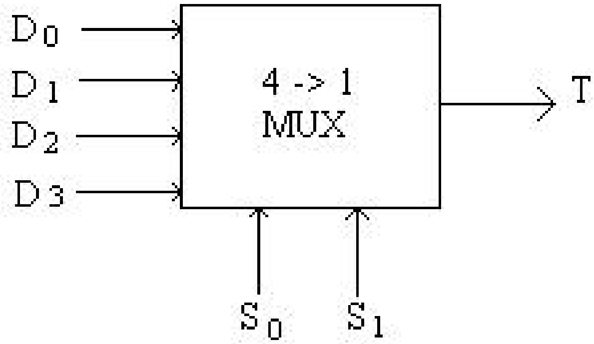
A Twisted Tail Ring counter is shown below. Show the state diagram, accounting for all possible states? Is this counter self-starting (self-correcting)? Explain.



Problem #2

A 4 --> 1 MUX (Multiplexer) shown below can be used to realize any 3-variable switching function with no added logic gates. In this problem we will try to find out whether a given 4-variable switching function *f(W, X, Y, Z)* can be realized using a single 4 --> 1 MUX *with no added gates.*

$S_0 S_1$	T
00	D_0
01	D_1
10	D_2
11	D_3



Problem #2a

Given the function *f(W, X, Y, Z)* = (Sigma)m(2, 3, 4, 6, 7, 15) + (Sigma)d(0, 5, 12, 13) and its K-map, is it possible to realize it using a single 4 --> 1 MUX by choosing S_1 S_0 = W X, D_i (a member of) {0, 1, Y, not Y, Z, not Z} ; i = 0, 1, 2, 3 (the complements of the input variables are available). If your answer is positive show the realiziation; if it's negative explain why.

Problem #2b

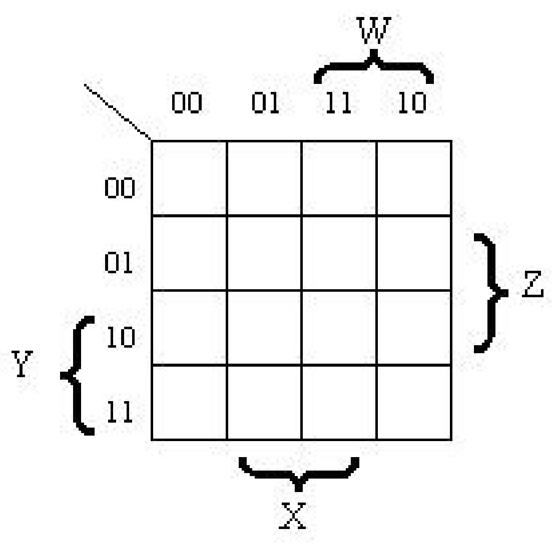
Repeat (a) for the choice S_1 S_0 = Y Z.

Problem #2c

Repeat (a) for the choice S_1 S_0 = W Z.

Problem #2d

How do you check with the aid of K-maps, the possibility of realizing a given 4-variable function using a single 4 --> 1 MUX?



Problem #2e

Estimate the percentage of 4-variable functions which can be realized using a single 4 --> 1 MUX.

Problem #3

State whether each of the following is true or false. If true prove or explain, if false give a counter example. A correct True or False ansewr with no explanation is worth only 1 point.

Problem #3a

No static hazards may occur when implementing a 4-variable logic function using a 4-to-16 decoder.

Problem #3b

The radix-4 modified Booth algorithm which examines three multiplier bits at once (with the rightmost bit serving as a reference bit) always results in the minimum number of add/subtract operations.

Problem #3c

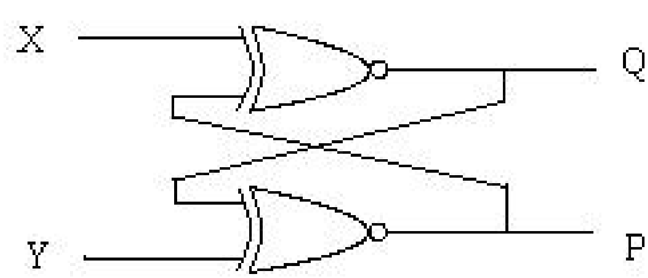
A 2048 X 1 ROM can be used to implement an 8:1 MUX.

Problem #3d

Every finite state machine can be implemented as a Linear-Feedback-Shift-Register (LFSR).

Problem #3e

The following circuit can serve as a Flip-Flop in any sequential circuit.



Problem #4

Show an implementation of a circuit that multiplies the (unsigned) input number $X = x_4\ x_3\ x_2\ x_1\ x_0$ by 7 using only Full Adders (FAs) and inverters. In other words, the output number $Z = z_{n-1}\ z_{n-2} \ldots z_1\ z_0$ satisfies Z = 7 * X. Determine the required number ofoutput bits, n, and show the implementation of your Multiply-by-7 circuit using as few FAs and inverters as possible.

Posted by HKN (Electrical Engineering and Computer Science Honor Society)
University of California at Berkeley
If you have any questions about these online exams
please contact mailto:examfile@hkn.eecs.berkeley.edu