UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering
and Computer Sciences
Computer Science Division

Computer Science 150

Fall 1991 - First Midterm Examination

Professor R. H. Katz

In taking this examination, you agree that all work recorded herein is your own. A student caught in the act of cheating will be given a grade of F on this examination and a letter will be written to his or her file.

All work is to be done on the attached sheets and under no circumstances are blue books or loose sheets to be used. Write your name at the top of every sheet.

Read the questions carefully. If something appears ambiguous, write down your assumptions. The points have been assigned according to the formula that 1 point = 1 exam minute, so pace yourself accordingly.

Question 1: Tri-State and Open Collector Gates [10 points]

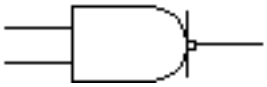
The 2:1 multiplexor function that has two data inputs A and B, a select control input S, and a single *positive-logic* output Z that operates according to the following truth table:

S	Z
0	A
1	B

(i) Draw a schematic that implements this function using only the following gates as building blocks [5 points]:

(ii) Implement the same function using only the following building blocks [5 points]:

Open Collector NAND



Conventional Inverter

Question 2: Word Problems [15 points]

A logic network has four inputs; Input0, Input1, Input2, Input3, and two outputs Output0, Output1:

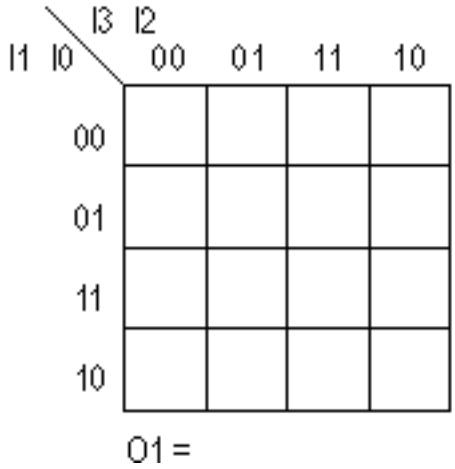
At least one of the inputs is always asserted high. If a give input line has a logic one applied to it, then the ouput signals will encode its indes in binary. For example, if input Input2 is asserted, then the output reads Output1 = 1, Output0 = 0. If two or more inputs are at a logic one, the output will be set according to which input has the highest index (Input3 > Input2 > Input1 > Input0).

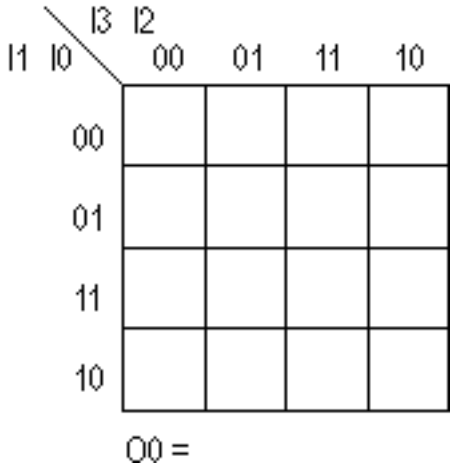
Fill in the Truth Table [5 points]:

I3	I2	I1	I0	O1	O0
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1		

I3	I2	I1	I0	O1	O0
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

Fill in the K-Maps for Output1 and Output0, and find the Boolean expression fo the minimum sum of products implementation [10 points]:

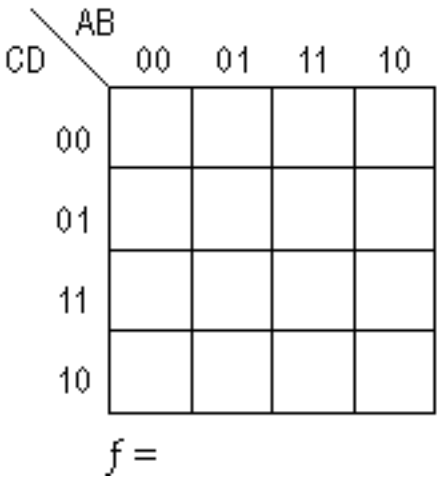


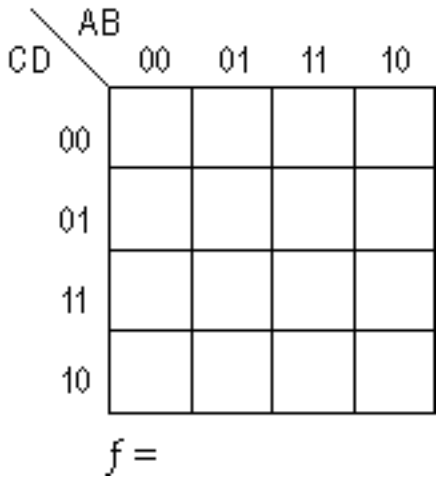


Question 3: Two Level Minimization [10 points]

"The minimized sum of products description of a Boolean function is always unique."

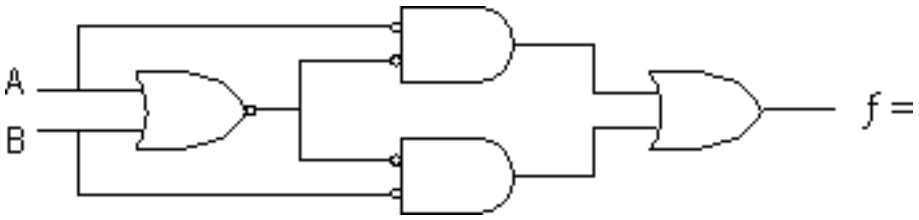
Demonstrate that this statement is FALSE by counter-example. Fill in the following two 4 variable K-maps with identical patters of 1's and 0's. Show that there are two different ways of circling the 1's to yield alternative minimized sum of froducts expressions with the same number of terms and literals.





Question 4: Multilevel Functions [10 points]

Write down the function represented by the following circuit network in a multi-level *factored form* using AND, OR, and NOT operations only -- that is, no NAND or NOR operations [5 points]:



show your derivation below:

Factored form

Derive the simplest Boolean expression (minimum number of literals and fewest number of gates) for this function represented by the above schematic [5 points]:

f =

Minimum Number of Literals/Gates

Question 5: Gate Logic [10 points]

It is sufficient to specify any Boolean expression in terms fo three types of gates: AND, OR and NOT (inverter). A set of logical operations if *functionally* if any Boolean function can be expressed in terms of this set of operations. Obviously, AND, OR and NOT are *functionally complete*.

(i) NOT and one of AND or OR is also functionally complete. Show that a two-input AND gate can be constructed from NOT and OR gates. Draw the schematic [2 points].

(ii) Show how an OR gate can be constructed from AND and NOT gates [2 points].

(iii) Prove that the NAND gate by itself is functionally complete by showing how it can be used to implement AND, OR, and NOT gates [2 points].

(iv) Is the NOR gate functionally complete? If so, show how to implement AND, OR and NOT. If not, explain why [2 points].

(v) Is the XOR gate functionally complete (simply answer yes or no)? [2 points].

Question 6: Canonical Forms [10 points] [10 points]

Given the following function in sum of products form (not necessarily minimized):

$$f(A,B,C,D)=\overline{A}\cdot B\cdot C + A\cdot D + A\cdot C$$

Reexpress the function in :

(i) cononical product of sums form. Use "Big M" notation [2 points].

(ii) minimized product of sums form [2 points].

(iii) $\overline{f}$ in minimized product of sums form [2 points]

(iv) $\overline{f}$ in minimized sum of products form [2 points]

(v) implement ***f*** using a single AND-OR-INVERT gate [2 points].

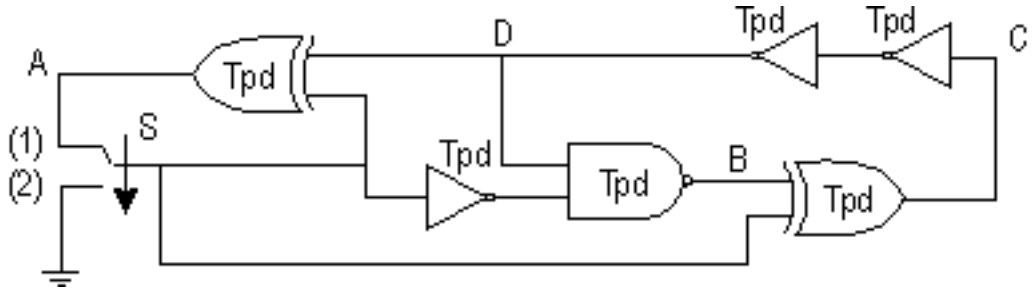
Question 7: Waveforms [10 points] [15 points]

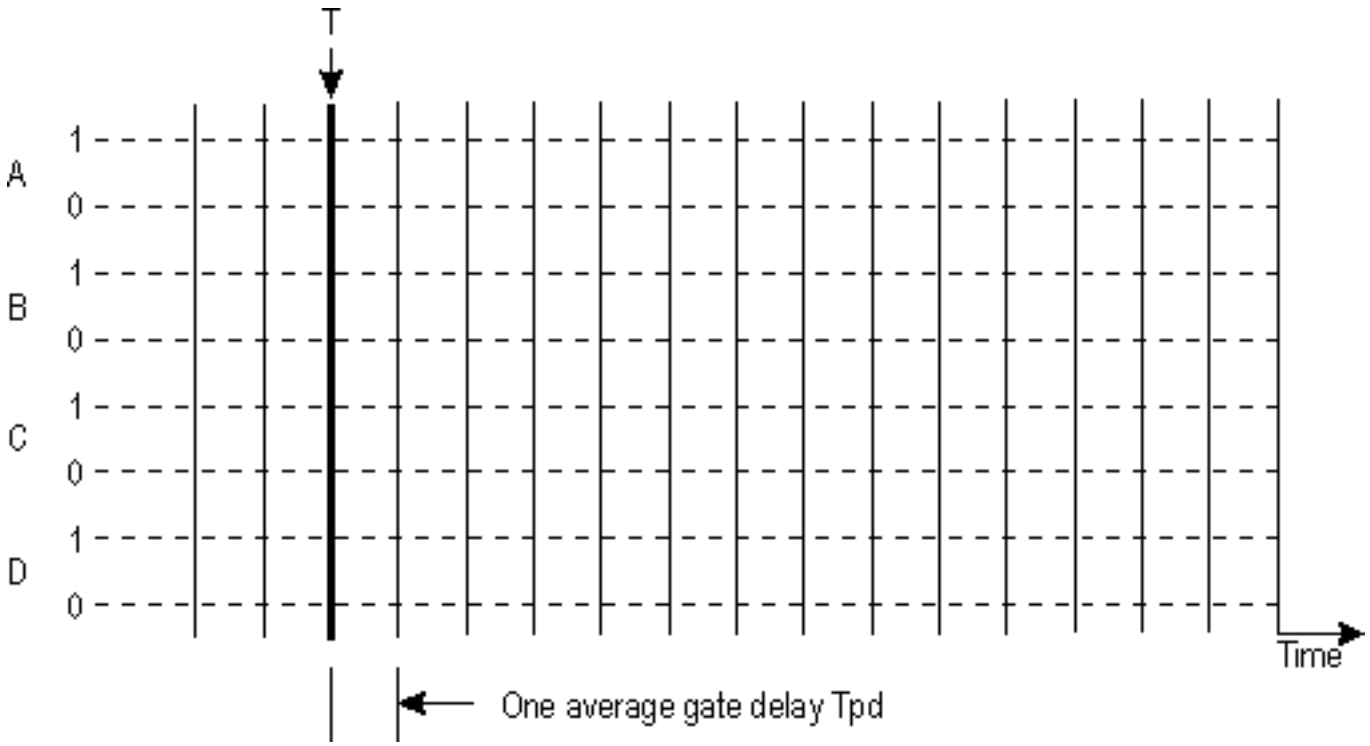
Start by finding a non-oscillating starting condition for the following circuit with the switch S in position 1 (up) as shown below. Fill in the iming waveform at the bottom of the page with your initial condition for the circuit nodes labeled A, B, C, and D to the left of the time point labeled T [5 points].

WARNING: It is very easy to choose an initial configuration that oscillates. A unique non-oscillating configuration does exist. *Start your reasoning with the tightest loops, or make an educated guess and verify that the assumed state is indeed non-oscillaing.*

At time T, the switch is moved from position 1 to position 2 (down).

Fill in the rest of the timing diagram with the logic values of the signals at points A, B, C, and D in the given circuit (10 points).



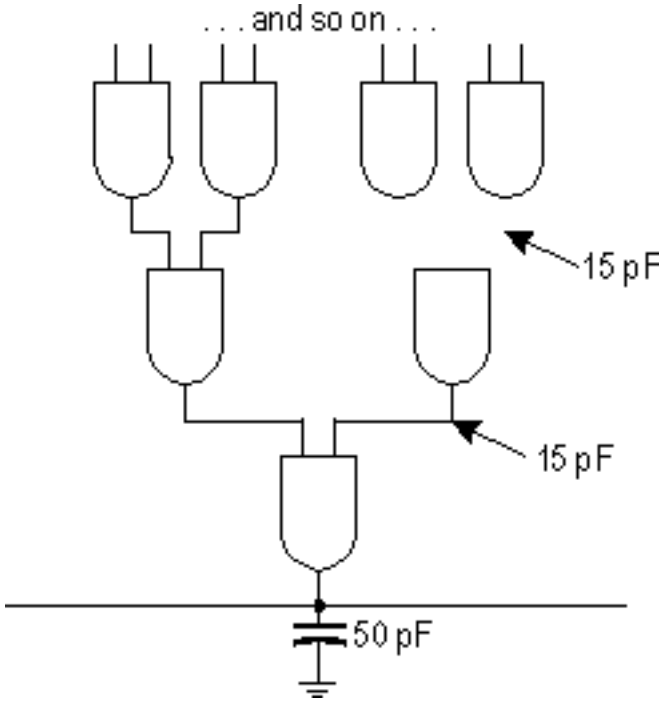


Question 6: TTL Data Book [10 points] [10 points]

Someone has constructed a giant 32-input AND gate from a cascaded tree of 2 input AND gates of type SN74S08. This circuit is to drive a bus with 50 picofarads (pf) of capacitance. Assume that the typical capacitance of interanl circuit nodes is more like 15 pF. Show your method of reasoning and computation to insure partial credit. Carefully examine the extract of the TTL Data Book found on the following page for relevant technical information about the gates.

(i) What is the typical average dely through this circuit? [5 points]

(ii) What is the typical average DC power consumption of this circuit? [5 points]



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translated to HTML by Walter Hsiao
Eta Kappa Nu (January 1996)